1. ALL RESISTANCE VALUES ARE IN OHMS, 0 1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X2818/MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
5	0047122567	ENGINEERING RELEASED	2023-08-29

LAST_MODIFICATION=Tue Aug 29 09:29:00 2023

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	Table of Contents	eli	10/12/2020
2	2	Reference Design Sync Tables		
3	3	BOM Configuration		
4	4	PD Parts		
5	5	SOC: CONFIG STRAPS	T585_REF_SOC_H15G_0.0.27	
6	6	SOC: MISC	T585_REF_SOC_H15G_0.0.27	
7	7	SOC: RESETS,CLOCKS,DEBUG	T585_REF_SOC_H15G_0.0.27	
8	8	SOC: GPIOS,NAND,MTP,UART	T585_REF_SOC_H15G_0.0.27	
9	9	SOC: I2S,I2C,SPI,THROT,CFG	T585_REF_SOC_H15G_0.0.27	
10	10	SOC: ISP, MIPI	T585_REF_SOC_H15G_0.0.27	
11	11	SOC: LPDP	T585_REF_SOC_H15G_0.0.27	
12	12	SOC: PCIE	T585_REF_SOC_H15G_0.0.27	
13	14	SOC: CIO	T585_REF_SOC_H15G_0.0.27	
14	19	SOC: SPI NOR, SEP ROM	T585_REF_SOC_H15G_0.0.27	
15	20	SOC: SOURCE TERMS		
16	21	SOC: SOURCE TERMS		
17	22	SOC: DUMMY DAM		12/12/2022
18	23	SOC: POWER PCPU	T585_REF_SOC_H15G_0.0.27	
19	24	SOC: POWER ECPU	T585_REF_SOC_H15G_0.0.27	
20	25	SOC: POWER SRAM	T585_REF_SOC_H15G_0.0.27	
21	26	SOC: POWER GRAPHICS	T585_REF_SOC_H15G_0.0.27	
22	27	SOC: POWER MEMORY	T585_REF_SOC_H15G_0.0.27	
23	28	SOC: POWER FIXED	T585_REF_SOC_H15G_0.0.27	
24	29	SOC: POWER VDD12	T585_REF_SOC_H15G_0.0.27	
25	30	SOC: POWER VDDIO, LOW, CIO	T585_REF_SOC_H15G_0.0.27	
26	40	SOC: GND (1 OF 2)	T585_REF_SOC_H15G_0.0.27	
27	41	SOC: GND (2 OF 2)	T585_REF_SOC_H15G_0.0.27	
28	50	Secure Element	SecureElement	05/22/2023
29	51	Battery Connector	X 818	01/31/2023
30	52	PBUS SUPPLY & BATTERY CHARGER	T585_REF_CHARGER_MANDOLA_MP_THIN_0 9 0	
31	53	BATTERY CHARGER SUPPORT	T585_REF_CHARGER_MANDOLA_MP_THIN_0.9.0	
32	54	MAGSAFE: CONNECTOR		
33	55	MAGSAFE: PORT CONTROLLER	T585_REF_MAGSAFE_ACE3_0.4.8	
34	56	MAGSAFE: CONTROLLER SUPPORT	T585_REF_MAGSAFE_ACE3_0.4.5	
35	57	POWER: 3V8 AON (1/2)	T585_REF_VR_ICEMAN_1.59.0	
36	58	POWER: 3V8 AON (2/2)	T585_REF_VR_ICEMAN_1.59.0	
37	59	POWER: 3V8 AON SUPPORT	T585_REF_VR_ICEMAN_1.59.0	
38	77	SPMU: INPUT PWR, BULK, BSTLQ	T585_REF_PMU_STOWE_VALE_H15G_0.37.0	
39	78	SPMU: LDO, SW	T585_REF_PMU_STOWE_VALE_H15G_0.37.0	
40	79	SPMU: GPIO, VSS	T585_REF_PMU_STOWE_VALE_H15G_0.37.0	
41	80	SPMU: ALIASES, SUPPORT		
42	81	MPMU: INPUT PWR, BUCK 0, 1, 2	T585_REF_PMU_STOWE_VALE_H15G_0.37.0	
43	82	MPMU: BUCK 3, 4, 7, 9, 11, 13, SW	T585_REF_PMU_STOWE_VALE_H15G_0.37.0	
44	83	MPMU: LDO	T585_REF_PMU_STOWE_VALE_H15G_0.37.0	
45	84	MPMU: MISC CKT, VSS	T585_REF_PMU_STOWE_VALE_H15G_0.37.0	
46	85	MPMU: GPIO	T585_REF_PMU_STOWE_VALE_H15G_0.37.0	
47	86	MPMU: ALIAS, PULLS		
48	87	MPMU: SUPPORT		
49	88	PMU: SUPPORT - FF		
50	121	----		04/30/2023
51	123	POWER: 5V S2	T585_REF_VR_5V_LT8642_1_LP_0.2.0	
52	126	POWER: 5V, 3V3 Support		
53	127	POWER: 3V3 S2	951-20715_0.5.0 2023-08-28	
54	128	Power: Load Switches		10/25/2022
55	130	I2C: AP, DISP		
56	131	I2C: ISP, AOP, SEP		
57	132	I2C: SMC		
58	135	SENSORS: POWER HIGH SIDE (1/2)		
59	136	SENSORS: POWER HIGH SIDE (2/2)		
60	138	SENSORS: POWER LOW SIDE		10/26/2022

LAST_MODIFICATION=Tue Aug 29 09:29:00 2023

PAGE	CSA	CONTENTS	SYNC	DATE
61	140	SENSORS: POWER SUPPORT		
62	141	SENSORS: THERMAL		
63	144	SENSORS: MOTION	T585_REF_IMU_SOVEREIGN_0.16.0	
64	147	USB-C: Connector(s)	vsun	02/15/2023
65	150	USB-C: High Speed ATC0	T585_REF_USBC_LFKA_3PRT_ACE3_0.46.0	
66	151	USB-C: High Speed ATC1	T585_REF_USBC_LFKA_3PRT_ACE3_0.46.0	
67	152	USB-C: Support 1 ATC01	T585_REF_USBC_LFKA_3PRT_ACE3_0.46.0	
68	153	USB-C: Support 2 ATC01	T585_REF_USBC_LFKA_3PRT_ACE3_0.46.0	
69	154	USB-C: Port Controller ATC0	T585_REF_USBC_LFKA_3PRT_ACE3_0.46.0	
70	155	USB-C: Port Controller ATC1	T585_REF_USBC_LFKA_3PRT_ACE3_0.46.0	
71	156	USB-C: USB2 RPT	T585_REF_USBC_LFKA_3PRT_ACE3_0.46.0	
72	157	USB-C: Support 3 ATC01	T585_REF_USBC_LFKA_3PRT_ACE3_0.46.0	
73	159	USB-C: ATC01 REGULATORS	T585_REF_VR_RT13_PORTABLES_X5R_0.3.0	
74	162	USB-C: PROJECT SUPPORT		10/27/2022
75	200	WIFI/BT: MODULE	T585_REF_WIRELESS_WILLAMETTE_0.36.0	
76	201	WIFI/BT: ANTENNA and GND	T585_REF_WIRELESS_WILLAMETTE_0.36.0	
77	220	STORAGE: SSD0 S5E MK2 <0>	T585_REF_STORAGE_S5E_MARK2_0.28.0	
78	221	STORAGE: SSD0 S5E MK2 <1>	T585_REF_STORAGE_S5E_MARK2_0.28.0	
79	230	STORAGE: SSD Support		
80	234	CAMERA: FLEX CONNECTOR	X2818	02/15/2023
81	236	eDP Display Connector	X2818	01/31/2023
82	237	DISPLAY POWER SEQUENCER	T585_REF_PANELPWR_BNM_0.9.0	
83	238	BEN: CONTROLLER	T585_REF_BLC_BEN_0.29 0	
84	239	BEN: PBUS E-Fuse		
85	240	PMU: SAN DIEGO	T585_REF_PMU_SAN_DIEGO_0.21.0	
86	241	PMU: SAN DIEGO SUPPORT		
87	243	SECDIS: SAK, AMR+LAS		08/17/2023
88	246	AUDIO AMPLIFIERS (1/2)	T585_REF_SPKRAMP_SN012776_3.10.0	
89	247	AUDIO AMPLIFIERS (2/2)	T585_REF_SPKRAMP_SN012776_3 10.0	
90	248	Audio Connectors		01/31/2023
91	250	BLC: KEYBOARD BACKLIGHT	T585_REF_BLC_BEN_KBD_ONLY_0.15.0	
92	251	Keyboard Support		10/25/2022
93	252	Keyboard Connector		10/26/2022
94	253	TRACKPAD SUPPORT	T585_REF_TPAD_IF_PKG_SMALL_0.17.0	
95	254	Trackpad Connector		10/26/2022
96	259	----		04/30/2023
97	270	DEBUG		
98	281	Desense 1		
99	282	Desense 2		
100	283	Desense 3		
101	400	POWER ALIASES 1		
102	401	POWER ALIASES 2		
103	402	POWER ALIASES 3		
104	403	POWER ALIASES 4		
105	405	Signal Aliases 1		10/25/2022
106	406	Signal Aliases 2		10/27/2022
107	420	SOC: ALIASES GPIO		
108	421	SOC: ALIASES SPI, I2S		
109	423	SOC: ALIASES LPDP RX		
110	424	SOC: ALIASES PCIE, LPDP TX		
111	425	SOC: ALIASES CAMERA, USB, MISC		
112	501	17.4 PHYSICAL CSETS		
113	502	17.4 SPACING CSETS, ISO		
114	503	17.4 SPACING CSETS, CLASS-CLASS		
115	601	BOM: SOC		
116	602	BOM: NAND		
117	603	BOM: Prog and Module Parts	X2818	06/15/2023
118	604	BOM: PMU		
119	610	BOM: Alternates		03/15/2023
120	611	BOM: Variants		

Table of Contents

DRAWING TITLE: SCHEM,MLB,X2818

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 1 OF 801

SHEET: 1 OF 121

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: TO MAINTAIN THIS DOCUMENT IN CONFIDENCE; NOT TO REPRODUCE OR COPY IT; NOT TO RELEASE OR PUBLISH IT IN WHOLE OR PART; ALL RIGHTS RESERVED.

www.repairlap.com

Reference Design Sync Tables

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD SO	SYNC_DATE TIME
T585	REF_SOC_H15G	5-12,14,19,23-30,40-41	0 0 27	H	2023_05_02_11 55 26
T585	REF_SE_JUNO	50	1 3	H	2023_05_16_10 36 04
T5 5	REF_CHARGER_NAND LA_MP_ HIN	52,53	0 9 0	H	2023_06_0 _16 07 41
T585	REF_MAGSAFE_ACE3	55	0 4 8	H	2023_06_15_09 03 14
T585	REF_USBC_LPKA_3PRT_ACE3	150-157	0 46 0	H	2023_06_01_16 07 27
T585	REF_VR_ICEMAN	57,58,59	1 59 0	H	2023_05_03_19 56 24
T585	REF_PMU_STOWE_VALE_H15G	77-79,81-85	0 37 0	H	2022_12_01_12 59 11
T585	REF_VR_5V_LT8642_1_LP	123	0 2 0	H	2023_01_24_17 09 32
T585	REF_VR_3V3_DISPLAY	127	0 5 0	H	2023_06_15_09 03 47
T585	REF_IMU_SOVEREIGN	144	0 17 0	H	2022_10_24_11 04 03
T585	REF_STORAGE_S5E_MARK2	220,221	0 28 0	S	2023_08_08_16 01 10
T585	REF_PANELPWR_BNM	237	0 9 0	S	2022_10_24_11 04 25
T585	REF_BLC_BEN	238	0 29 0	S	2022_10_24_11 04 36
T585	REF_PMU_SAN_DIEGO	240	0 21 0	S	2022_10_24_11 04 47
T585	REF_SECDIS_AMR_LAS_H15G	243	0 9 0	H	2023_06_01_16 08 46
T585	REF_SPKRAMP_SN012776	246,247	3 10 0	H	2022_10_24_11 04 59
T585	REF_VR_H713_PORTABLES_X5R	159	0 3 0	H	2023_02_15 14 35 47
T585	REF_WIRELESS_WILLAMETTE	200,201	0 37 0	H	2023_06_15_ 9 03 33
T585	REF_TPAD_IF_PKG_SMALL	253	0 17 0	S	2023_05_10_10 14 34
T585	REF_BLC_BEN_KBD_ONLY	250	0 15 0	S	2023_06_01_16 07 50

PIN DELAY MAPPING FILE	
RE ERENCE DE GN OR	IN DE A CSV E N ME
U0600	2023_01_24_0630_BALLBAR_DRAC_3 14_PI DELA E08.csv

PART SWAP CONFIGURATION			
REPLACE APN/REFDES	WITH APN	PAGES	DELETE PROPERTY
117S00090	117S00064	54,55,150-157	?
117S00095	117S00065	54,55,57,150-157	?
117S00122	11 S00084	54, 5,15 -157	?
117S00129	117S00068	54,55,57,150-157	?
117S0105	117S00068	54,55,57,150-157	?
117S00081	118S00339	54,55,150-157	?
117S00115	118S00257	54,55,150-157	?
117S00096	117S00066	54,55,57,150-157	?
117S00130	117S00100	54,55,150-157	?
117S00124	118S00329	54,55,150-157	?
118S00334	118S00259	54,55,150-157	?
131S00003	131S00333	54,55,57,150-157	?
117S00123	117S00101	54,55,150-157	?
117S00111	118S00292	54,55,150-157	?
117S00112	118S00332	152	?
131S00464	131S00170	58	?
118S00397	118S00263	58	?
118S00367	118S00306	57	?
R5762,R5763	1170 0045,1170000 7	57	?
R5760,R5761	1170 0040,1170000 3	57	?
RF333,RF335	1170 0076,1170000 6	153	?

10k 0201 -> 01005
100k 020 - 01005
33 0201 - 01005
47k 0201 5% -> 47k 01005 5%
47k 0201 5% -> 47k 01005 5%
5.1k 0201 5% -> 4.99k 01005 1%
200k 0201 5% -> 200k 01005 1%
1M 0201 5% -> 1M 01005 1%
470k 0201 5% -> 470k 01005 5%
33k 0201 5% -> 33k 01005 1%
200 0201 1% -> 200 01005 1%
10pF 0201 -> 10pF 01005 2%
3.3k 5% 0201 -> 3.3k 5% 01005
15 5% 0201 -> 15 1% 01005
1.5k 5% 0201 -> 1.5k 1% 01005
220pF 0201 -> 220pF 01005
1 1% 0201 - 1 1% 01005
2.21k 1% 0201 -> 2.21k 1% 01005
0 0201 -> 0 01005

SYNC DATE=

PAGE T LE
Reference Design Sync Tables

Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
RE ISION 5.0.0
BRANCH dvt-1
PAGE 2 OF 801
SHEE 2 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC
HE P SE OR AGREES O HE FOLLOWING
I O MA N A N IS DOCUMEN N CONF DENCE
II NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR
I ALL R GH S RESER ED

www.repairlap.com

A BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	SCHEM,PCBF,ALTERN TE:PART,ALT_CMN,COMMON,MLB_PROGPARTS, LB_USBC,MLB_POWER,MLB_PMU,MLB_MISC,MLB_BLC,MLB_TCON,MLB_WIRELESS,MLB_BLC KB ,MLB_IPD,MLB_SECDIS,MLB_SPKRAMP,DVT
MLB_USBC	OTP_CONN CTRL _S PI TAGLE,ATCKCMN:BLC_A09_DEV,USBCPC:PORTA LE_A1 USBC_DUAL_KIS:YES,LPMA_TEST_MODE:NO,ATCRT R ROM CFP_ALARM,STRAPS_L4:NO,EYE_BOOST_PWM:DEFAUL _5GHz ,OR C_DUAL_DFU:YES,USBCPC_A1:DUY
MLB_PROGPARTS	SOC_ROM:BLANK,RT13_ROM:BLANK,JUNO:A0_PROD,UPC01_ROM:BLANK,UPC5_ROM:BLANK
MLB_POWER	P3V8AON_IC:A2_R170,P3V8AON_LPM,MANDOLA:EVT,P5VS2PWREN_BYPASS:NO,3V8_AON_SNSAMP:2STG,3V8_AON_THRPWM:YES
MLB_PMU	MPMU_IC:A1_CPG,SPMU_IC:A1_CPG,PMU_BULK_VDDQL,PMU_32K_CLK:XOSC,PMU_FB:PP,BUCK6_BULK_REG,PMU_FBUS:BATT33,SPMU_RSTLQ_CAPS,MPMU_RSTLQ_CAPS,PMU_OUT32K:WLBT
MLB_SPKRAMP	SPKR_ID:NO
MLB_DEV	SENSORS:DEV,DEVELOPMENT,USBC_DBG,BTN_DBG,BATT_DISCON_BUTTON,DEV_IPD,DBG_TCON_UART
MLB_BLC	BLC_BEN_IC:V8,BLC_5V_CAP:4P7_UF,BLC_5V_SERIES:10_OHM_0201,BLC_KBD_BOOST_USED:NO,DISP_I2C_BUFFER:NO
MLB_TCON	PMIC_SDG_VBUCK1:NO,SDG_TI,SDG_TI_PROG:X2203,PMIC_SDG_VGH:ZRBCAP,PMIC_SDG_OUT6:ZRBCAP
MLB_WIRELESS	RF_CONN
MLB_MISC	BOARD_ID,BOOST_CFG_2,BOOST_CFG_1,TPAD_32KCLK:YES,SENSOR_INS,REFIMU_IC:BMI296,WIFI_PWR:NO,DEV_DFU:TAGFU,REFIMU_RE400:47K,I2C_PNB_PU:TIN ,RSLOC:YES
MLB_BLC_KBD	BLC_KBD_BEN_IC:V4,BLC_KBD_5V_CAP:4P7_UF,BLC_KBD_5V_SERIES:10_OHM,BLC_KBD_KBD_BOOST_USED:NO,BLC_KBD_SW_MODE_DEBENGE,BLC_KBD_PWM:TKN0101,BLC_KBD_PWM_OE:CTL
MLB_IPD	TPAD_SOC_PULLUP:47K,IPD_SPI_CS_R:20_OHM,IPD_SPI_CLK_MOSI_R:51_OHM
MLB_SECDIS	REFSECDIS_RR302:47K,REFSECDIS_IPD:1V2

B Build Specific Groups

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARD_ID_4
PROTO1_BU	BOARD_REV_3,BOARD_REV_2,BOARD_REV_1
PROTO1	BOARD_REV_3,BOARD_REV_2,BOARD_REV_0
EVT1	BOARD_REV_3,BOARD_REV_2
EVT2	BOARD_REV_3,BOARD_REV_1,BOARD_REV_0
DVT	BOARD_REV_3,BOARD_REV_1

Pull-ups BOARD_ID[7 0] 8'b0011_0000
Start at 1 to match board APN Rev.
Pull-downs: 4'b0001
Pull-downs: 4'b0010
Pull-downs: 4'b0011
Pull-downs: 4'b0100
Pull-downs: 4'b0101

C RF BOM Groups

BOM GROUP	BOM OPTIONS
RF_COMMON	SCHEM,PCBF,RF_CONN

D Top-Level APNs

PAR #	Q	DE CRIP ION	REFERENCE DE IGNA OR S)	CRI ICAL	BOM OP ION
051-09343	1	SCHEM,MLB,X2818	SCHEM	CRITICAL	SCHEM
820-03285	1	PCBF,MLB,X2818	PCBF	CRITICAL	PCBF
685-00547	1	COMMON PARTS,MLB,X2818	CBOM	CRITICAL	CMN_PARTS_BOM
985-02073	1	DEV PARTS,MLB,X2818	DEV1	CRITICAL	DEV_PARTS_BOM

E Reference Design Pack Options

USB-C

ACK_O IONS O INC UDE IN NE S
USBC SPI UPC0
USBC01 VR5V LOCAL NO
USBC_LAPTOP
PKGS SMALL_PITCH
USBCPC_SS CAP
ACTIVE_WEAKY:SMALL_PITCH_CAC _NI W_SRK
DUAL_KIS YES
USBC_GATE PACKAGE XSON
UPC1 ROM NO
UPC1 UART PD NO
LDCM ENABLED
ATC RTMR ROM WLCSP
ATC_BOUNDARYSCAN NO
SOC FORCE DFU YES
SOC_FORCE_DFU_YES XSON

Iceman VR

ACK_O IONS O INC UDE IN NE S
3V8 AON PBUS-18V
3V8 AON I2C-POR
3V8_INDUCTOR 1P5MM
3V8 AON MLCC-LN
3V8_AON LG_R YES
3V8_AON_CTRL_PKG QFN
3V8_AON_OA BGA

Wireless

ACK_O ONS O NC UDE IN NE IS
SUNWAY 1P5
WLBT D2R TP STATEN
WLBT_TP_0P5

Audio

ACK_O IONS O INC UDE N NE IS
SPKRAMP A
SPKRAMP B
SPKRAMP_C
SPKRAMP_D
SPKRAMP_E
SPKRAMP_F
SPKRAMP IOC GB
SPKR_CONN TINY

USB-C VRs

ACK_O IONS O INC UDE IN NE S
ATC VR PG-RES
ATC VR MLCC-DSCHG
ATC_VR_DSCHG-EN-R NO

Trackpad Interface

ACK_O ONS NC UDE IN NE IS
IPD_RESETS LS LVL SHIFTER
IPD_TOUCH C K SRC MLB BUF
IPD_PACK_MTP_FUNC1_FLEX:PULLUP

KBD Backlight

ACK_O IONS O INC UDE N NE IS
BLC_KBD_IND_HGT 1P4

PP3V3_S2 VR

ACK_O ONS O INC UDE N NE IS
3V3 S2 PBUS-18V
3V3 S2 MLCC-LN
3V3_S2 VOUT-B12

Charger & MagSafe

ACK_O IONS O INC UDE IN NE S
CHGR 72W
CHGR PBUS18V
CHGR MLCC-LN
UPC5_STRAP3 GND
BATT_CONN TINY

PP5V_S2 VR

ACK_O ONS O NC UDE IN NE IS
5V S2 MLCC-LN
5V S2 THINSTNCL

Display Backlight

ACK_O IONS O INC UDE N NE IS
BLC CBULK 0603
BLC FET OFF
BLC_IND 10UH
PANELPWR MINNIE
BLC_FERRITE YES
BLC_FUSE NO
BLC_RP8XX 0201

PMU

ACK_O IONS O INC UDE IN NE S
PMU 32K XOSC
PMU LDO2
PMU LDO10
PBUS SNS TLV9051
MPMU VSW2
PMU WLBT IPD 32K
PMU 32K WLBT

SOC

ACK_O ONS INC UDE N NE IS
ONE SIDED
PCIE GPO
LPDP INT RCAL
LPDPRX0 RCAL

San Diego & Disp

ACK_O IONS O INC UDE IN NE
PMIC SDG VGH ZRBCAP
PMIC SDG VBUCK3 IND LARGE
DISP CONN TINY

IMU

ACK_O IONS O VDC UDE N N S
REFIMU VDD LCFILT
REFIMU TEST NO

G DC Resistance Table

DC RESISTANCE FAI REQUIRED MEASUREMENTS			
ROM IN RE DES N)	O IN R DES N)	VA UE (MI IOHM)(O IONA)	O ERANCE (+) (O IONA)
LC320 2	SPEED:X1 ,X12,19,121,8 0,X12,49,E21	12 28	10%
LC320 2	SPEED:X1 ,X12,19,121,8 0,X12,49,E21	6 02	10%
JE701 29	. .. .	2 62	10%
JE701 30	. .. .	2 62	10%
JE 01 31	. .. .	2 62	10%
JE 01 32	. .. .	2 62	10%
JE700 29	. .. .	3 66	10%
JE700 30	. .. .	3 66	10%
JE700 31	. .. .	3 66	10%
JE700 32	. .. .	3 66	10%

SYNC DATE=

PAGE I LE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-09343

SIZE D

RE ISION 5.0.0

BRANCH dvt-1

PAGE 3 OF 801

SHEE 3 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC HE P SE OR AGREES O HE FOLLOWING I O MA N A N IS DOCUMEN N CONF DENCE
III NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR I ALL R GH S RESER ED

www.repairlap.com

A Mounting Holes

SH0400
TH-NSP
SL-3.41X2.0-5.91X4.5
998-19374

SH0401
4.6R2.0-NSP
998-25030

SH0403
4.6X5.2R1.7X2.3-NSP
998-11114

SH0402
5.0R2.0-NSP
998-25031

B MDB Cowling Bosses

SH0440
2 7X1.8R-1.4ID-1.26H-SM
860-01964

C MagSafe/USB-C Cowling Bosses

SH0450
2.7X1.8R-1.4ID-1.16H-SM
860-01916

SH0451
2.7X1.8R-1.4ID-1.16H-SM
860-01916

SH0452
2.7X1.8R-1.4ID-1.16H-SM
860-01916

SH0453
2.7X1.8R-1.4ID-1.16H-SM
860-01916

D WiFi Module Cowling Boss

SH0470
1.8X2.7R-1.64H-SM
860-01957

E Right Speaker Cowling Boss

SH0480
5 48X1.8R-2HOLE-1.38H-1
860-02822

F MLB Shield Fence

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-42305	1	FENCE,MLB,X2965	SHLD1	CRITICAL	

SH0430
TH-NSP
SL-0 5X1 28-1 25X2 03
998-21458

SH0432
TH-NSP
SL-0 5X1 28-1 25X2 03
998-21458

SH0436
TH-NSP
SL-0 5X1 28-1 25X2 03
998-21458

SH0431
TH-NSP
SL-0 5X1 28-1 25X2 03
998-21458

SH0433
TH-NSP
SL-0 5X1 28-1 25X2 03
998-21458

SH0437
TH-NSP
SL-0 5X1 28-1 25X2 03
998-21458

G SOC Thermal Module Bosses

SH0490
STDOFF-3.8X2.5R-1.32H-SM
860-02449

SH0491
STDOFF-3.8X2.5R-1.32H-SM
860-02449

SH0492
STDOFF-3.8X2.5R-1.32H-SM
860-02449

SH0493
STDOFF-3.8X2.5R-1.32H-SM
860-02449

H Antenna Cowling Bosses

SH04A0
2 44X2 448Q-1 151D-1 044H-SM
860-02043

SH04A1
2 44X2 448Q-1 151D-1 044H-SM
860-02043

I Spacers

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-31591	1	SPACER,MLB,ORIGIN,SMT,X2147	SH04B0		
806 31119	1	SPACER,MLB,SMT,X2147	SH04B1		
806-31120	1	SPACER,MLB,SMT,SML SLOT,X2147	SH04B2		
806-31121	1	SPACER,MLB,SMT,LRG SLOT,X2147	SH04B3		

J Keyboard Bracket

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-45003	1	BRKT,MLB,SMT,X2965	BRKT1	CRITICAL	

K MLB Bracket Slot

BRKT6
TH
SL-0 4X1 20
998-1681

BRKT7
TH
SL-0 4X1 20
998-1681

BOM_COST_GROUP=MECHANICALS

SYNC DATE=
PAGE TITLE
PD Parts

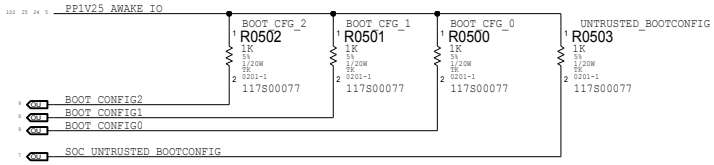
Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 4 OF 801
SHEET 4 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS PROVIDED BY THE FOLLOWING WRITTEN AGREEMENT THIS DOCUMENT CONTAINS CONFIDENCE INFORMATION. NO REPRODUCTION OR COPY IN WHOLE OR PART IS PERMITTED. ALL RIGHTS RESERVED

www.repairlap.com

A BOOT CONFIG ID

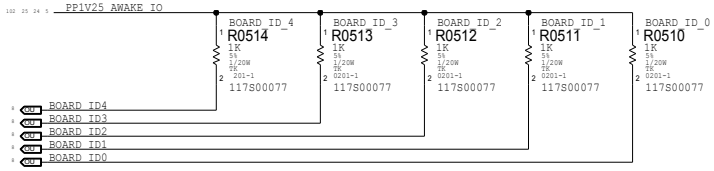


BOOT_CFG[2:0]	MODE V BUS FREQ USAGE
000	NAND, 1.2V SPI0, 12MHZ, PRODUCTION
001	NAND, 1.2V SPI0, 40MHZ, PRODUCTION
010	QUADNOR, 1.2V SPI1, 24MHZ, BACKUP PRODUCTION
011	RESERVED, 1.2V NA, NA, M ONLY
100	NOR, 1.2V SPI1, 6MHZ, BRINGUP
101	NOR, 1.2V SPI1, 12MHZ, MANUFACTURING/SIVAL
110	QUADNOR, 1.2V SPI1, 40MHZ, PRODUCTION
111	NOR, 1.2V SPI1, 40MHZ, LEGACY PRODUCTION

SOC BOOT AND POWER ARCH SPEC 1.0.4 TABLE 2.4

STUFF R0503 FOR UNTRUSTED_BOOTCONFIG

B BOARD ID

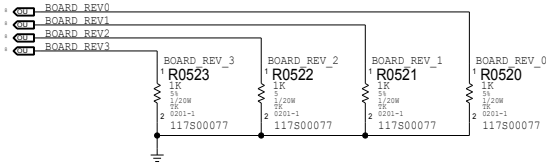


MLB BOARD_ID[7:0]:

BOARD_ID[7:5] COMES FROM SOC INTERNALLY

BOARD_ID[4:0] ARE THE STRAPS ON MLB, SAMPLED 100US AFTER COLD RESET DEASSERT

C BOARD REV



STUFFING RESISTOR MEANS BIT=0, START AT REV 0001 (match physical rev) AND COUNT UP TO 1111

0001: P1Bu
0010: Proto 1
0011: EVT1
0100: EVT2
0101: DVT
0110:
0111:
1000:
1001:
1010:
1011:
1100:
1101:
1110:
1111:

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: CONFIG STRAPS

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

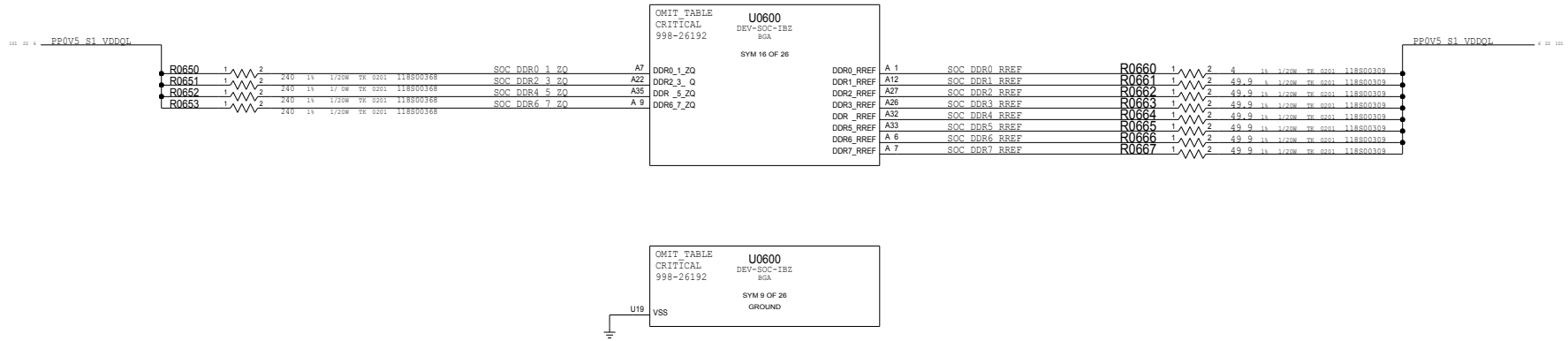
BRANCH dvt-1

PAGE 5 OF 801

SHEET 5 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE STATED HEREIN OR IN A WRITTEN AGREEMENT WITH APPLE INC. THE FOLLOWING INFORMATION IS APPLE INC. CONFIDENTIAL. DO NOT DUPLICATE OR REPRODUCE IN WHOLE OR IN PART. DO NOT DISCLOSE TO THIRD PARTIES. ALL RIGHTS RESERVED.

www.repairlap.com



PAGE TITLE

SOC: MISC

Apple Inc.

DRAWING NUMBER 051-09343

SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 6 OF 801

SHEET 6 OF 121

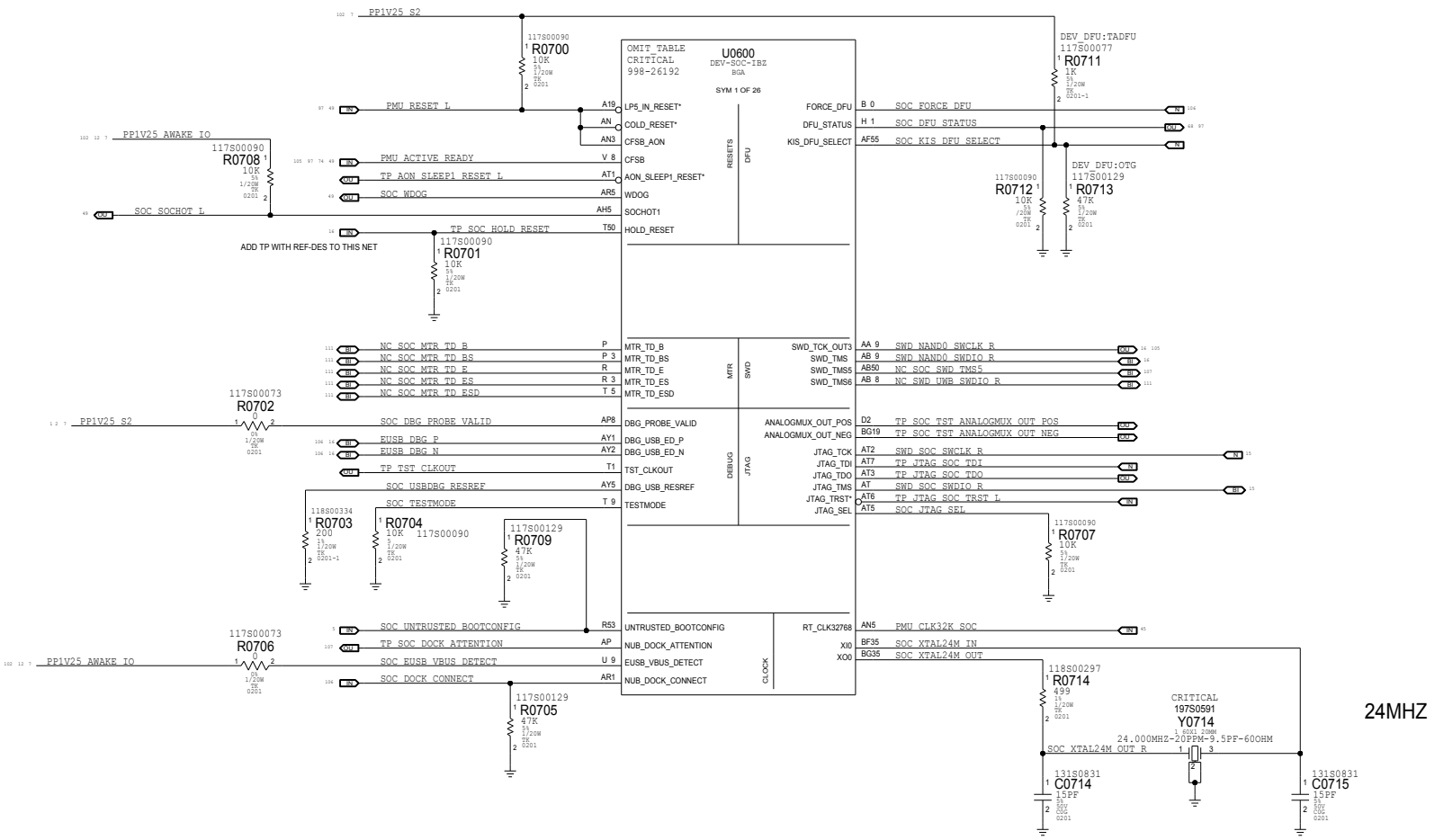
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING

1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
2. NOT TO REPRODUCE OR COPY IT
3. NOT TO RELEASE OR PUBLISH IT IN WHOLE OR PART

ALL RIGHTS RESERVED

www.repairlap.com



BOM_COST_GROUP=SOC

PAGE TITLE
SOC: RESETS,CLOCKS,DEBUG

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 7 OF 801

SHEET 7 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING
1. DO MAINTAIN THIS DOCUMENT IN CONFIDENCE
2. NOT REPRODUCE OR COPY
3. NOT DISCLOSE OR PUBLISH IN WHOLE OR PART
4. ALL RIGHTS RESERVED

www.repairlap.com

OMIT_TABLE
CRITICAL
998-26192

U0600
DEV-SOC-IBZ
BGA

SYM 8 OF 26

NC_PDM_DMIC_DATA2	AD7	AOP_SCM_IO[0]	AOP GPIO	NUB GPIO	NUB_CLK_OUT0	AM2	NC_SOC_NUB_CLK_OUT_0
NC_UWB_CS_L	AA7	AOP_SCM_IO[1]			NUB_CLK_OUT1	AM1	TP_SOC_NUB_CLK_OUT_1
NC_UWB_DUMP_TRIG	Y7	AOP_SCM_IO[2]					
NC_UWB_HOST_WAKE	Y6	AOP_SCM_IO[3]			NUB_SCM_IO[0]	AN1	NC_BKLT_PWR_ON
TP_AOP_LEAP_MADI_IN	AA6	AOP_SCM_IO[ ]			NUB_SCM_IO[1]	AK5	CODEC_RESET_L
TP_AOP_LEAP_MADI_OUT	AB6	AOP_SCM_IO[5]			NUB_SCM_IO[2]	AL7	NC_SOC_NUB_GPIO_2
SPI_GYRO_CS_L	AB8	AOP_SCM_IO[6]			NUB_SCM_IO[3]	AM7	NC_SOC_NUB_GPIO_3
GYRO_INT	AC7	AOP_SCM_IO[7]			NUB_SCM_IO[ ]	AL6	NC_SOC_NUB_GPIO_4
GYRO_MOTION_INT	AC6	AOP_SCM_IO[8]			NUB_SCM_IO[5]	AK	NC_SOC_NUB_GPIO_5
NC_HDMI_CEC_AOP_TX	AB7	AOP_SCM_IO[9]			NUB_SCM_IO[6]	AK3	CHGR_INT_L
NC_HDMI_CEC_AOP_RX	Y5	AOP_SCM_IO[10]			NUB_SCM_IO[7]	AM5	SMC_FIXTURE_MODE_L
ALS_INT_L	W6	AOP_SCM_IO[11]			NUB_SCM_IO[8]	AK2	SOC_SW_DBG
NC_SPI_DP2HDMI_HOLD_L	Y	AOP_SCM_IO[2]			NUB_SCM_IO[9]	AL3	NC_ENET_LOW_PWR
SPI_LAS_CS_L	AA	AOP_SCM_IO[3]			NUB_SCM_IO[10]	AK6	NC_SOC_NUB_GPIO_10
NC_HDMI_HDP_AOP	AA5	AOP_SCM_IO[1]			NUB_SCM_IO[11]	AM	IPD_SYS_AWAKE
NC_SOC_AOP_GPIO_15	AA3	AOP_SCM_IO[15]			NUB_SCM_IO[12]	AL	NC_SOC_NUB_GPIO_12
					NUB_SCM_IO[13]	AL1	TOUCHID_PWR_EN
					NUB_SCM_IO[1]	AK1	NC_SOC_NUB_GPIO_14
					NUB_SCM_IO[15]	AM3	NC_SOC_NUB_GPIO_15
I2C_AOP_ALS_SCL	AD5	AOP_I2CM0_SCL	AOP I2C				
I2C_AOP_ALS_SDA	AD1	AOP_I2CM0_SDA					
NC_SOC_AOP_I2CM1_SCL	AD2	AOP_I2CM _SCL		NUB SPMI	NUB_SPMI0_SCLK	AP1	SPMI_NUB_MPMU_CLK_R
NC_SOC_AOP_I2CM1_SDA	AE1	AOP_I2CM _SDA			NUB_SPMI0_SDATA	AN2	SPMI_NUB_MPMU_DATA_R
NC_SOC_AOP_I2CM2_SCL	AD3	AOP_I2CM2_SCL			NUB_SPMI1_SCLK	AR	SPMI_NUB_SPMU_CLK_R
NC_SOC_AOP_I2CM2_SDA	AD	AOP_I2CM2_SDA			NUB_SPMI1_SDATA	AP3	SPMI_NUB_SPMU_DATA_R
					NUB_SPMI2_SCLK	AR3	NC_SOC_NUB_SPMI2_SCLK
					NUB_SPMI2_SDATA	AR2	NC_SOC_NUB_SPMI2_SDATA
NC_AOP_I2S0_BCLK	AB3	AOP_I2S0_BCLK	AOP I2S				
NC_AOP_I2S0_DIN	AC5	AOP_I2S0_DIN					
NC_AOP_I2S0_DOUT	AB	AOP_I2S0_DOUT					
NC_AOP_I2S0_LRCLK	AA1	AOP_I2S0_LRCK					
NC_AOP_I2S0_MCK	AA2	AOP_I2S _MCK					
PDM_DMIC_CLK5_R	AB1	AOP_I2S _BCLK		NUB SWD	NUB_SWD_TCK_OUT0	AR7	SWD_NUB_PMU_SWCLK_R
PDM_DMIC_DATA1	AC2	AOP_I2S1_DIN			NUB_SWD_TCK_OUT1	AP7	SWD_IPD_SWCLK_R
PDM_DMIC_CLK6_R	AC	AOP_I2S1_DOUT			NUB_SWD_TCK_OUT2	AR6	SWD_NUB_ATCRTMR_SWCLK_R
NC_PDM_DMIC_CLK7_R	AC3	AOP_I2S1_LRCK			NUB_SWD_TMS0	AN7	SWD_NUB_PMU_SWDIO_R
PDM_DMIC_DATA0	AC1	AOP_I2S1_MCK			NUB_SWD_TMS1	AM6	SWD_IPD_SWDIO_R
					NUB_SWD_TMS2	AP6	SWD_NUB_ATCRTMR_SWDIO_R
					NUB_SWD_TMS3	AN6	NC_SOC_NUB_SWD_TMS3
SPI_AOP_GYRO_MISO	W1	AOP_SP 0_MISO	AOP SPI	SMC I2C	SMC_I2CM0_SCL	AJ5	SPMI_NUB_UPC015_CLK_R
SPI_AOP_GYRO_MOSI_R	Y3	AOP_SP 0_MOSI			SMC_I2CM0_SDA	AH6	SPMI_NUB_UPC015_DATA_R
SPI_AOP_GYRO_CLK_R	W	AOP_SP _SCLK			SMC_I2CM1_SCL	AG1	I2C_SMC_PWR_SCL
SPI_AOP_SENSORS_MISO	Y2	AOP_SPI1_MISO			SMC_I2CM1_SDA	AG2	I2C_SMC_PWR_SDA
SPI_AOP_SENSORS_MOSI_R	W3	AOP_SPI1_MOSI			SMC_I2CM2_SCL	AG6	I2C_SMC_SNS1_SCL
SPI_AOP_SENSORS_CLK_R	Y1	AOP_SPI1_SCLK			SMC_I2CM2_SDA	AG	I2C_SMC_SNS1_SDA
					SMC_I2CM3_SCL	AG7	I2C_SMC_IPD_SCL
					SMC_I2CM3_SDA	AG5	I2C_SMC_IPD_SDA
					SMC_I2CM _SCL	AG3	NC_I2C_SMC_SNS0_SCL
					SMC_I2CM _SDA	F7	NC_I2C_SMC_SNS0_SDA
SPMI_AOP_WLBT_CLK_R	AE6	AOP_SPMI0_SCLK	AOP SPMI				
SPMI_AOP_WLBT_DATA_R	AE7	AOP_SPMI0_SDATA					
SPMI_AOP_SE_CLK_R	AD6	AOP_SPMI1_SCLK					
SPMI_AOP_SE_DATA_R	AF1	AOP_SPMI1_SDATA					
NC_SOC_AOP_UART0_RXD	AF3	AOP_UART0_RXD	AOP UART	SMC	SMC_UART0_RXD	A	TP_SOC_UART_SMC_DEBUGPRT_D2R
NC_SOC_AOP_UART0_TXD	AF5	AOP_UART0_TXD			SMC_UART0_TXD	AJ	TP_SOC_UART_SMC_DEBUGPRT_R2D
NC_SOC_AOP_UART1_RXD	AE	AOP_UART1_RXD		SMC GPIO	SMC_GP O0	AH7	NC_UPC_SMC_I2C_INT_L
NC_SOC_AOP_UART1_TXD	AE3	AOP_UART1_TXD			SMC_GP O1	AJ1	NC_SOC_SMC_GPIO_1
NC_SOC_AOP_UART2_RXD	AF2	AOP_UART2_RXD					
NC_SOC_AOP_UART2_TXD	AF	AOP_UART2_TXD					
DMIC_DISABLE_L	AF6	MIC_DISABLE		SMC FPWM	SMC_FPWM0	AJ3	NC_SMC_FAN_0_PWM
DMIC_WARN_L	AF8	MIC_DISABL _WARN*			SMC_FPWM1	AH3	NC_SMC_FAN_0_TACH
					SMC_FPWM2	AH1	NC_SMC_FAN_1_PWM
					SMC_FPWM3	A 2	NC_SMC_FAN_1_TACH

OMIT_TABLE
CRITICAL
998-26192

U0600
DEV-SOC-IBZ
BGA

SYM 3 OF 26

NC_UPC_I2C_INT_L	G 1	GPIO[0]	GPIO	UART0_RXD	AF 8	UART_DEBUGPRT_D2R
NC_SOC_AP_GPIO_1	AJ 9	GPIO[1]		UART0_TXD	AG 9	UART_DEBUGPRT_R2D
NC_SOC_AP_GPIO_2	AH50	GPIO[2]		UART _CTS*	N55	NC_SOC_AP_UART1_CTS_L
NC_SOC_AP_GPIO_3	AJ50	GPIO[3]		UAR 1_RTS*	M55	NC_SOC_AP_UART1_RTS_L
SPKRAMP_RESET_L	F39	GPIO[ ]		UAR 1_RXD	R55	NC_SOC_AP_UART1_RXD
SPKRAMP_INT_L	E 0	GPIO[5]		UART1_TXD	T55	NC_SOC_AP_UART1_TXD
CODEC_INT_L	V53	GPIO[6]				
SWD_UPC_SWCLK_R	Y53	GPIO[7]		UART2_CTS*	R5	NC_SOC_AP_UART2_CTS_L
SWD_UPC_SWDIO0_R	W53	GPIO[8]		UART2_RTS*	M5	NC_SOC_AP_UART2_RTS_L
NC_SWD_UPC_SWDIO1_R	V52	GPIO[9]		UART2_RXD	P5	NC_SOC_AP_UART2_RXD
NC_CCG_I2C_INT	W52	GPIO[10]		UART2_TXD	P55	NC_SOC_AP_UART2_TXD
BOARD_REV0	V51	GPIO[11]				
BOARD_REV1	V50	GPIO[12]		UART3_CTS*	Y5	NC_SOC_AP_UART3_CTS_L
BOARD_REV2	D 1	GPIO[13]		UART3_RTS*	Y55	NC_SOC_AP_UART3_RTS_L
BOARD_REV3	D39	GPIO[1]		UART3_RXD	AA55	NC_SOC_AP_UART3_RXD
NC_SD_PRSNT_L_DMIC_ID	V8	GPIO[15]		UART3_TXD	AB55	NC_SOC_AP_UART3_TXD
UPC0_SOC_DFU_BOOTED_L	T53	GPIO[16]		UART _RXD	AA53	NC_SOC_AP_UART4_RXD
NC_SOC_AP_GPIO_17	U53	GPIO[17]		UART _TXD	AA5	NC_SOC_AP_UART4_TXD
NC_SOC_AP_GPIO_18	T52	GPIO[18]				
NC_SOC_AP_GPIO_19	U52	GPIO[19]		UART5_RXD	AB52	UART_TCON_D2R
NC_SOC_AP_GPIO_20	R52	GPIO[20]		UART5_TXD	AB53	NC_UART_TCON_R2D
TOUCHID_INT	U50	GPIO[21]				
NC_SOC_AP_GPIO_22	U51	GPIO[22]		UART6_RXD	AK 8	NC_UART_HDMI_D2R
NC_SOC_AP_GPIO_23	W50	GPIO[23]		UART6_TXD	AK 9	NC_UART_HDMI_R2D
NC_SOC_AP_GPIO_24	V 9	GPIO[2]				
NC_SOC_AP_GPIO_25	B 1	GPIO[25]				
NC_SOC_AP_GPIO_26	C39	GPIO[26]				
BOARD_ID0	W55	BOARD_ID0	BOARD ID	NAND_SYS_CLK0	AH51	NAND0_CLK24M0_R
BOARD_ID1	V55	BOARD_ID1		NAND_SYS_CLK1	AG51	NAND0_CLK24M1_R
BOARD_ID2	V5	BOARD_ID2				
BOARD_ID3	U55	BOARD_ID3		SSD_BFH	AH 9	NAND_BFH
BOARD_ID	U5	BOARD_ID		SSD_RESET0*	AH52	NAND_RESET0_L
				SSD_RESET1*	AG52	NAND_RESET1_L
IPD_TOUCH_INT_L	AV6	MTP_FUNC0	MTP	MTP_I2C0_SCL	AU6	NC_SOC_MTP_I2C0_SCL
NC_SOC_MTP_FUNC_1	AU	MTP_FUNC1		MTP_I2C0_SDA	AU3	NC_SOC_MTP_I2C0_SDA
NC_SOC_MTP_FUNC_2	AU1	MTP_FUNC2				
SPI_IPD_MCU_CS_L	AV5	MTP_FUNC3		MTP_SPI0_MISO	AV3	SPI_IPD_MISO
SPI_IPD_TOUCH_CS_L	AV2	MTP_FUNC		MTP_SPI0_MOSI	AV	SPI_IPD_MOSI_R
IPD_MCU_INT_L	AU7	MTP_FUNC5		MTP_SPI0_SCLK	AV1	SPI_IPD_CLK_R
NC_SOC_MTP_FUNC_6	AV8	MTP_FUNC6				
NC_SOC_MTP_FUNC_7	AV7	MTP_FUNC7				

BOM_COST_GROUP=SOC

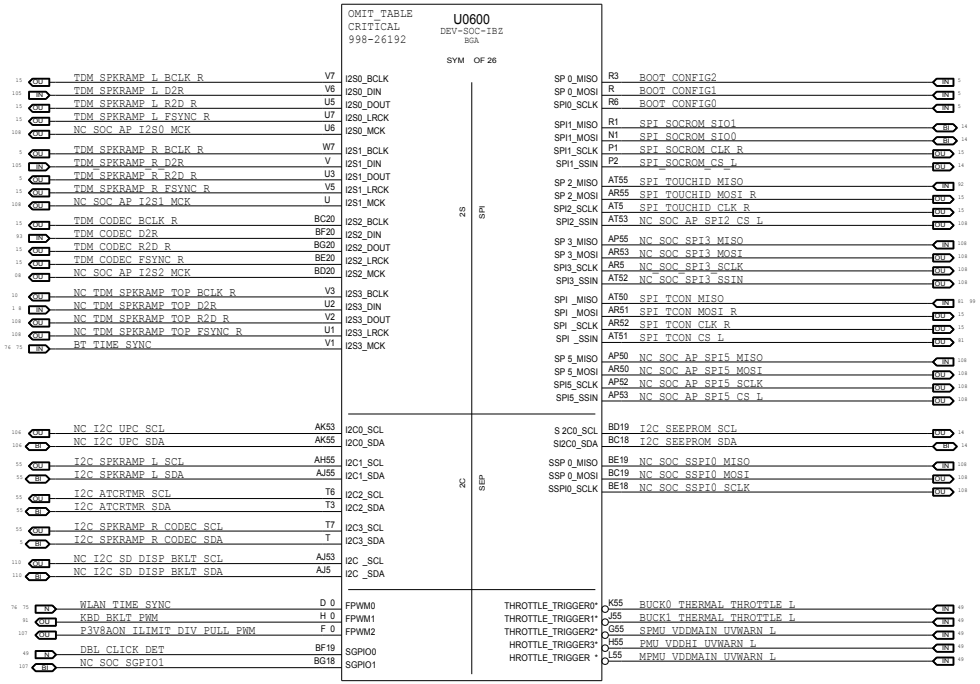
PAGE TITLE
SOC: GPIOS,NAND,MTP,UART

Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 8 OF 801
SHEET 8 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING
THIS DOCUMENT CONFIDENTIAL
NO REPRODUCE OR COPY
NO REVEAL PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com



BOM_COST_GROUP=SOC

PAGE TITLE
SOC: I2S,I2C,SPI,THROT,CFG

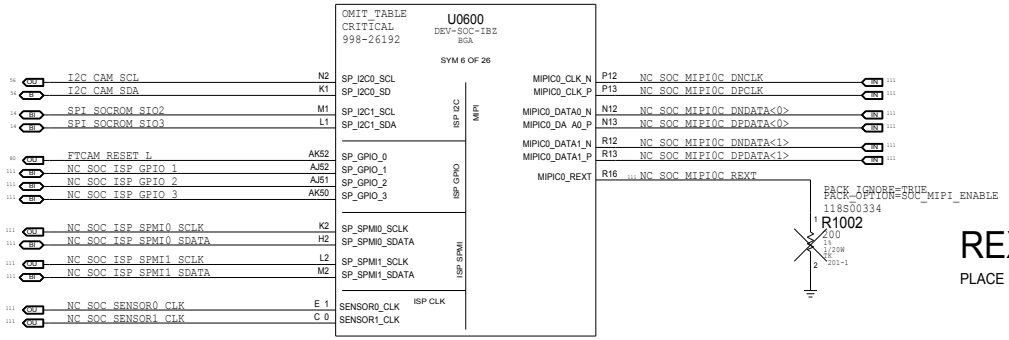
Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 9 OF 801
SHEET 9 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. THE PARTIES OF AGREES TO THE FOLLOWING
1. OMAN AN IS DOCUMENT CONFIDENCE
II NO REPRODUCE OR COPY
III NO OREAL PUBLISH IN WHOLE OR PART
I ALL RIGHTS RESERVED

www.repairlap.com

ISP / MIPI



REXT

PLACE NEAR SOC BALL

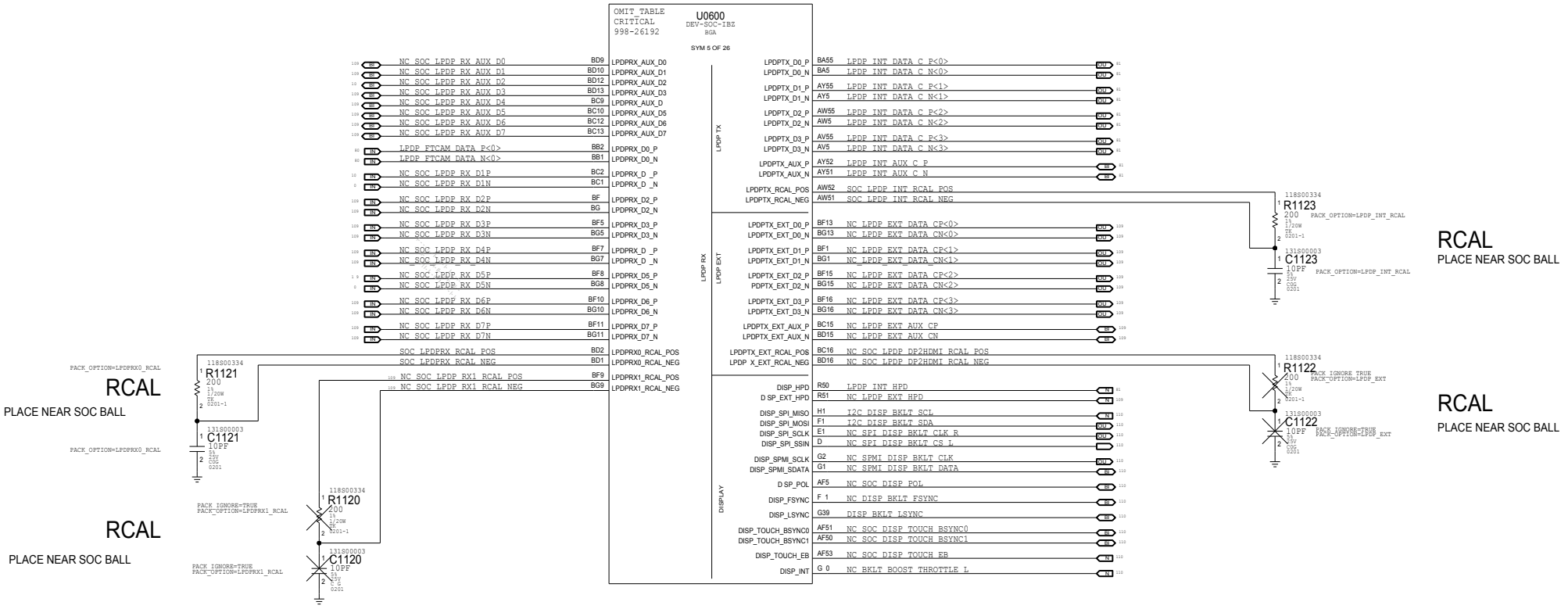
BOM_COST_GROUP=SOC

PAGE TITLE	SOC: ISP, MIPI
Apple Inc.	DRAWING NUMBER 051-09343
	SIZE D
	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 10 OF 801
	SHEET 10 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. THE PARTIES OF AGREES TO THE FOLLOWING: (1) MAINTAIN IS DOCUMENT IN CONFIDENCE (2) NOT REPRODUCE OR COPY (3) NOT REPUBLISH IN WHOLE OR PART. ALL RIGHTS RESERVED.

www.repairlap.com

LPDP



SOC: LPDP

Apple Inc.

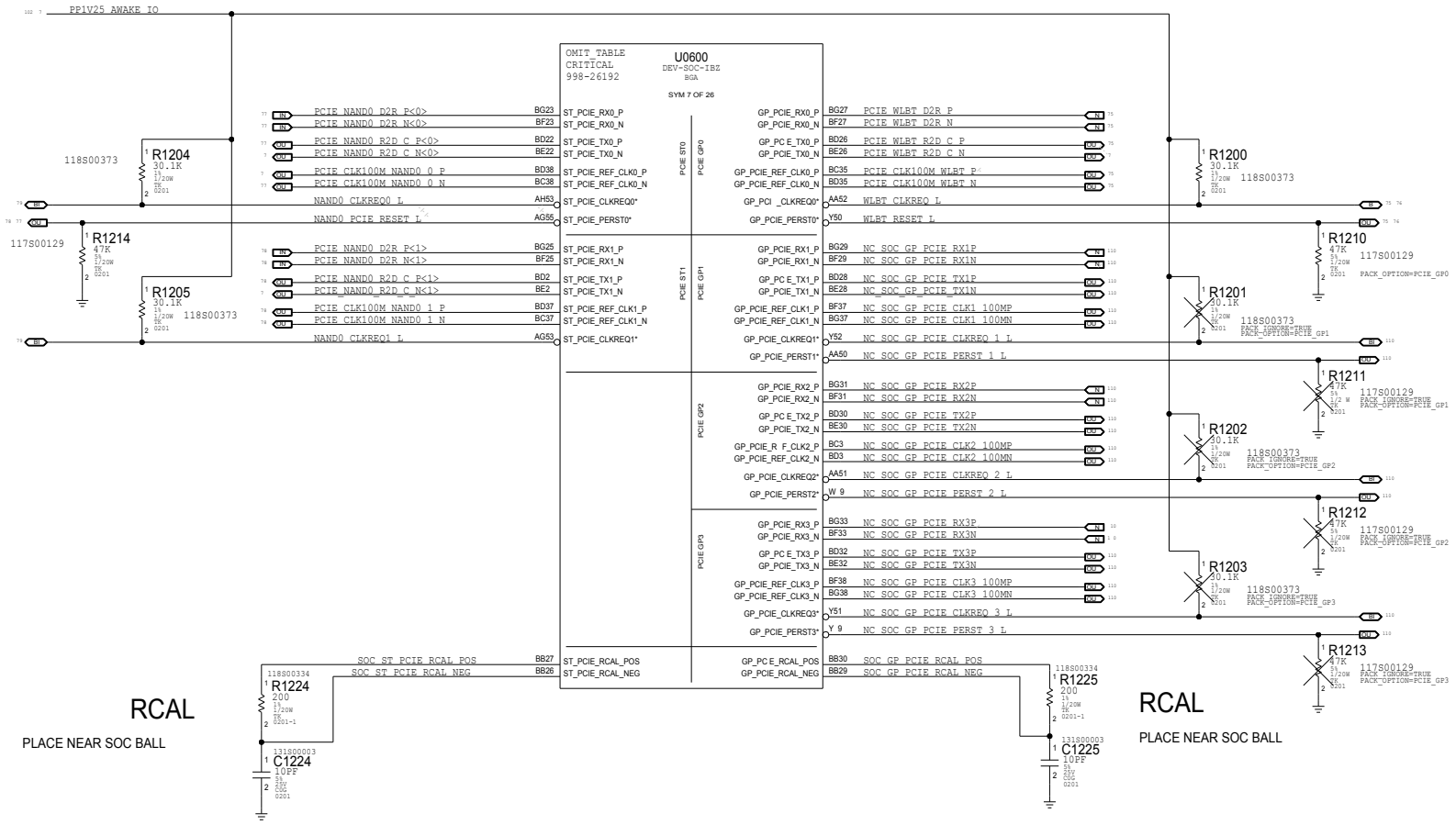
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO IN THE FOLLOWING WRITTEN DOCUMENT, THIS DOCUMENT CONTAINS CONFIDENTIAL INFORMATION. NO PART OF THIS DOCUMENT MAY BE REPRODUCED OR COPIED IN WHOLE OR PART. ALL RIGHTS RESERVED.

DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	11 OF 801
SHEET	11 OF 121

www.repairlap.com

PCIE

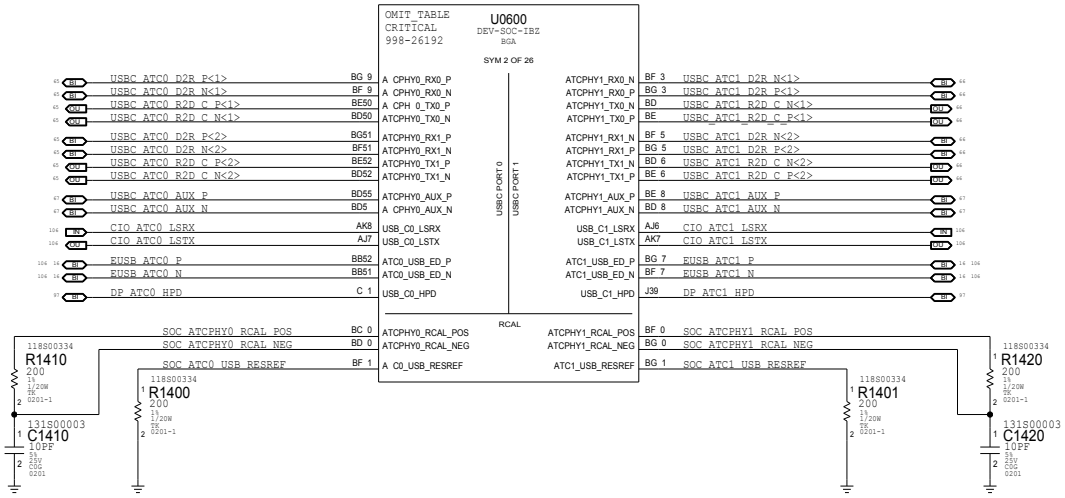


PAGE TITLE	SOC: PCIE
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 12 OF 801
	SHEET 12 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO THE FOLLOWING
1. OMIT ANY INFORMATION DOCUMENTS CONFIDENCE
2. NOT TO REPRODUCE OR COPY
3. NOT TO RELEASE, PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

CIO



RCAL

PLACE NEAR SOC BALL

RCAL

PLACE NEAR SOC BALL

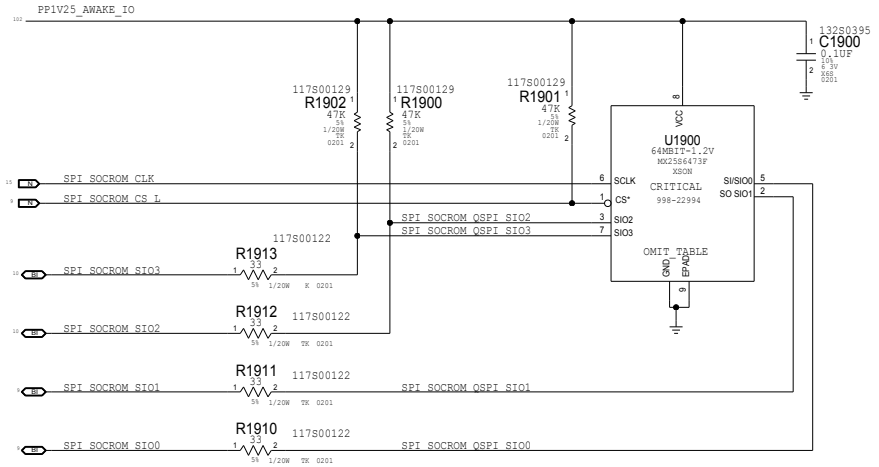
BOM_COST_GROUP=SOC

PAGE TITLE	SOC: CIO
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 14 OF 801
	SHEET 13 OF 121

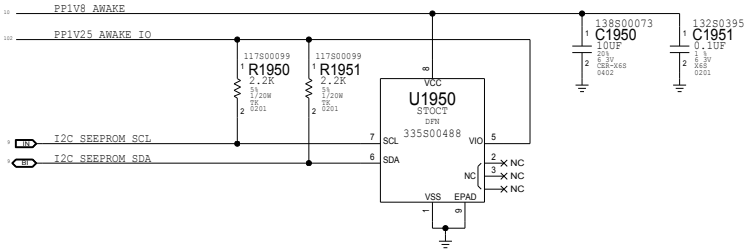
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING
1. TO MAINTAIN IS DOCUMENT IN CONFIDENCE
2. NOT TO REPRODUCE OR COPY
3. NOT TO REVEAL PUBLISH IN WHOLE OR PART
4. ALL RIGHTS RESERVED

www.repairlap.com

A SPI ROM



B SEP EEPROM



BOM_COST_GROUP=SOC

PAGE TITLE	SOC: SPI NOR, SEP ROM
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 19 OF 801
	SHEET 14 OF 121

www.repairlap.com

A SOC ROM Source Terminations

R2000 — SPI_SOCROM_CLK_R → SPI_SOCROM_CLK, 20, 118S00467, PLACE_NEAR=U0600.P1:10MM

B TOUCHID Source Terminations

R2004 — SPI_TOUCHID_MOSI_R → SPI_TOUCHID_MOSI, 20, 118S00467, PLACE_NEAR=U0600.AR55:10MM

R2005 — SPI_TOUCHID_CLK_R → SPI_TOUCHID_CLK, 20, 118S00467, PLACE_NEAR=U0600.AT5 :10MM

C IPD Source Terminations

R2006 — SPI_IPD_MOSI_R → SPI_IPD_MOSI, 20, 118S00467, PLACE_NEAR=U0600.AV :10MM

R2007 — SPI_IPD_CLK_R → SPI_IPD_CLK, 20, 118S00467, PLACE_NEAR=U0600.AV1 10MM

D TCON Source Terminations

R2090 — SPI_TCON_MOSI_R → SPI_TCON_MOSI, 20, 118S00467, PLACE_NEAR=U0600.AR51:10MM

R2091 — SPI_TCON_CLK_R → SPI_TCON_CLK, 20, 118S00467, PLACE_NEAR=U0600.AR52:10MM

E IMU Source Terminations

R2008 — SENSOR_IMU — SPI_AOP_GYRO_MOSI_R → SPI_AOP_GYRO_MOSI, 20, 118S00467, PLACE_NEAR=U0600.Y3:10MM

R2009 — SENSOR_IMU — SPI_AOP_GYRO_CLK_R → SPI_AOP_GYRO_CLK, 20, 118S00467, PLACE_NEAR=U0600.W :10MM

F SOC SWD Source Terminations

R2084 — SWD_SOC_SWCLK_R → SWD_SOC_SWCLK, 20, 118S00467, PLACE_NEAR=U0600.AT2:10MM

R2085 — SWD_SOC_SWDIO_R → SWD_SOC_SWDIO, 20, 118S00467, PLACE_NEAR=U0600.AT :10MM

G SOC SPMI MPMU Source Terminations

R2060 — SPMI_NUB_MPMU_CLK_R → SPMI_NUB_MPMU_CLK, 33, 118S00377, PLACE_NEAR=U0600.AP1:10MM

R2061 — SPMI_NUB_MPMU_DATA_R → SPMI_NUB_MPMU_DATA, 33, 118S00377, PLACE_NEAR=U0600.AN2:10MM

H SOC SPMI SPMU Source Terminations

R2062 — SPMI_NUB_SPMU_CLK_R → SPMI_NUB_SPMU_CLK, 33, 118S00377, PLACE_NEAR=U0600.AR :10MM

R2063 — SPMI_NUB_SPMU_DATA_R → SPMI_NUB_SPMU_DATA, 33, 118S00377, PLACE_NEAR=U0600.AP3:10MM

I PMU SWD Series R

R2072 — SWD_NUB_PMU_SWCLK_R → SWD_NUB_PMU_SWCLK, 15, 118S00465, PLACE_NEAR=U0600.AR7:10MM

R2070 — SWD_NUB_SWCLK_SPMU, 49.9, 118S00309, PLACE_NEAR=R2071.1:10MM

R2071 — SWD_NUB_SWCLK_MPMU, 49.9, 118S00309, PLACE_NEAR=R2070. :10MM

R2075 — SWD_NUB_PMU_SWDIO_R → SWD_NUB_PMU_SWDIO, 15, 118S00465, PLACE_NEAR=U0600.AN7:10MM

R2073 — SWD_NUB_SWDIO_SPMU, 49.9, 118S00309, PLACE_NEAR=R207 .1:10MM

R2074 — SWD_NUB_SWDIO_MPMU, 49.9, 118S00309, PLACE_NEAR R2073.1:10MM

J LAS Source Terminations

R2080 — SPI_AOP_SENSORS_CLK_R → SPI_AOP_SENSORS_CLK, 20, 118S00467, PLACE_NEAR=U0600.Y1:10MM

R2081 — SPI_AOP_SENSORS_MOSI_R → SPI_AOP_SENSORS_MOSI, 20, 118S00467, PLACE_NEAR=U0600.W3:10MM

K UPC 015 SPMI Terminations

R20A3 — SPMI_NUB_UPC015_CLK_R → SPMI_NUB_UPC015_CLK, 33, 118S00377, PLACE_NEAR=U0600.AR3 10MM

R20B0 — 117S00096, 1M

R20A0 — SPMI_NUB_UPC0_CLK, 10, 118S00311, PLACE_NEAR=R20A1.1:10MM

R20A1 — SPMI_NUB_UPC1_CLK, 10, 118S00311, PLACE_NEAR=R20A0.1:10MM

R20A2 — SPMI_NUB_UPC5_CLK, 10, 118S00311, PLACE_NEAR=R20A0.1:10MM

R20A7 — SPMI_NUB_UPC015_DATA_R → SPMI_NUB_UPC015_DATA, 33, 118S00377, PLACE_NEAR=U0600.AR2:10MM

R20B1 — 117S00096, 1M

R20A4 — SPMI_NUB_UPC0_DATA, 28, 118S00619, PLACE_NEAR=UF 00.N25 10MM

R20A5 — SPMI_NUB_UPC1_DATA, 28, 118S00619, PLACE_NEAR=UF500.N25:10MM

R20A6 — SPMI_NUB_UPC5_DATA, 28, 118S00619, PLACE_NEAR=U5500.N25:10MM

L TDM Source Terminations

R2010 — TDM_SPKRAMP_L_BCLK_R → TDM_SPKRAMP_L_BCLK, 20, 118S00467, PLACE_NEAR=U0600.V7:10MM

R2011 — TDM_SPKRAMP_L_R2D_R → TDM_SPKRAMP_L_R2D, 20, 118S00467, PLACE_NEAR=U0600 U5:10MM

R2012 — TDM_SPKRAMP_L_FSYNC_R → TDM_SPKRAMP_L_FSYNC, 20, 118S00467, PLACE_NEAR=U0600 U7:10MM

R2020 — TDM_SPKRAMP_R_BCLK_R → TDM_SPKRAMP_R_BCLK, 20, 118S00467, PLACE_NEAR=U0600.W7 10MM

R2021 — TDM_SPKRAMP_R_R2D_R → TDM_SPKRAMP_R_R2D, 20, 118S00467, PLACE_NEAR=U0600 U3:10MM

R2022 — TDM_SPKRAMP_R_FSYNC_R → TDM_SPKRAMP_R_FSYNC, 20, 118S00467, PLACE_NEAR=U0600.V5:10MM

R2030 — TDM_CODEC_BCLK_R → TDM_CODEC_BCLK, 20, 118S00467, PLACE_NEAR=U0600.BC20 10MM

R2031 — TDM_CODEC_R2D_R → TDM_CODEC_R2D, 20, 118S00467, PLACE_NEAR=U0600 BG20:10MM

R2032 — TDM_CODEC_FSYNC_R → TDM_CODEC_FSYNC, 20, 118S00467, PLACE_NEAR=U0600.BE20:10MM

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: SOURCE TERMS

Apple Inc.

DRAWING NUMBER: 051-09343 | SIZE: D

REVISION: 5.0.0

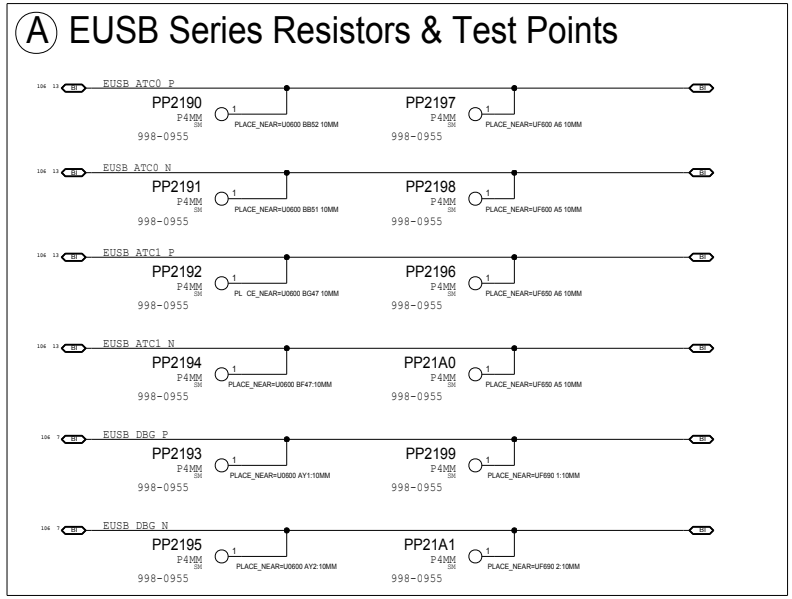
BRANCH: dvt-1

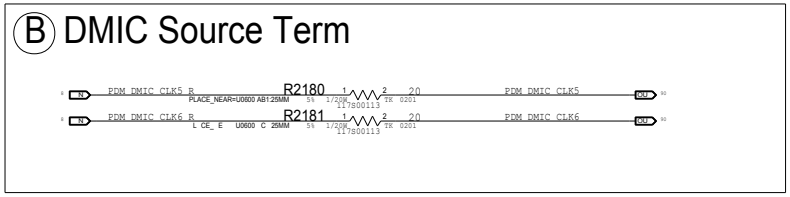
PAGE: 20 OF 801

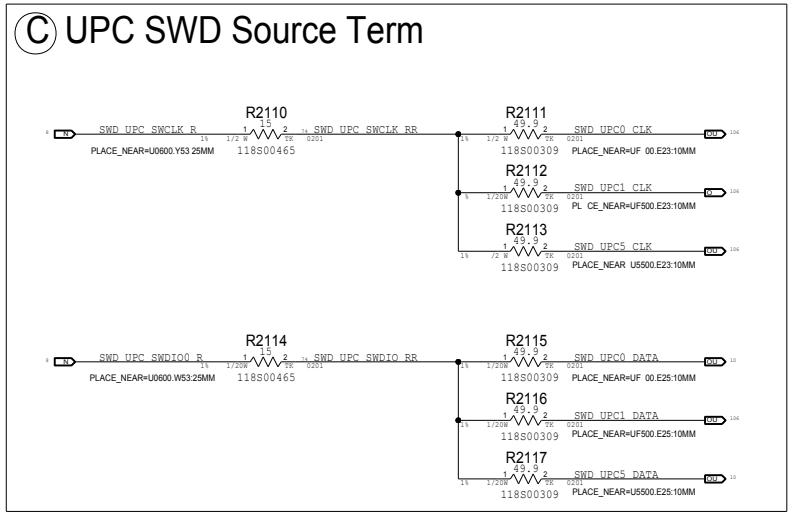
SHEET: 15 OF 121

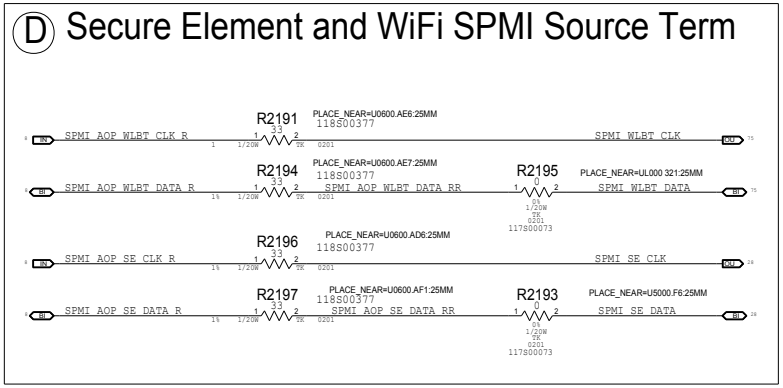
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: THIS DOCUMENT CONFIDENTIAL. NO REPRODUCE OR COPY. NO DISCLOSE OR PUBLISH IN WHOLE OR PART. ALL RIGHTS RESERVED.

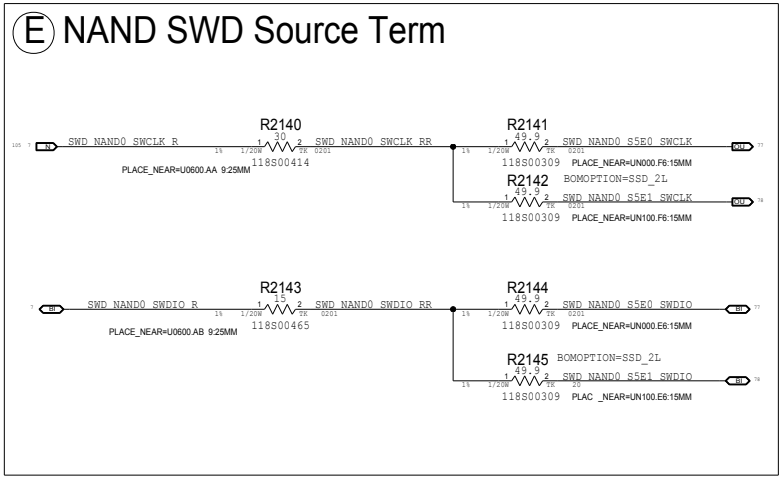
www.repairlap.com

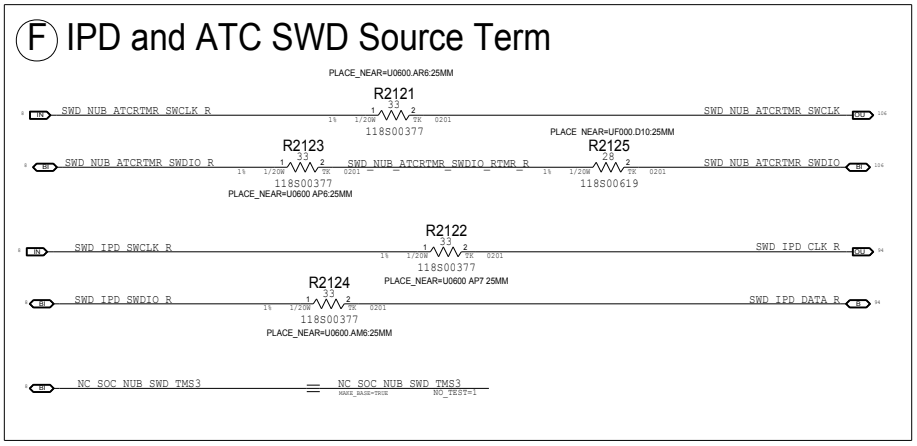


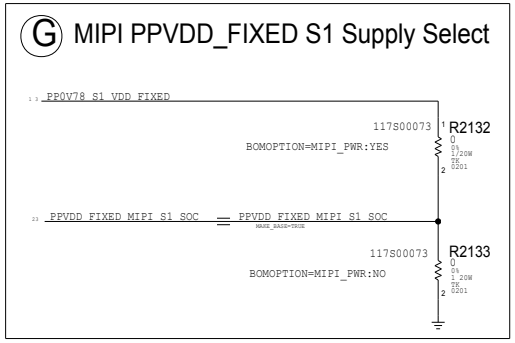


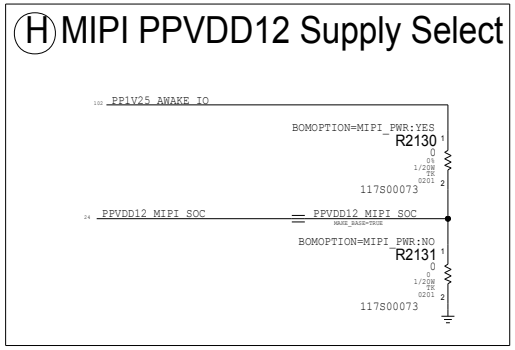


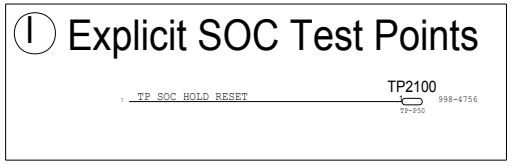


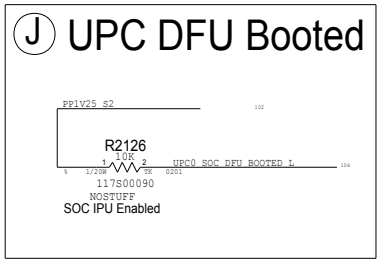












PAGE TITLE
SOC: SOURCE TERMS

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (1) MAINTAIN CONFIDENTIALITY; (2) NO REPRODUCTION OR COPYING; (3) NO DISCLOSURE; (4) ALL RIGHTS RESERVED

DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	21 OF 801
SHEET	16 OF 121

www.repairlap.com

C2200 2200PF	C2209 2200PF	C2212 2200PF	C221B 2200PF	C2224 2200PF	C2233 2200PF	C223C 2200PF	C2245 2200PF	C224E 2200PF	C2257 2200PF	C2260 2200PF	C2268 2200PF
C2201 2200PF	C220A 2200PF	C2213 2200PF	C221C 2200PF	C2225 2200PF	C2234 2200PF	C223D 2200PF	C2246 2200PF	C224F 2200PF	C2258 2200PF	C2261 2200PF	C2269 2200PF
C2202 2200PF	C220B 2200PF	C2214 2200PF	C221D 2200PF	C2226 2200PF	C2235 2200PF	C223E 2200PF	C2247 2200PF	C2250 2200PF	C2259 2200PF	C2262 2200PF	C226A 2200PF
C2203 2200PF	C220C 2200PF	C2215 2200PF	C221E 2200PF	C2227 2200PF	C2236 2200PF	C223F 2200PF	C2248 2200PF	C2251 2200PF	C225A 2200PF	C2263 2200PF	C226B 2200PF
C2204 2200PF	C220D 2200PF	C2216 2200PF	C221F 2200PF	C2228 2200PF	C2237 2200PF	C2240 2200PF		C2252 2200PF	C225B 2200PF	C2264 2200PF	C226C 2200PF
C2205 2200PF	C220E 2200PF	C2217 2200PF	C2220 2200PF	C2229 2200PF	C2238 2200PF	C2241 2200PF	C224A 2200PF	C2253 2200PF	C225C 2200PF	C2265 2200PF	C226D 2200PF
C2206 2200PF	C220F 2200PF	C2218 2200PF	C2221 2200PF	C2230 2200PF	C2239 2200PF	C2242 2200PF	C224B 2200PF	C2254 2200PF	C225D 2200PF	C2266 2200PF	C226E 2200PF
C2207 2200PF	C2210 2200PF	C2219 2200PF	C2222 2200PF	C2231 2200PF	C223A 2200PF	C2243 2200PF	C224C 2200PF	C2255 2200PF	C225E 2200PF	C2267 2200PF	C226F 2200PF
C2208 2200PF	C2211 2200PF	C221A 2200PF	C2223 2200PF	C2232 2200PF	C223B 2200PF	C2244 2200PF	C224D 2200PF	C2256 2200PF	C225F 2200PF	C2270 2200PF	C2271 2200PF
C2272 2200PF	C2273 2200PF	C2274 2200PF									

SYNC DATE=12/12/2022

PAGE TITLE

SOC: DUMMY DAM

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

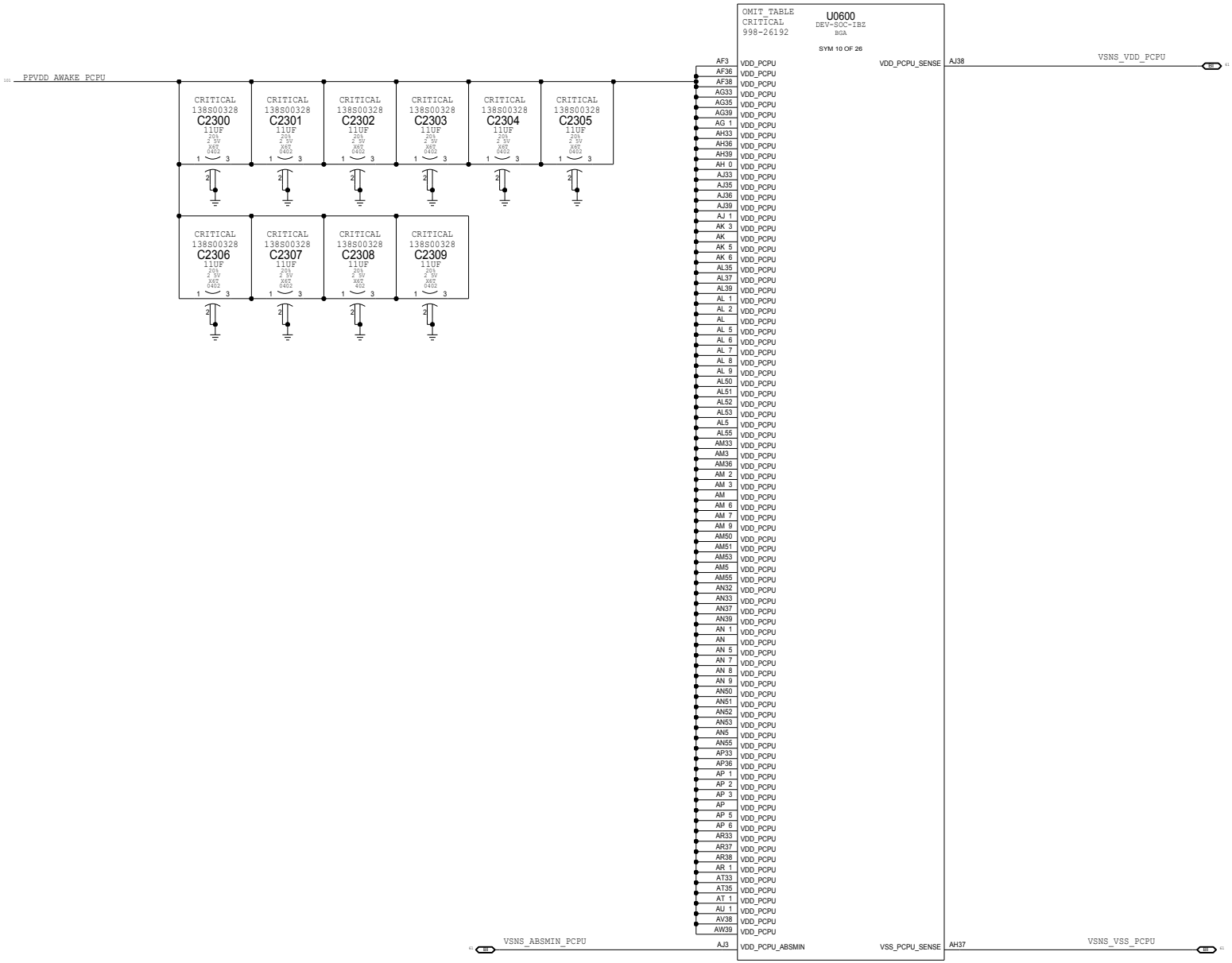
BRANCH dvt-1

PAGE 22 OF 801

SHEET 17 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: THIS DOCUMENT CONFIDENTIAL. NO REPRODUCE OR COPY. NO OTHER USE, PUBLISH IN WHOLE OR PART. ALL RIGHTS RESERVED

www.repairlap.com



BOM_COST_GROUP=SOC

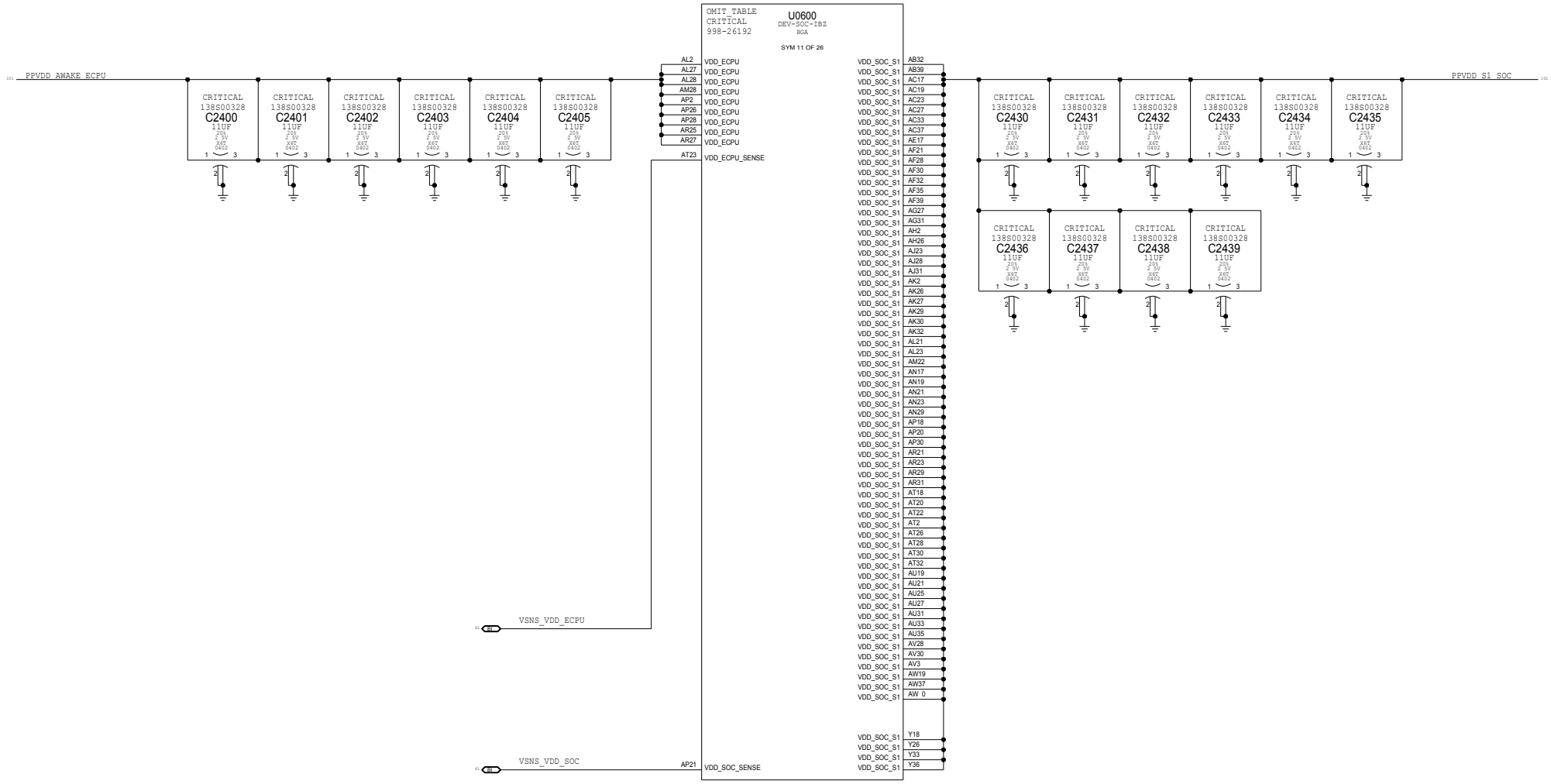
PAGE TITLE
SOC: POWER PCPU

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 23 OF 801
SHEET 18 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (1) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (2) NOT TO REPRODUCE OR COPY IT (3) NOT TO RELEASE OR PUBLISH IT IN WHOLE OR PART. ALL RIGHTS RESERVED.

www.repairlap.com



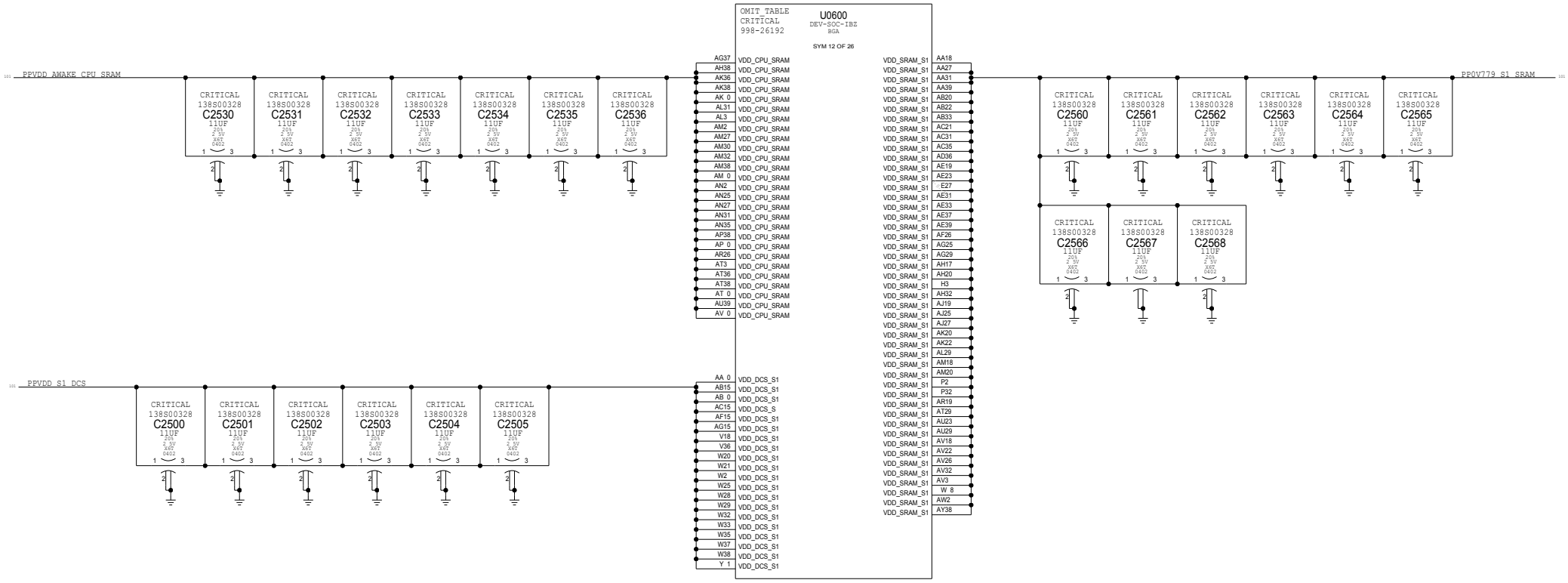
PAGE TITLE
SOC: POWER ECPU

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 24 OF 801
SHEET 19 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (I) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE, (II) NOT TO REPRODUCE OR COPY, (III) NOT TO RELEASE, PUBLISH, IN WHOLE OR PART, (IV) ALL RIGHTS RESERVED.

www.repairlap.com



BOM_COST_GROUP=SOC

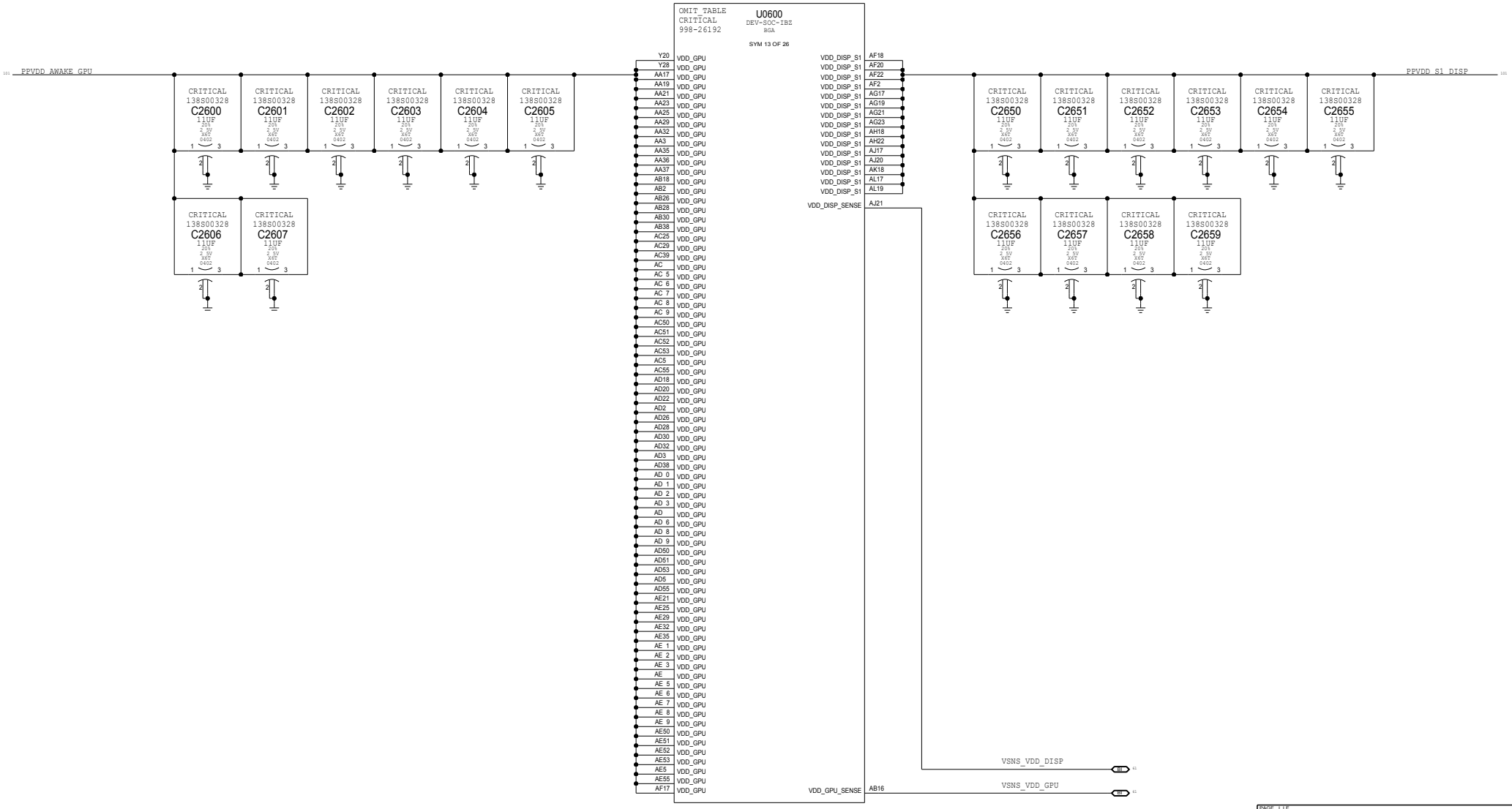
PAGE TITLE
SOC: POWER SRAM

Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 25 OF 801
SHEET 20 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (I) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE, (II) NOT TO REPRODUCE OR COPY, (III) NOT TO REVEAL, PUBLISH, IN WHOLE OR PART, ALL RIGHTS RESERVED.

www.repairlap.com



SOC: POWER GRAPHICS

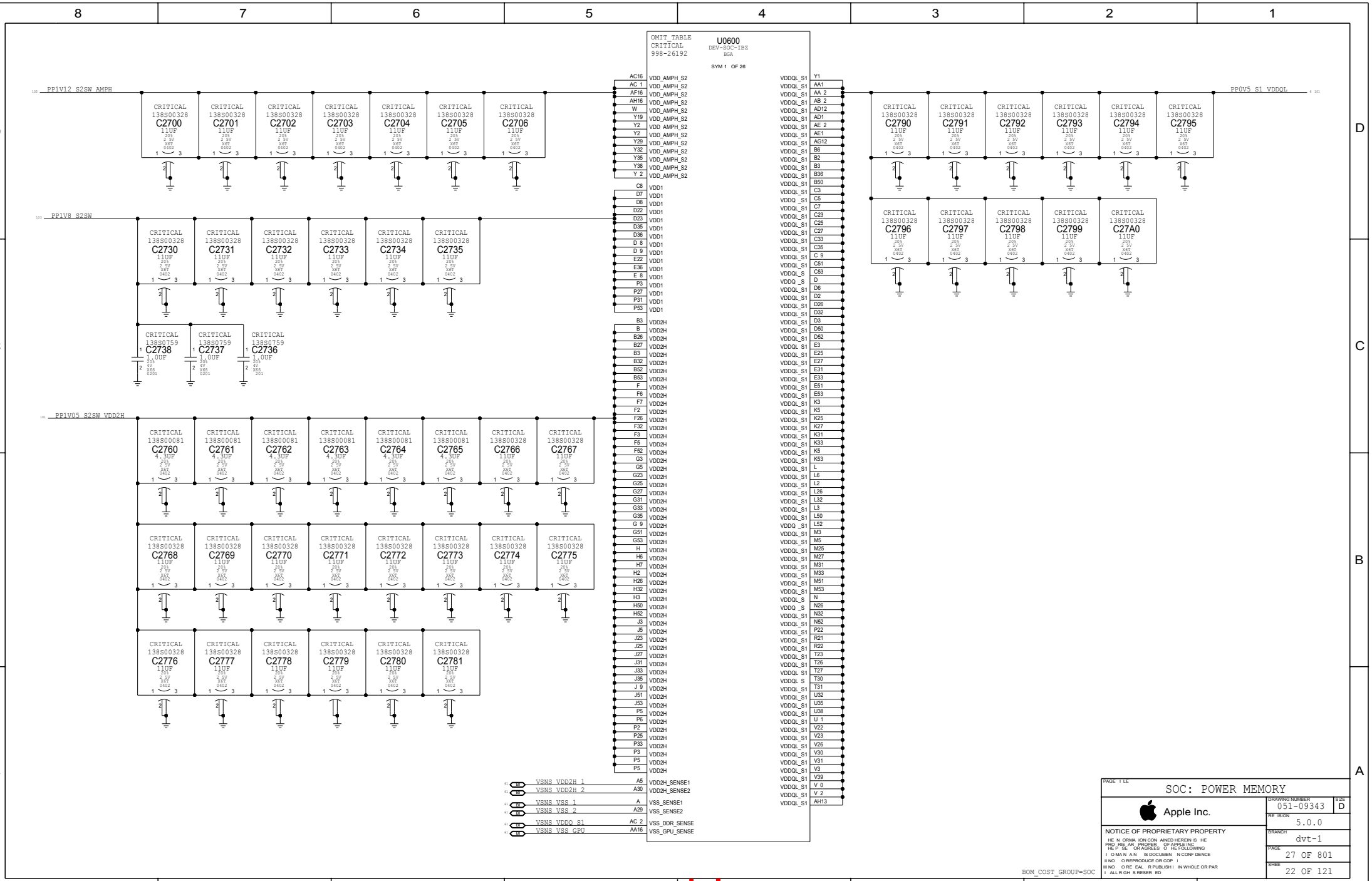
Apple Inc.

NOTICE OF PROPRIETARY PROPERTY

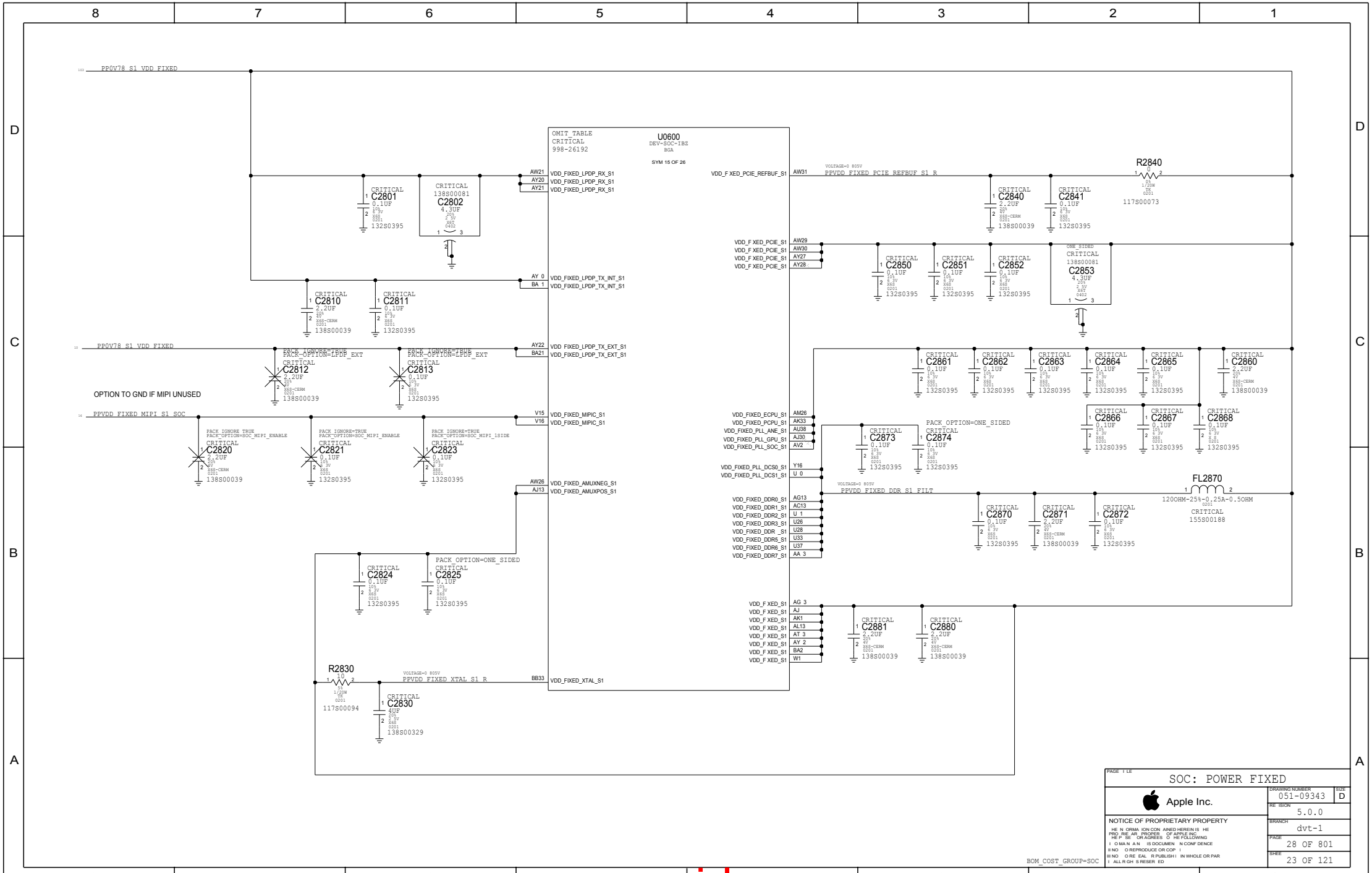
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE STATED HEREIN, THE FOLLOWING IS THE PROPRIETARY DOCUMENT. NO PART OF THIS DOCUMENT MAY BE REPRODUCED OR COPIED IN WHOLE OR PART WITHOUT THE PRIOR WRITTEN CONSENT OF APPLE INC. ALL RIGHTS RESERVED.

DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	26 OF 801
SHEET	21 OF 121

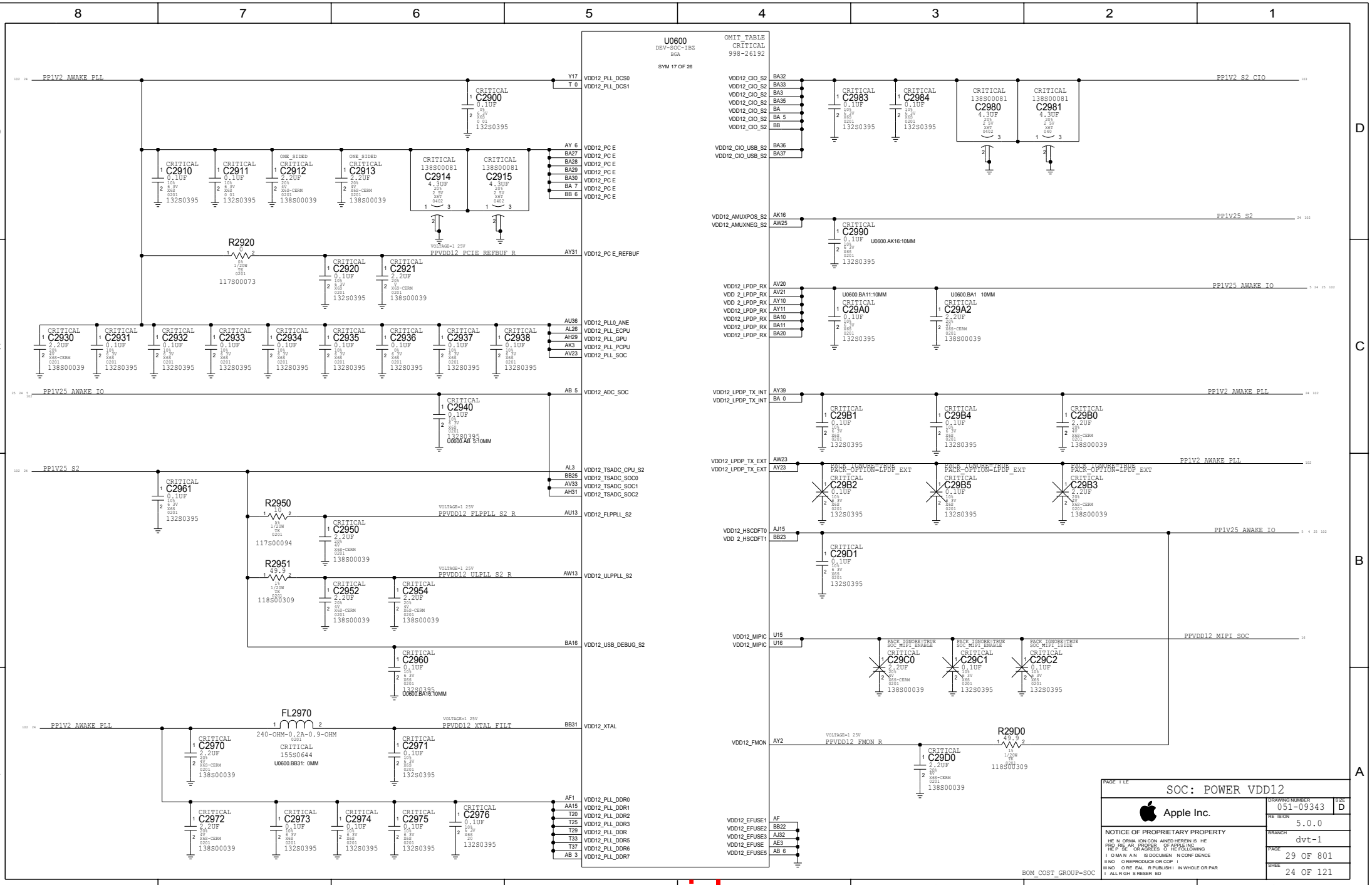
www.repairlap.com



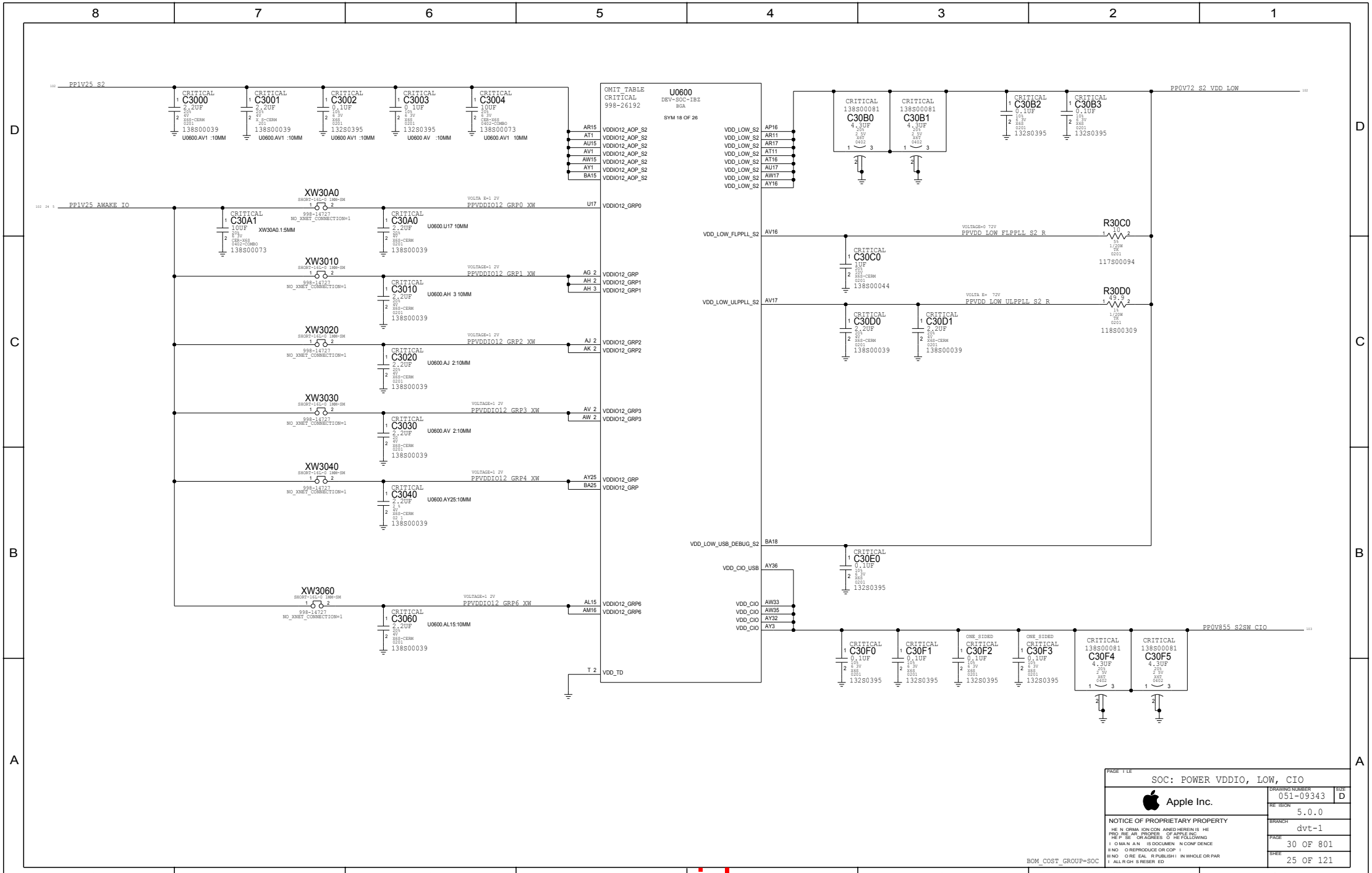
www.repairlap.com



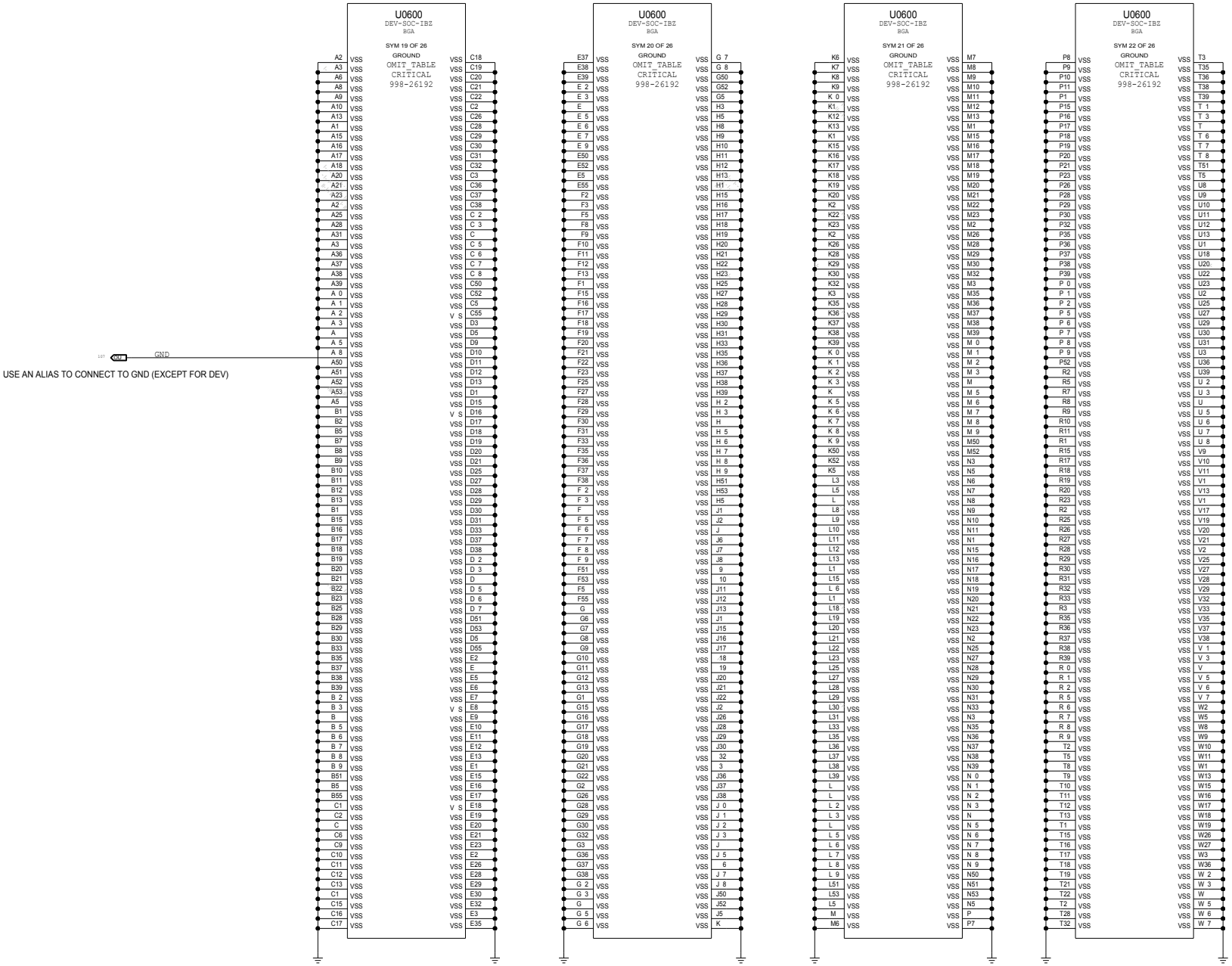
www.repairlap.com



www.repairlap.com



www.repairlap.com



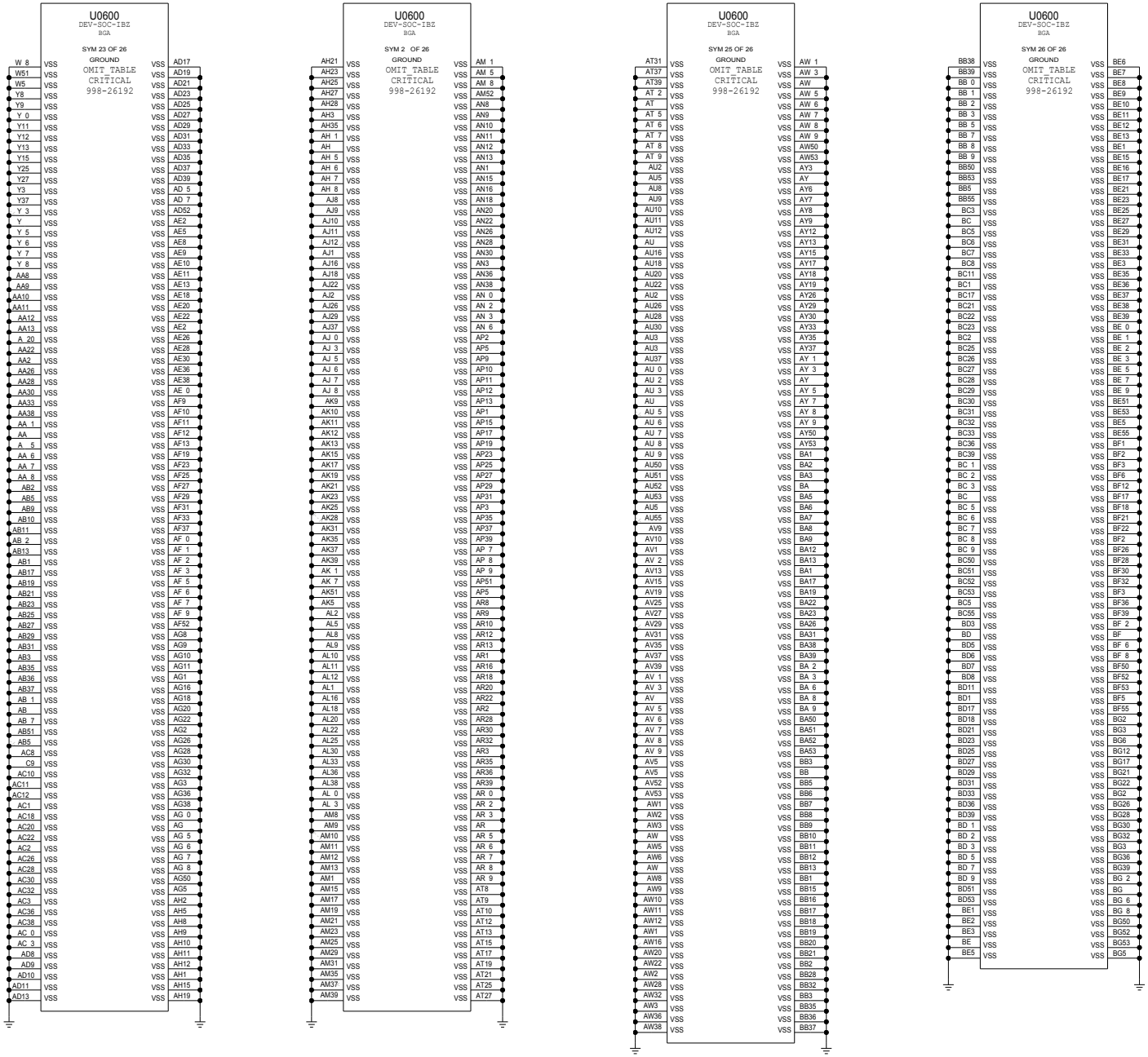
PAGE TITLE
SOC: GND (1 OF 2)

Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 40 OF 801
SHEET 26 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS PER WRITTEN AGREEMENT OF THE FOLLOWING
1. THIS DOCUMENT CONTAINS CONFIDENCE
2. NO REPRODUCE OR COPY
3. NO OTHER PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com



PAGE TITLE
SOC: GND (2 OF 2)

Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 41 OF 801
SHEET 27 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OF AGREES TO THE FOLLOWING: (I) MAINTAIN IS DOCUMENT IN CONFIDENCE (II) NOT REPRODUCE OR COPY IT (III) NOT DISCLOSE IT IN WHOLE OR PART. ALL RIGHTS RESERVED

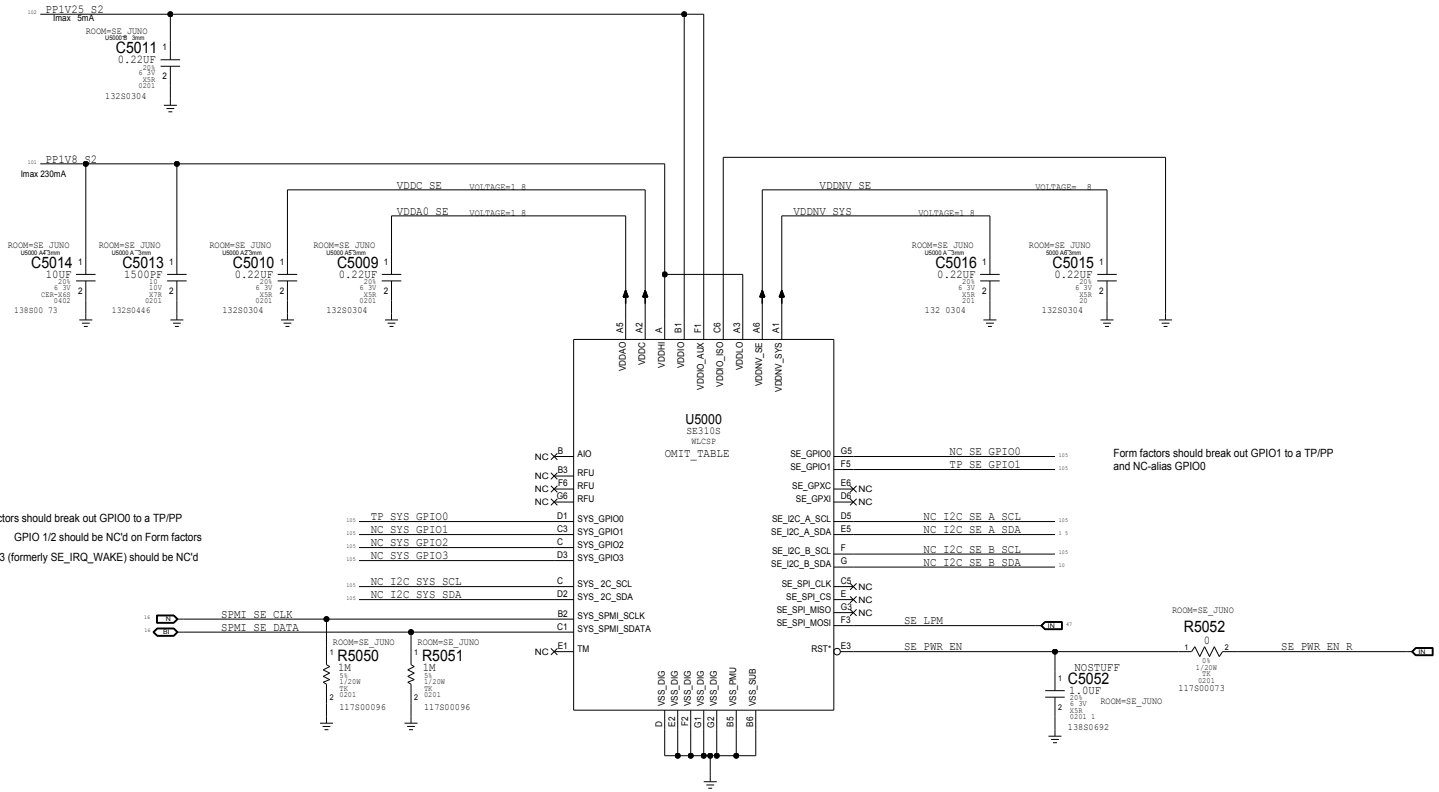
www.repairlap.com

Juno - Secure Element

AONSW nets will connect to e ther AON LDOs or dedicated AONSW rails. Consult power arch docs to determine appropriate connectivity.

Form factors should break out GPIO0 to a TP/PP
GPIO 1/2 should be NC'd on Form factors
SE_SYS_GPIO3 (formerly SE_IRQ_WAKE) should be NC'd

Form factors should break out GPIO1 to a TP/PP and NC-alias GPIO0



PAR #	Q	DESCRIP ION	REFERENCE DESIGNA OR(S)	BOM OP ON
338S00941	1	IC,JUNO,SE310S,A0,DEV,10C,WLCSP42	U5000	JUNO A0_DEV
338S00956	1	IC,JUNO,SE310S,A0,PROD,1PB,WLCSP42	U5000	JUNO A0_PROD
338S01012	1	IC,JUNO,SE310S,A0,0 V,10C1,WLCSP42	U5000	JUNO A0_DEV_DLY
338S 1013	1	IC,JUNO,SE310S,A0,PRO ,1P 1,WLCSP42	U5000	JUNO A0_PROD_DLY

<rdar://problem/89368110> [SE310S] Data Sheet
<rdar://problem/90105225> [SE310S] Juno Reference Schematic

BOM_COST_GROUP=SECURE ELEMENT

SYNC MASTER=SecureElement SYNC DATE=05/22/2023

PAGE TITLE: Secure Element

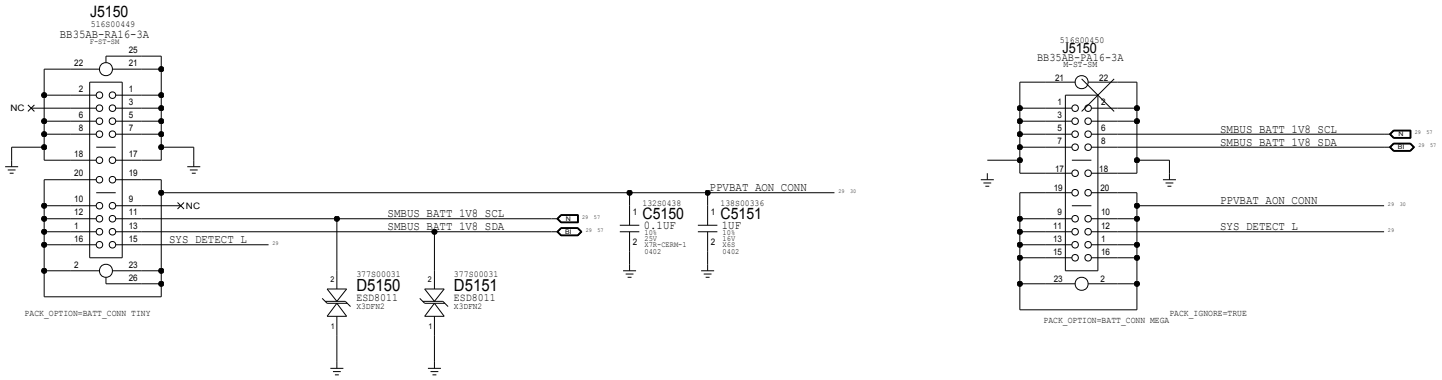
Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D
REVISION: 5.0.0
BRANCH: dvt-1
PAGE: 50 OF 801
SHEET: 28 OF 121

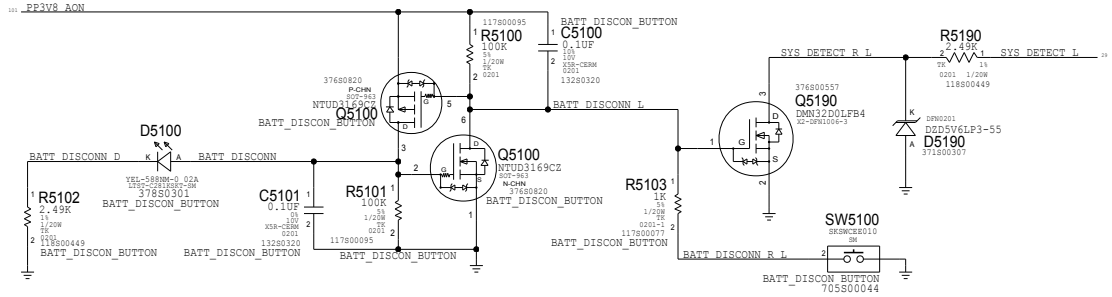
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (I) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE, (II) NOT TO REPRODUCE OR COPY IT, (III) NOT TO RELEASE PUBLISH IT IN WHOLE OR PART. ALL RIGHTS RESERVED.

www.repairlap.com

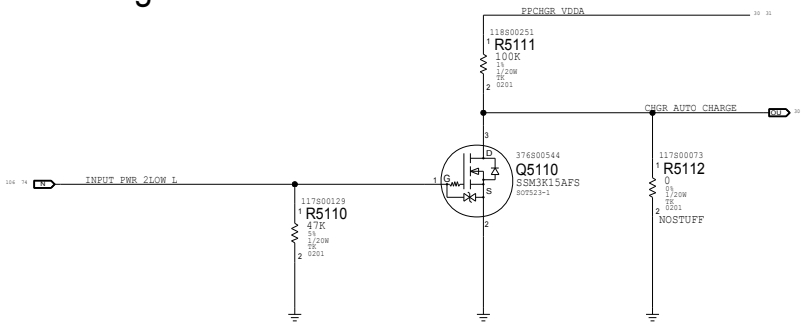
A BMU Connector



B BMU SYS_DETECT Circuit



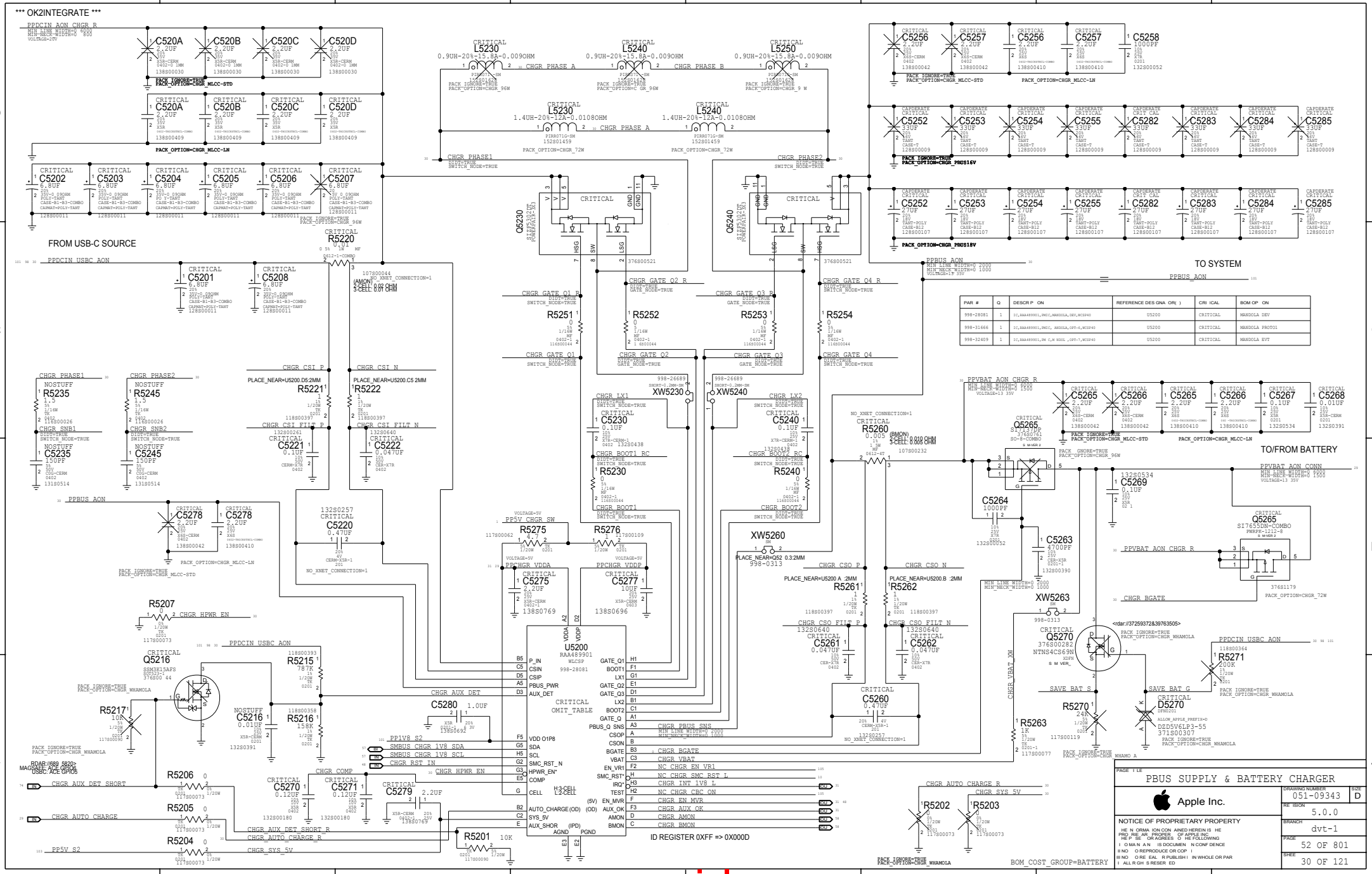
C Auto-Charge Enable



BOM_COST_GROUP=BATTERY

PAGE TITLE	Battery Connector
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 51 OF 801
	SHEET 29 OF 121

www.repairlap.com



PART #	Q	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-28081	1	IC,RAA489901,PMIC,MANDOLA,DEV,WCSP40	U5200	CRITICAL	MANDOLA DEV
998-31666	1	IC,RAA489901,PMIC, MANDOLA,OPT-6,WCSP40	U5200	CRITICAL	MANDOLA PROTO1
998-32409	1	IC,RAA489901,PW C,M NDOL ,OPT-7,WCSP40	U5200	CRITICAL	MANDOLA EVT

www.repairlap.com

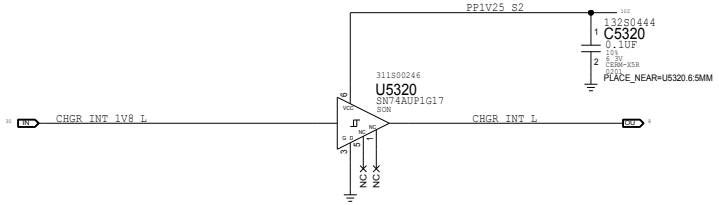
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level transla ion circu t to be placed in project speci ic I2C page.

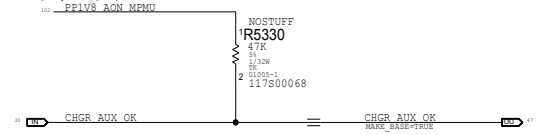
Probe points - bottom

CHGR_INT_L Level Translation



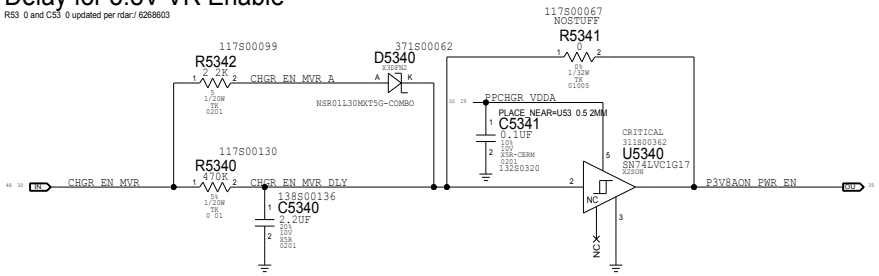
CHGR_AUX_OK Pull Up

Pu l up to MPMU LDO9, or rely on MPMU internal pull u . .
OK, to completely remo e p ll up , but consult PMU architecture and check OTP before that.

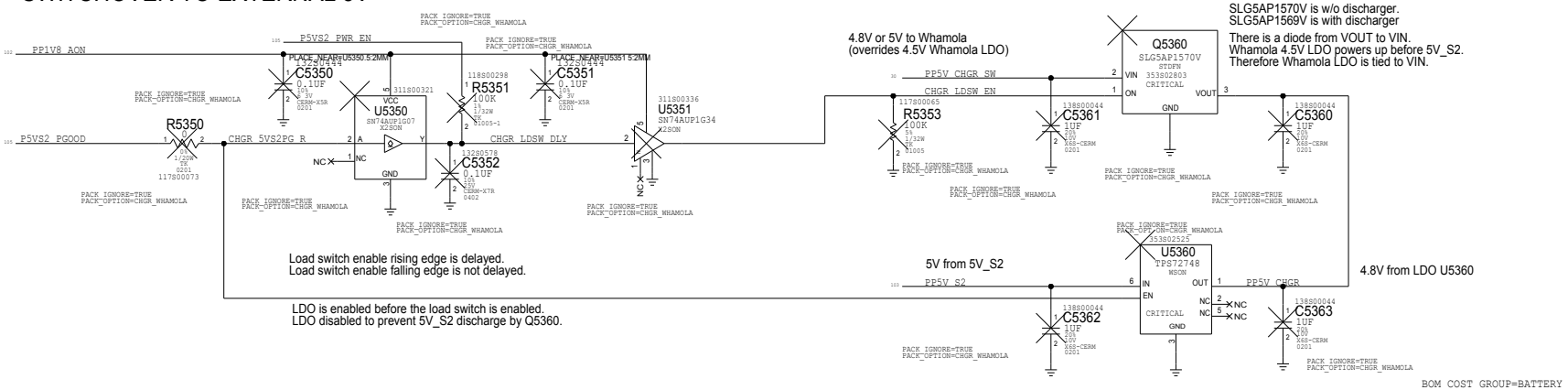


Delay for 3.8V VR Enable

R53 0 and C53 0 updated per rdar:/ 6268603



SWITCHOVER TO EXTERNAL 5V

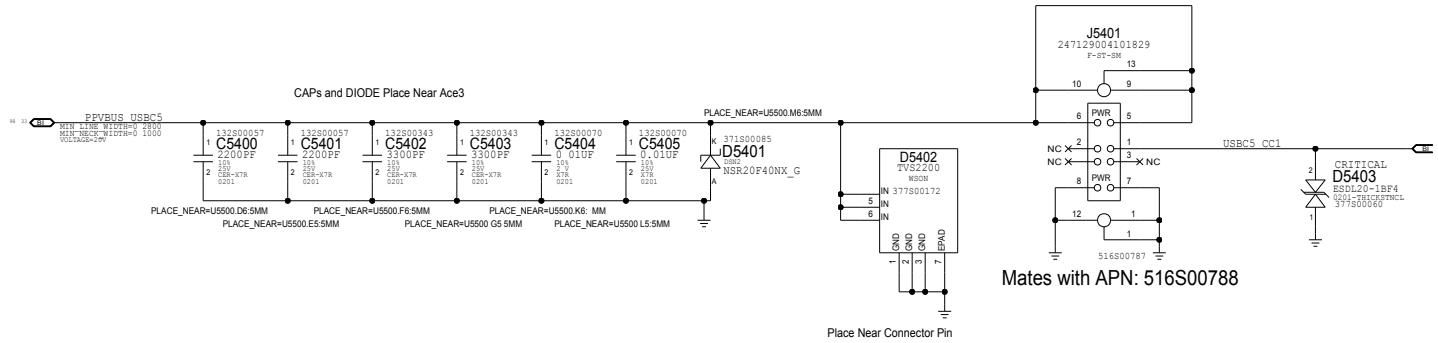


BOM_COST_GROUP=BATTERY

PAGE TITLE	BATTERY CHARGER SUPPORT
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
NOTICE OF PROPRIETARY PROPERTY	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 53 OF 801
	SHEET 31 OF 121

www.repairlap.com

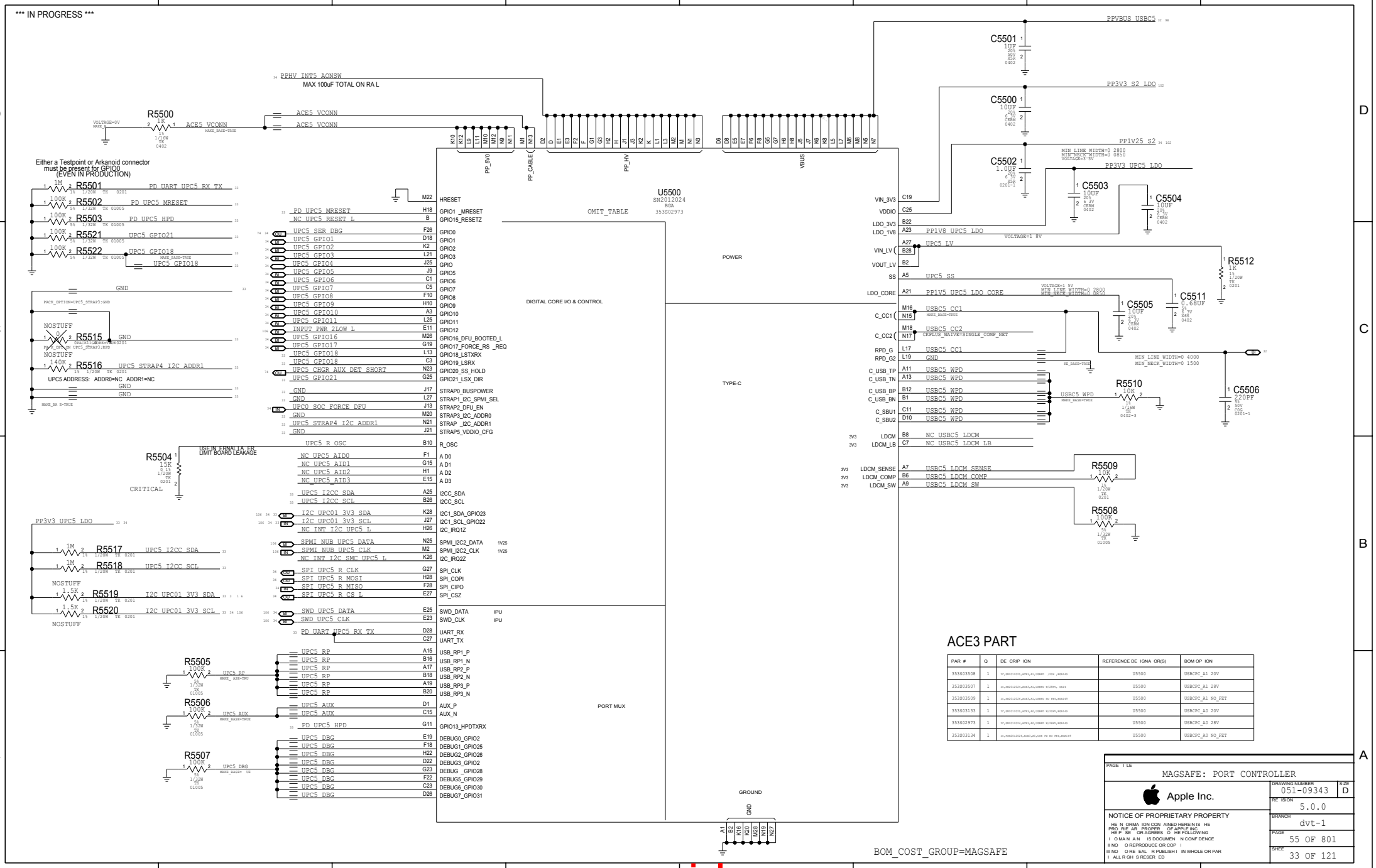
Ⓐ MagSafe Connector



BOM_COST_GROUP=MAGSAFE

PAGE TITLE	MAGSAFE: CONNECTOR
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 54 OF 801
	SHEET 32 OF 121

www.repairlap.com



ACE3 PART

PAR #	Q	DE CRIP ION	REFERENCE DE IGNA OR(S)	BOM OP ION
353803508	1	IC,SN2012024,ACE3,A1,USB PD /20W,BGA149	U5500	USBCPC_A1 20V
353803507	1	IC,SN2012024,ACE3,A1,USB PD 8/28V, GA14	U5500	USBCPC_A1 28V
353803509	1	IC,SN2012024,ACE3,A1,USB PD NO FET,BGA149	U5500	USBCPC_A1 NO_FET
353803133	1	IC,SN2012024,ACE3,A0,USB PD 8/28V,BGA149	U5500	USBCPC_A0 20V
353802973	1	IC,SN2012024,ACE3,A0,USB PD 8/28V,BGA149	U5500	USBCPC_A0 28V
353803134	1	IC,SN2012024,ACE3,A0,USB PD NO FET,BGA149	U5500	USBCPC_A0 NO_FET

PAGE TITLE
MAGSAFE: PORT CONTROLLER

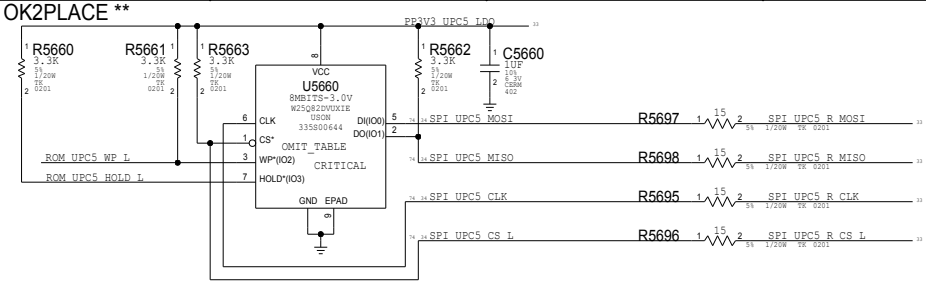
Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 55 OF 801
SHEET 33 OF 121

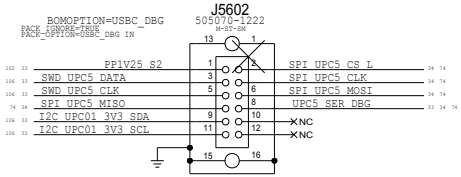
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING: THIS DOCUMENT CONTAINS INFORMATION. NO REPRODUCTION OR COPYING. NO REVEALING PUBLISHING IN WHOLE OR PART. ALL RIGHTS RESERVED.

www.repairlap.com

** OK2PLACE **

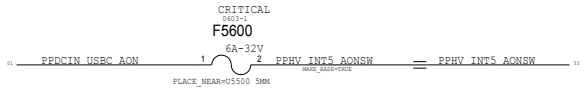


AARDVARKANOID CONN

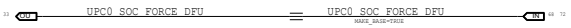


Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

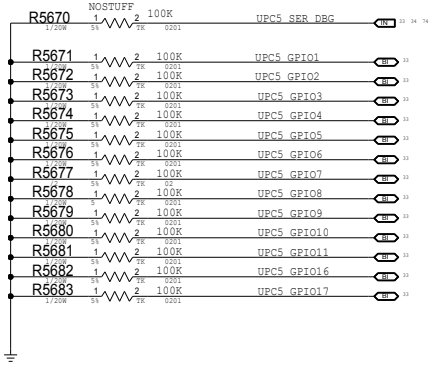
CONNECTION TO DCIN



UPC5 FUSE



Unused ports and GPIOs



BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: CONTROLLER SUPPORT

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

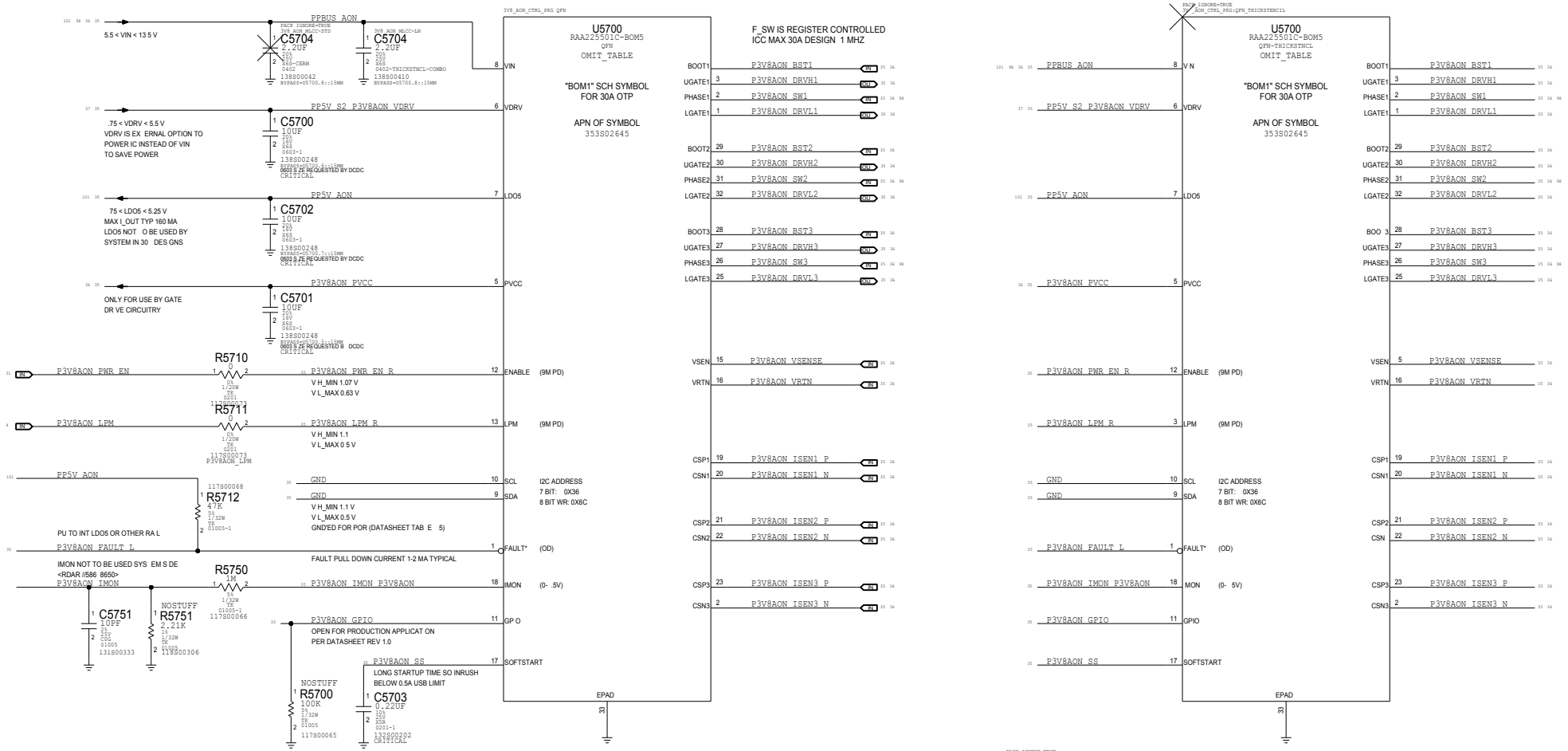
PAGE: 56 OF 801

SHEET: 34 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. EXCEPT WHERE OTHERWISE AGREED TO BY THE FOLLOWING THIS DOCUMENT IS CONFIDENTIAL. NO REPRODUCTION OR COPY IN WHOLE OR PART IS ALLOWED. ALL RIGHTS RESERVED.

www.repairlap.com

3V8 AON CONTROLLER
30A ICC MAX



30A OTP CHANGES DOCUMENTED IN <RDAR //61519509>
BOM5 IS A CONTINUATION OF BOM1 SINCE BOM1 S FROZEN FOR TGA PROGRAMS

PAR #	Q	DESCR P ION	REFERENCE DESIGNA OR( )	CRI ICAL	BOM OP ON
353802326	1	IC, AAZ25501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC A0
353802472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-RGB0,QFN32	U5700	CRITICAL	P3V8AON_IC A1_RGB0
353802544	1	IC,RAA225501B,ICE,BOM1,A1,OTP-RGB1,QFN32	U5700	CRITICAL	P3V8AON_IC A1_RGB1
353802560	1	IC,RAA225501B,ICE,BOM1,A1,OTP-RGB2,QFN32	U5700	CRITICAL	P3V8AON_IC A1_RGB2
353802576	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R B3, FN32	U5700	CRITICAL	P3V8AON_IC A1_RGB3
353802592		IC, AAZ25501B,ICE,BOM1,A2,OTP-R0 ,QFN32	U5700	CRITICAL	P3V8AON_IC A2_RGB0
353802645	1	C,RAA225501C,ICE,BOM5,A2,OTP-R170,QFN 2	U5700	CRITICAL	P3V8AON_IC A2_R170

<- 30A BOM OTP TGA PROGRAMS ARE GOING TO RAMP WITH
<- NEW BOM5 OTP FOR FUTURE PROGRAMS

BOM_COST_GROUP=SOC POWER

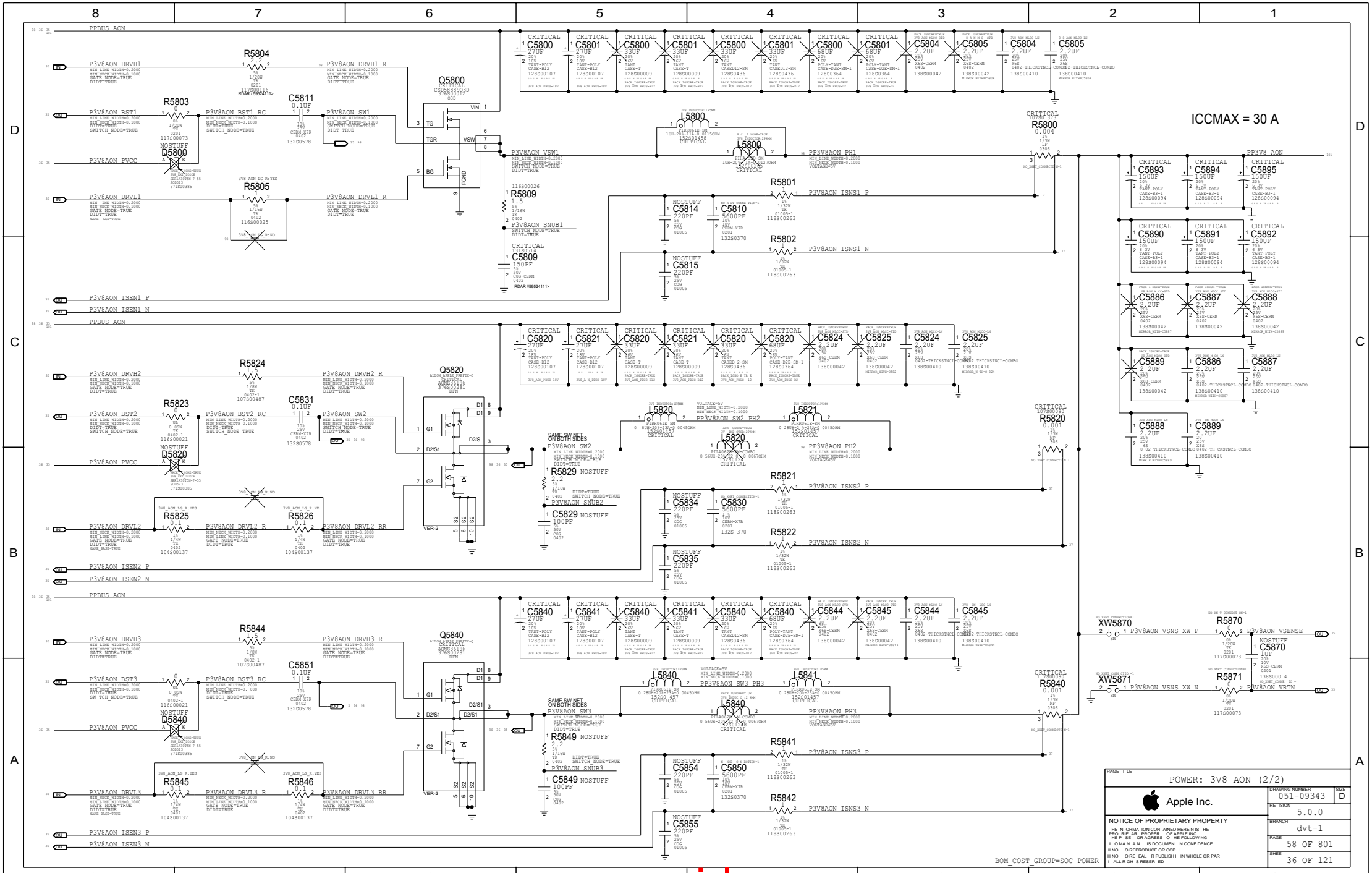
PAGE TITLE: POWER: 3V8 AON (1/2)

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES BY ACCEPTING OR ACCESSING THE DOCUMENT HEREIN AGREE TO THE FOLLOWING: (1) TO MAINTAIN IN CONFIDENCE THE DOCUMENT AND THE INFORMATION CONTAINED HEREIN, (2) NOT TO REPRODUCE OR COPY THE DOCUMENT, (3) NOT TO REVEAL, PUBLISH OR DISTRIBUTE THE DOCUMENT IN WHOLE OR PARTIAL, ALL RIGHTS RESERVED

DRAWING NUMBER: 051-09343 | SIZE: D
REVISION: 5.0.0
BRANCH: dvt-1
PAGE: 57 OF 801
SHEET: 35 OF 121

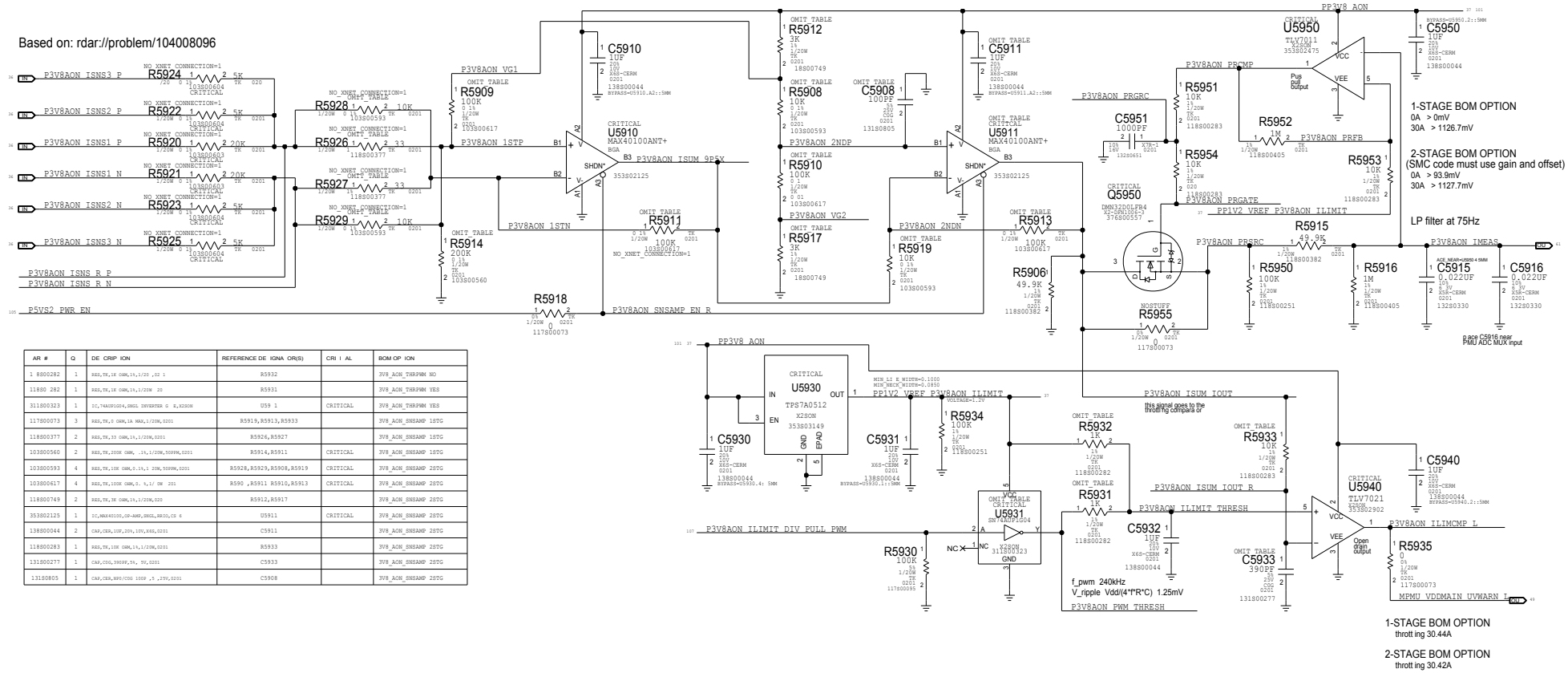
www.repairlap.com



www.repairlap.com

A PP3V8_AON Current Sensing & Throttling

Based on: rdar://problem/104008096



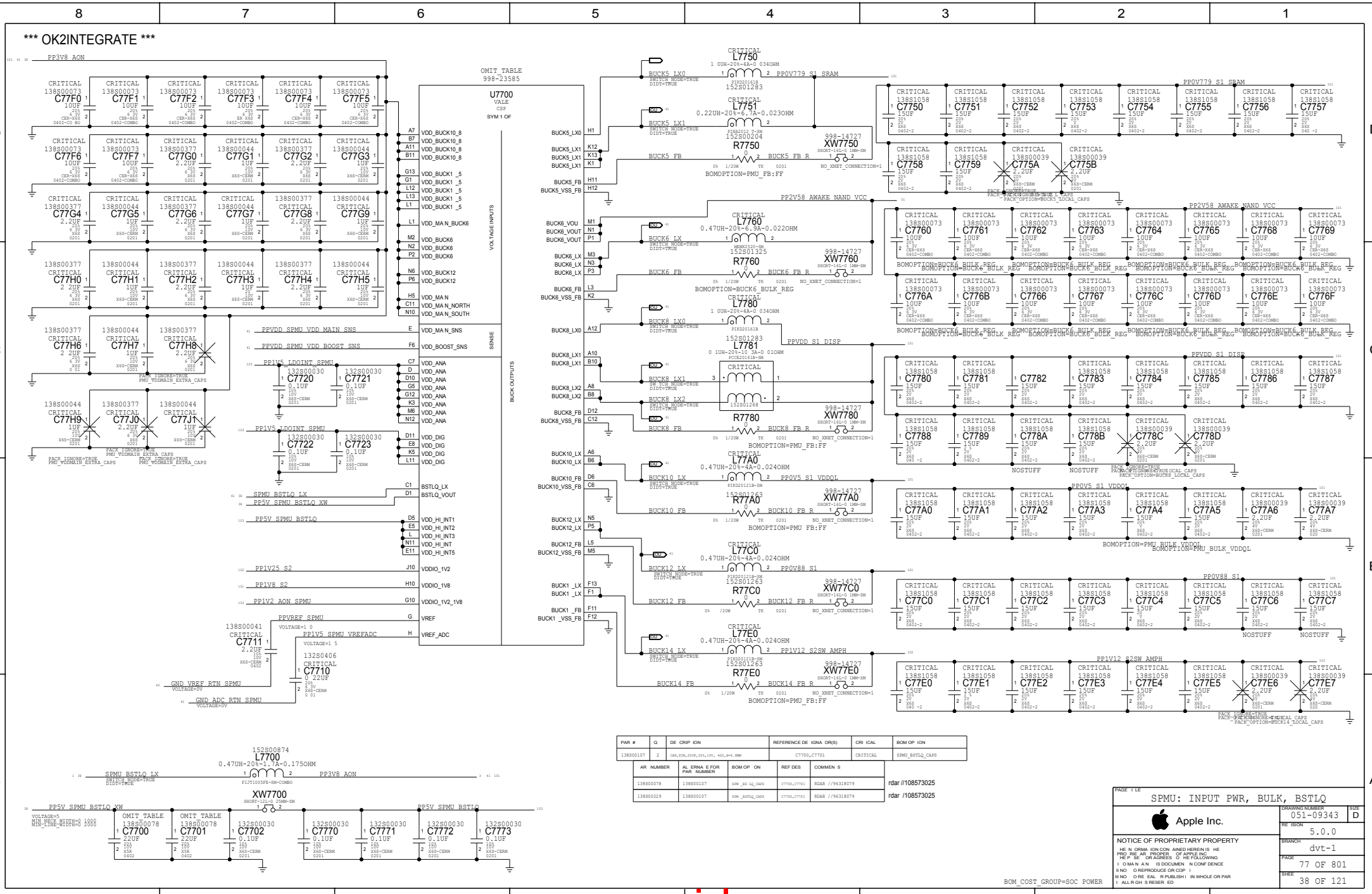
AR #	Q	DE CRIP ION	REFERENCE DE IGNA OR(S)	CRI I AL	BOM OP ION
1 8800282	1	RES,TK,1K OHM,1%,1/20 ,02 1	R5932		3V8_AON_THRPWM NO
11880 282	1	RES,TK,1K OHM,1%,1/20W 20	R5931		3V8_AON_THRPWM YES
311800323	1	IC,74AUP1G04,SNGL INVERTER G E,X2SON	U59 1	CRITICAL	3V8_AON_THRPWM YES
117800073	3	RES,TK,0 OHM,1A MAX,1/20W,0201	R5919,R5913,R5933		3V8_AON_SNSAMP 18TG
118800377	2	RES,TK,33 OHM,1%,1/20W,0201	R5926,R5927		3V8_AON_SNSAMP 18TG
103800560	2	RES,TK,200K OHM, .1%,1/20W,500PPM,0201	R5914,R5911	CRITICAL	3V8_AON_SNSAMP 18TG
103800593	4	RES,TK,10K OHM,0.1%,1 20W,500PPM,0201	R5928,R5929,R5908,R5919	CRITICAL	3V8_AON_SNSAMP 28TG
103800617	4	RES,TK,100K OHM,0. %,1/ OW 201	R590 ,R5911 R5910,R5913	CRITICAL	3V8_AON_SNSAMP 28TG
118800749	2	RES,TK,3K OHM,1%,1/20W,020	R5912,R5917		3V8_AON_SNSAMP 28TG
353802125	1	IC,MAX40100,OP-AMP,SNGL,WSIO,CS 6	U5911	CRITICAL	3V8_AON_SNSAMP 28TG
138800044	2	CAP,CER,10UF,20%,10V,X6S,0201	C5911		3V8_AON_SNSAMP 28TG
118800283	1	RES,TK,10K OHM,1%,1/20W,0201	R5933		3V8_AON_SNSAMP 28TG
131800277	1	CAP,CSG,390PF,5%, 50,0201	C5933		3V8_AON_SNSAMP 28TG
13180805	1	CAP,CER,NPO/COG 100P ,5 ,25V,0201	C5908		3V8_AON_SNSAMP 28TG

B PP5V_S2 to PP3V8_AON VDRV Connection

BOM_COST_GROUP=SOC POWER

PAGE TITLE	POWER: 3V8 AON SUPPORT
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
NOTICE OF PROPRIETARY PROPERTY	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 59 OF 801
	SHEET 37 OF 121

www.repairlap.com



PART #	Q	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S00107	2	CAP,X5R,20UF,20%,10V, 402,H=0.8MM	C7700,C7701	CRITICAL	SPMU_BSTLQ_CAPS

ARCHIVE NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS	
138S00078	138S00107	SPM_BSLQ_CAPS	C7700,C7701	RDAR //96318079	rdar //108573025
138S00229	138S00107	SPM_BSTLQ_CAPS	C7700,C7701	RDAR //96318079	rdar //108573025

www.repairlap.com

*** OK2INTEGRATE ***

OMIT_TABLE
998-23585

U7700
VALE
CSP
SYM 2 OF

LDO INPUTS

Net	Pin	Pin name
PP3V8_AON	M8	VDD_CTRL_LDOG
PP3V8_AON	A1, A, A3	VDD_BOOST_LDO
PP3V8_AON	C1, C2, C3	VDD_MAIN_LDO
PP3V8_AON	A	VDD_LDO15
PP1V25_S2	N7	VDD_LDO
PP0V88_S1	N8	VDD_LDO12

LDO OUTPUTS

Pin	Pin name	Net	Max
P7	VLDO	PP0V72_S2_VDD_LOW	LDO4 300MA MAX
D3	VLDO6	NC_SPMU_VLDO6	LDO6 50MA MAX
D1	VLDO9	PP1V8_AON_SPMU	LDO9 10MA MAX
B1	VLDO9B	PP1V2_AON_SPMU	LDO9B 10MA MAX
P8	VLDO12	PP0V78_S1_VDD_FIXED	LDO12 850MA MAX
B	VLDO15	NC_SPMU_VLDO15	LDO15 100MA MAX
B2	VLDO17	NC_SPMU_VLDO17	LDO17 250MA MAX
B3	VLDO18	NC_SPMU_VLDO18	LDO18 250MA MAX
D2	VLDOIN	PP1V5_LDOINT_SPMU	LDOINT 150MA MAX

LOAD SWITCHES

Net	Pin	Pin name
PP1V8_S2	M13	VDD_SW
PP1V25_S2	P13, P1	VDD_SW5
PP0V88_S1	P12	VDD_SW6
PP0V88_S1	P10	VDD_SW7

Pin	Pin name	Net	Max
M1	VSW	PP1V8_AWAKE_SPMU_GPIO	VSW4 200MA MAX, 125MOHM MAX
N13, N1	VSW5	PP1V25_AWAKE_NAND_VCCQ	VSW5 890MA MAX, 23MOHM MAX
P11	VSW6	PP0V88_AWAKE_NAND_VDD	VSW6 150MA MAX, 23MOHM MAX
P9	VSW7		VSW7 820MA MAX, 23MOHM MAX

VDD_LDO4
DECOUPLING SHARED WITH J10 (VDDIO_1V2)

PP1V25_S2
- CRITICAL 138S00073 C7820 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7821 10UF 20% 4V CER-X6S 0402-COMBO

VLDO4

PP0V72_S2_VDD_LOW
- CRITICAL 138S00073 C7840 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7841 10UF 20% 4V CER-X6S 0402-COMBO

VLDO12

PP0V78_S1_VDD_FIXED
- CRITICAL 138S00073 C78C0 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C78C1 10UF 20% 4V CER-X6S 0402-COMBO

VDD_SW4
DECOUPLING SHARED WITH H10 (VDDIO_1V8)

PP1V8_S2
- CRITICAL 138S00073 C7830 10UF 20% 4V CER-X6S 0402-COMBO

VSW4

PP1V8_AWAKE_SPMU_GPIO
- CRITICAL 138S00044 C7850 1UF 10% 10V X6S-CERM 0201

VLDO9

PP1V8_AON_SPMU
- CRITICAL 138S00073 C7890 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7891 10UF 20% 4V CER-X6S 0402-COMBO

VLDOINT

PP1V5_LDOINT_SPMU
- CRITICAL 138S00073 C7810 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7811 10UF 20% 4V CER-X6S 0402-COMBO

VDD_SW5
DECOUPLING SHARED WITH J10 (VDDIO_1V2)

PP1V25_S2
- CRITICAL 138S00073 C7822 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7823 10UF 20% 4V CER-X6S 0402-COMBO

VSW5

PP1V25_AWAKE_NAND_VCCQ
- CRITICAL 138S00073 C7860 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7861 10UF 20% 4V CER-X6S 0402-COMBO

VLDO9B

PP1V2_AON_SPMU
- CRITICAL 138S00073 C78A0 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C78A1 10UF 20% 4V CER-X6S 0402-COMBO

UN-UNUSED LDOS

LDO 6, 15, 17, 18

VDD_SW6/7
DECOUPLING SHARED VDD_LDO12

PP0V88_S1
- CRITICAL 138S00073 C7831 10UF 20% 4V CER-X6S 0402-COMBO

VSW6/7

PP0V88_AWAKE_NAND_VDD
- CRITICAL 138S00073 C7870 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7871 10UF 20% 4V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7872 10UF 20% 4V CER-X6S 0402-COMBO

BOM_COST_GROUP=SOC POWER

PAGE TITLE: SPMU: LDO, SW

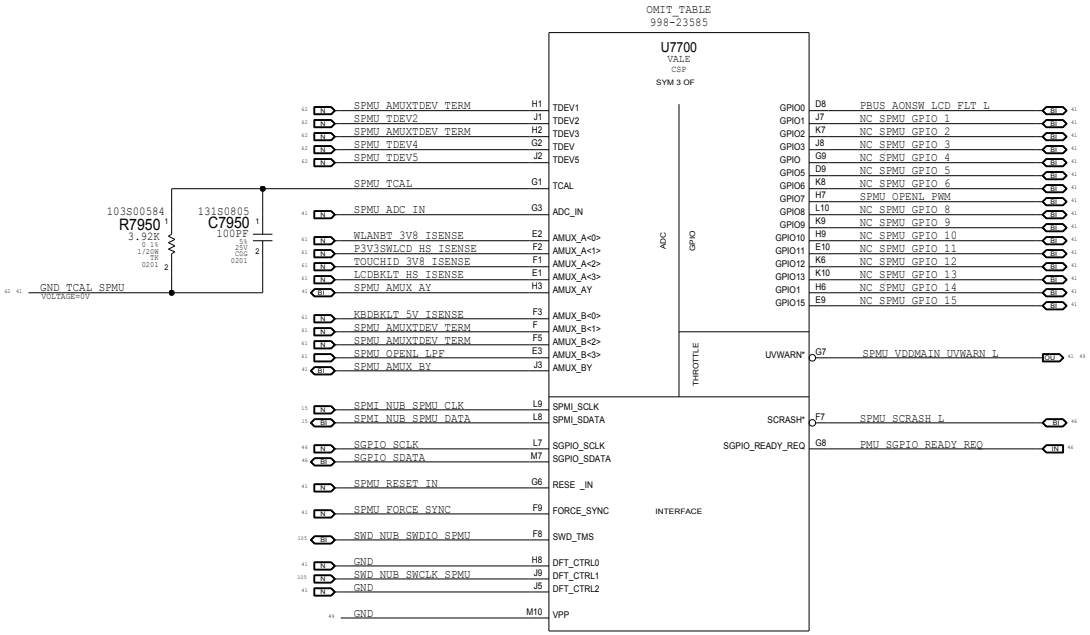
Apple Inc.

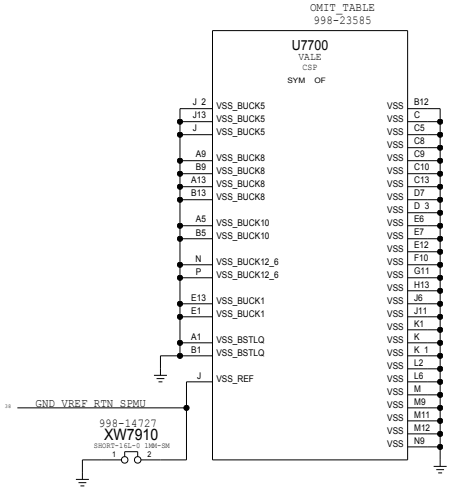
DRAWING NUMBER: 051-09343 | SIZE: D
REVISION: 5.0.0
BRANCH: dvt-1
PAGE: 78 OF 801
SHEET: 39 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (1) MAINTAIN IS DOCUMENT IN CONFIDENCE (2) NO REPRODUCE OR COPY (3) NO OTHER DISCLOSE PUBLISH IN WHOLE OR PART. ALL RIGHTS RESERVED

www.repairlap.com

*** OK2INTEGRATE ***





PLACEMENT NOTES

CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

BOM_COST_GROUP=SOC POWER

PAGE TITLE
SPMU: GPIO, VSS

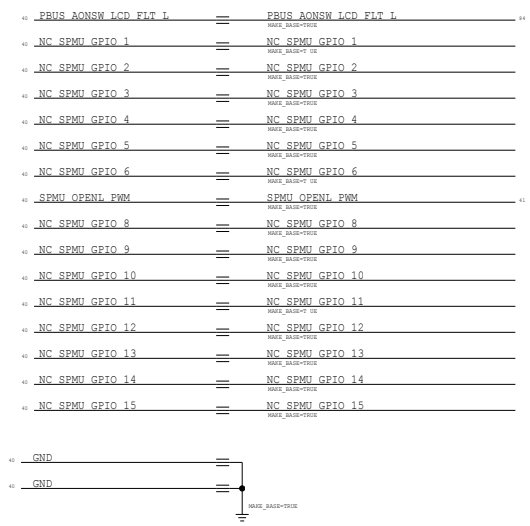
Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 79 OF 801
SHEET 40 OF 121

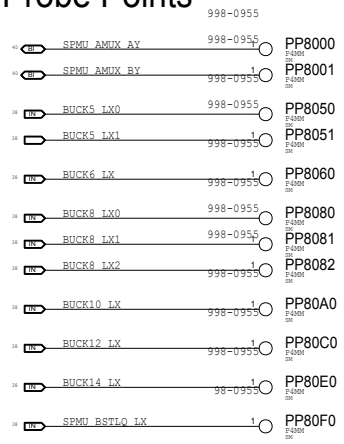
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING
1. OMIT ANY ANY DOCUMENT CONFIDENCE
2. DO NOT REPRODUCE OR COPY
3. DO NOT REVEAL PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

A SPMU GPIO

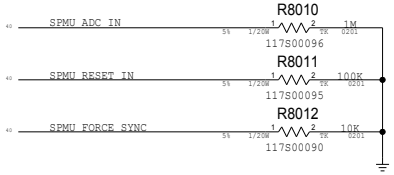


B Probe Points



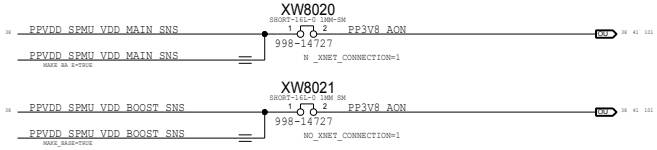
C SPMU Quiet GND Connections

D SPMU Input Protection

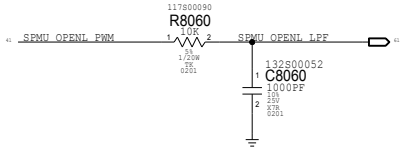


E SPMU/SOC Throttle PP

F SPMU Sense Connections



D SPMU Open Coil Test



BOM_COST_GROUP=SOC POWER

PAGE TITLE
SPMU: ALIASES, SUPPORT

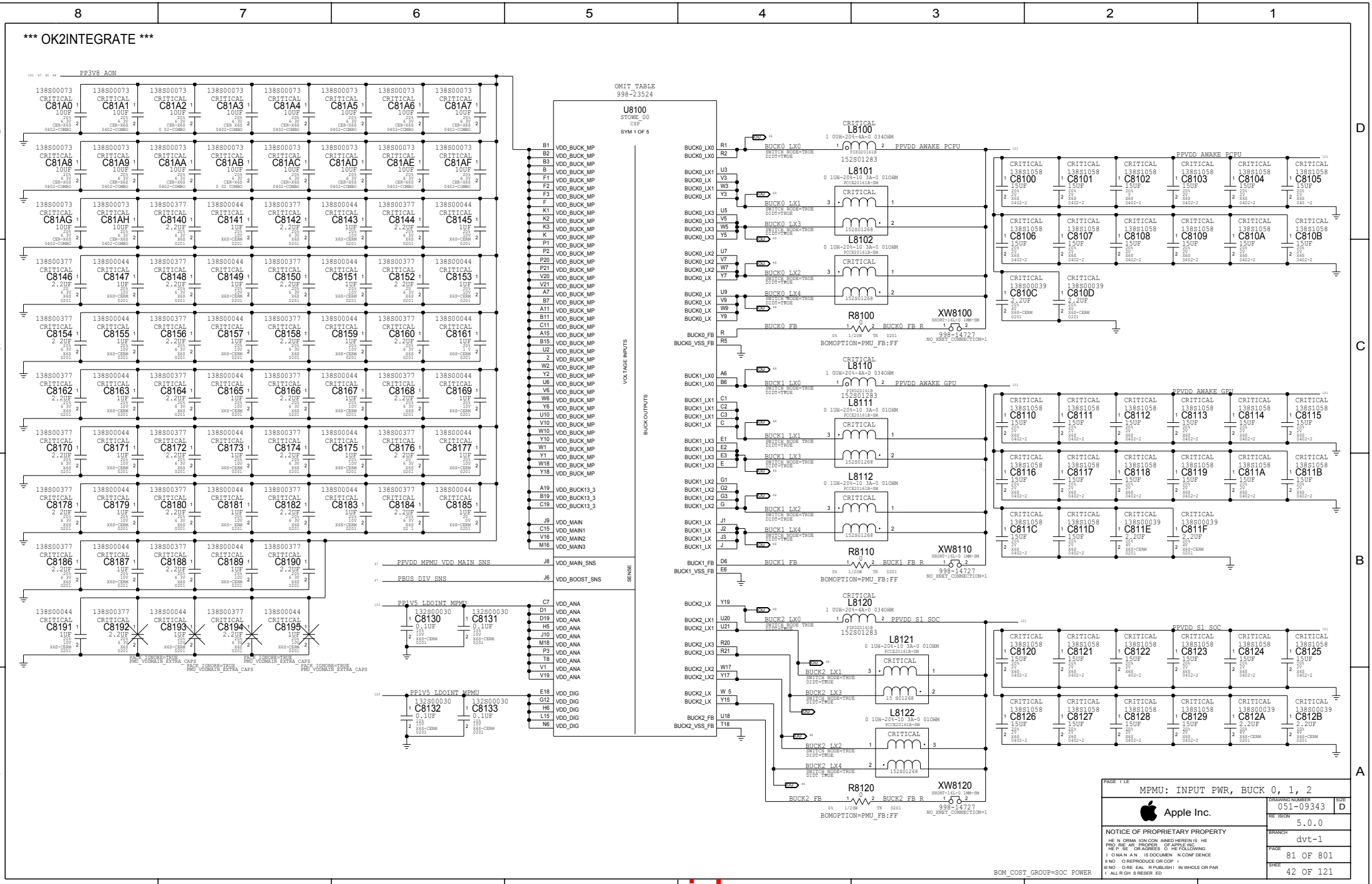
Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 80 OF 801
SHEET 41 OF 121

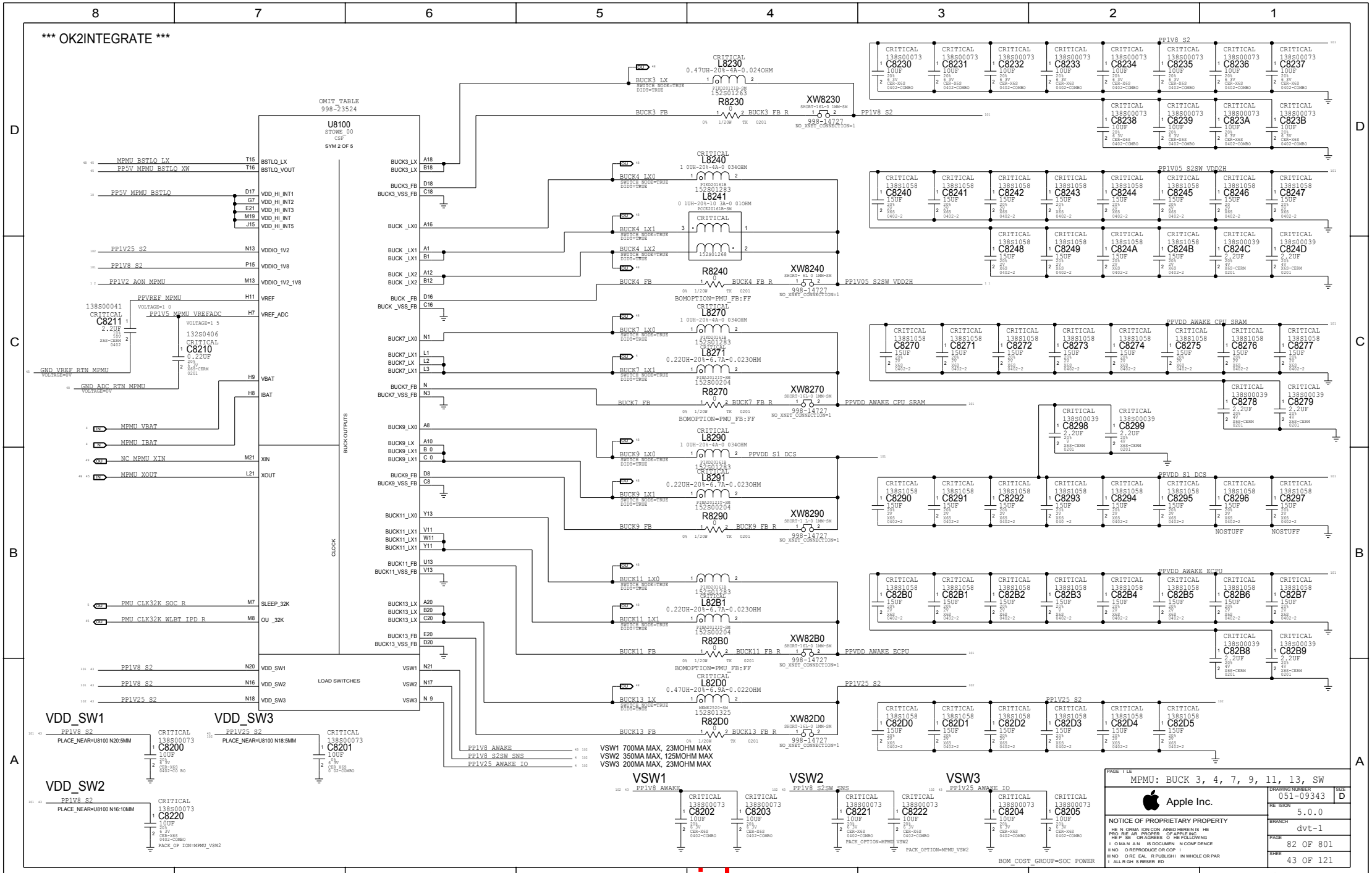
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (1) MAINTAIN IS DOCUMENT IN CONFIDENCE (2) NOT REPRODUCE OR COPY IT (3) NOT RELEASE PUBLISH IT IN WHOLE OR PART. ALL RIGHTS RESERVED

www.repairlap.com

*** OK2INTEGRATE ***



www.repairlap.com



www.repairlap.com

*** OK2INTEGRATE ***

OMIT_TABLE
998-23524

U8100
STOWE_00
CSP
SYM 3 OF 5

LDO INPUTS

Signal	Pin	Pin name
VDDMAIN>> PP3V8_AON	F15	VDD_CTRL_LDOG
PP3V8_AON	G7, G18, H7, H18, J18	VDD_BOOST_LDO
PP3V8_AON	J17, K17, K19	VDD_MAIN_LDO
PORTABLES SHOR TO VDD_MAIN >> DESKTOPS CONNEC TO CON CELL >> PP3V8_AON	L18	VDD_RTC_ALT
BUCK3 OR BUCK13>> PP1V25_S2	F19, F20, G20, H20	VDD_LDO20_1_8_3
BUCK >> PP1V05_S2SW_VDD2H	J20	VDD_LDO11
BUCK >> PP1V05_S2SW_VDD2H	F16	VDD_LDO16
IN NC_MPMU_LDO1_EN	R13	LDO1_EN

LDO OUTPUTS

Pin	Signal	Rail	Max
G19	NC_MPMU_VLDO1	LDO1	300MA MAX
J16	PP1V8_AON	LDO2	50MA MAX
F18	NC_MPMU_VLDO3	LDO3	600MA MAX
G16	NC_MPMU_VLDO5	LDO5	250MA MAX
H19	PP3V3_S2_LDO	LDO7	250MA MAX
H21	PP1V2_AWAKE_PLL	LDO8	730MA MAX
K16	PP1V8_AON_MPMU	LDO9	10MA MAX
K18	PP1V2_AON_MPMU	LDO9B	10MA MAX
H16	PP3V3_AON	LDO10	250MA MAX
J21	PP0V855_S2SW_CIO	LDO11	1000MA MAX
J19	NC_PPVOUT_MPMU_VLDO13_REG	LDO13	250MA MAX
F21	NC_MPMU_VLDO14	LDO14	300MA MAX
F17	NC_MPMU_VLDO16	LDO16	1500MA MAX
G21	PP1V2_S2_CIO	LDO20	400MA MAX
K20	PP1V5_LDOINT_MPMU	LDOINT	150MA MAX
L19	PP1V5_LDOINT_MPMU	VLDORTC	VLDORTC: SHORT TO LDO_INT FOR PORTABLES VLDORTC: CONNECT TO DECOUPLING CAP (ENABLE PACK_OPT ON: PMU_DESKTOPS)
L20	GND	VLDORTC2	VLDORTC2: SHORT TO GND ONLY IF LDORTC2 IS DISABLED PER OTP (PORTABLES) VLDORTC2: DEV/DESKTOP HAVE OPTIONS TO USE LDORTC2

UN-UNUSED LDOS

LDO 3, 5, 14, 16

VDD LDO 3/8/14/20

PP1V25_S2

Part	Value	Note
C8300	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8301	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073

VLDO2 DECOUPLING

PP1V8_AON

Part	Value	Note
C8320	4.7UF 20% 6.3V X6S 40	CRITICAL 138S0750; PACK_OPTION=PMU_LDO2

VLDO9 DECOUPLING

PP1V8_AON_MPMU

Part	Value	Note
C8310	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8311	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073

VLDO11 DECOUPLING

PP0V855_S2SW_CIO

Part	Value	Note
C83B5	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C83B6	10UF 20% 6.3V CER-X6S 0402-C MBO	CRITICAL 138S00073

VLDOINT DECOUPLING

PP1V5_LDOINT_MPMU

Part	Value	Note
C8380	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8381	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073

VDD_LDO11

PP1V05_S2SW_VDD2H

Part	Value	Note
C83B0	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C83B1	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073

VLDO7 DECOUPLING

PP3V3_S2_LDO

Part	Value	Note
C8330	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8331	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073

VLDO9B DECOUPLING

PP1V2_AON_MPMU

Part	Value	Note
C8340	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8341	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073

VLDO13 DECOUPLING

NC_PPVOUT_MPMU_VLDO13_REG

Part	Value	Note
C83D0	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073; PACK_IGNORE=TRUE; PACK_OPTION=MPMU_VLDO13

VLDORTC DECOUPLING

PP1V5_LDOINT_MPMU

Part	Value	Note
C8370	4.7UF 20% 6.3V X6S 0402	CRITICAL 138S0750; PACK_IGNORE=TRUE; PACK_OPTION=PMU_DESKTOPS

VLDO1 DECOUPLING

NC_PPVOUT_MPMU_VLDO1

Part	Value	Note
C8390	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8391	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073; PACK_IGNORE=TRUE; PACK_OPTION=PMU_LDO1

PACK_IGNORE=TRUE
PACK_OPTION=PMU_LDO1

VLDO8 DECOUPLING

PP1V2_AWAKE_PLL

Part	Value	Note
C8360	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8361	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8362	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073

NOSTUFF

VLDO10 DECOUPLING

PP3V3_AON

Part	Value	Note
C83A0	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073; PACK_OPTION=PMU_LDO10

VLDO20 DECOUPLING

PP1V2_S2_CIO

Part	Value	Note
C8350	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073
C8351	10UF 20% 6.3V CER-X6S 0402-COMBO	CRITICAL 138S00073

VLDORTC2 DECOUPLING

GND

Part	Value	Note
C8371	1UF 20% 6.3V X6S-CERM 0201	138S00040; PMU_RTC_LDO_INT2; PACK_IGNORE=TRUE; PMU_DESKTOPS

BOM_COST_GROUP=SOC POWER

PAGE TITLE
MPMU: LDO

Apple Inc.

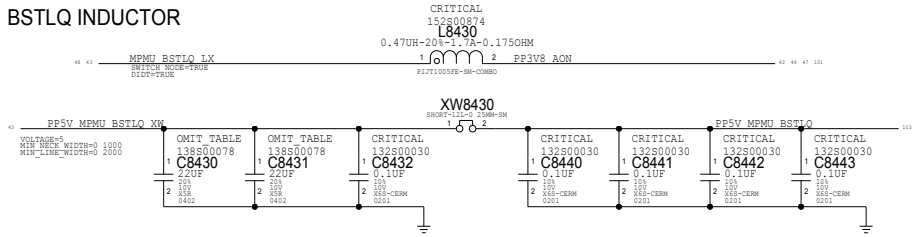
DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	83 OF 801
SHEET	44 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. EXCEPT WHERE OTHERWISE STATED THE FOLLOWING
THIS DOCUMENT CONTAINS CONFIDENCE
DO NOT REPRODUCE OR COPY
DO NOT DISCLOSE OR PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

*** OK2INTEGRATE ***

BSTLQ INDUCTOR

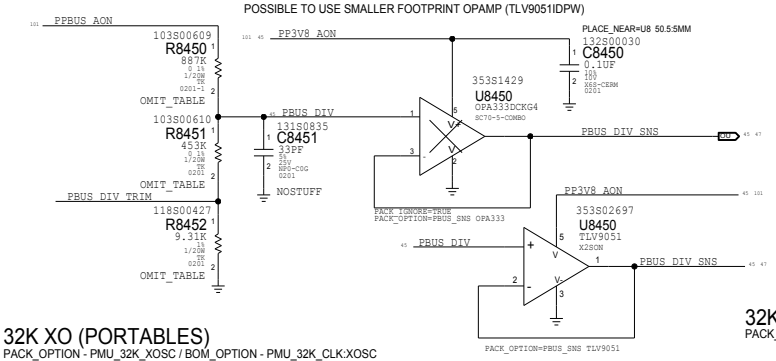


PAR #	Q	DE CR P ION	REFERENCE DE IGNA OR(S)	CRI ICAL	BOM OP ION
138800107	2	CAP,X5R,2 UF,20%,10V,0402,H=0.8MM	C8430,C8431	CRITICAL	MPMU_BSTLQ_CAPS

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S	
138800078	138800107	MPMU_BSTLQ_CAPS	C8430,C8431	RDAR //96318079	rdar //108573025
138800229	138800107	MPMU BST Q_CAPS	C8430,C8431	RDAR //96318079	rdar //108573025

PBUS SENSE

POSSIBLE TO USE SMALLER FOOTPRINT OPAMP (TLV9051IDPW)

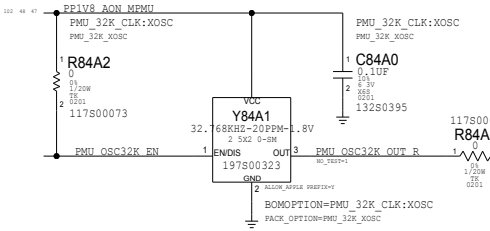


PAR #	Q	DESCR P ON	REFERENCE DES GNA OR( )	BOM OP ION
103800609	1	RES,TK,887KOHM,0.1%,50PPM,1/20W,0201	R8450	PMU_PBUS BATT38
103800610	1	RES,TK,453KOHM,0.1%,50PPM,1/20W,0201	R8451	PMU_PBUS BATT38
117800073	1	RES,TK,0OHM,1A MAX,1/20W, 201	R8452	PMU_PBUS BATT38
103800669	1	RES,TK,910 KOHM,0.1%,1/20W 020	R8 50	PMU_PBUS 12V
103800661	1	RE ,TK,280K OHM,0.1%,50PPM,1/20W, 201	R8451	PMU_PBUS 12V
117800073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8452	PMU_PBUS 12V
103800609	1	RES,TK,887KOHM,0.1%,50PPM,1/20W,0201	R8450	PMU_PBUS 15V8
103800658	1	RES,TK,205K OHM,0.1%,50PPM,1/20W,0201	R8451	PMU_PBUS 15V8
117800073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8452	PMU_PBUS 15V8
103800669	1	RES,TK,910 KOHM,0.1%,1/20W,0201	R8450	PMU_PBUS DEV_ UAL
103800661	1	RES,TK,280K OHM,0.1%,50PPM, 20 , 2 1	R84 1	PMU_PBUS DEV_DUAL
117800073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8452	PMU_PBUS DEV_DUAL

PMU_PBUS:DEV_DUAL IS POTENTIALLY USED IN DEV BOARD ON OTHER PAGES.
R8452 SHOULD BE 118S00427 (9.31K) IF ENABLING BOOST_SNS PULL DOWN CIRCUIT (NON POR)

32K XO (PORTABLES)

PACK_OPTION - PMU_32K_XOSC / BOM_OPTION - PMU_32K_CLK:XOSC
>> LDO9

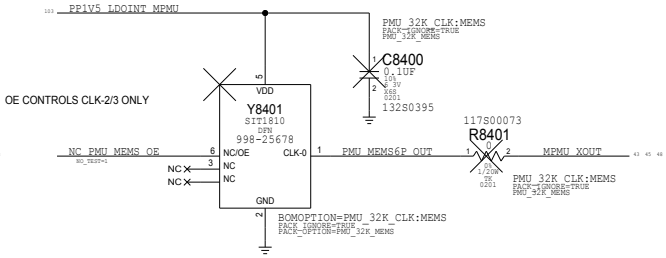


32K MEMS CLOCK (DESKTOPS)

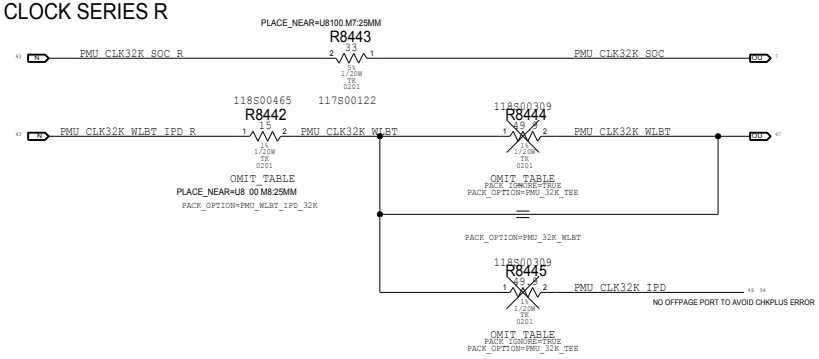
PACK_OPTION - PMU_32K_MEMS / BOM_OPTION - PMU_32K_CLK:MEMS

>> RTC SUPPLY (DISCRETE, VLDORTC, OR VLDORTC2)

OE CONTROLS CLK-2/3 ONLY

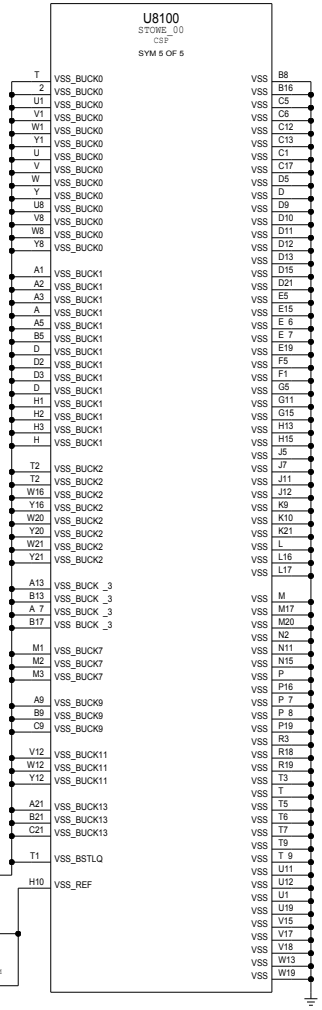


32K CLOCK SERIES R



PAR #	Q	DESCR P ON	REFERENCE DES GNA OR(	CRI ICAL	BOM OP ON
118S00465	1	RES,TK,15 OHM,1%,1/20W,0201	R8442		PMU_OUT32K TEE
117S00122	1	RES,TK,33 OHM,5%,1/20W,0201	R8442		PMU_OUT32K WLBT
118S00309	2	RES,TK,49 9 OHM,1%,1/20W,0201	R8444,R8445		PMU_OUT32K TEE

OMIT_TABLE
998-23524



PLACEMENT NOTES

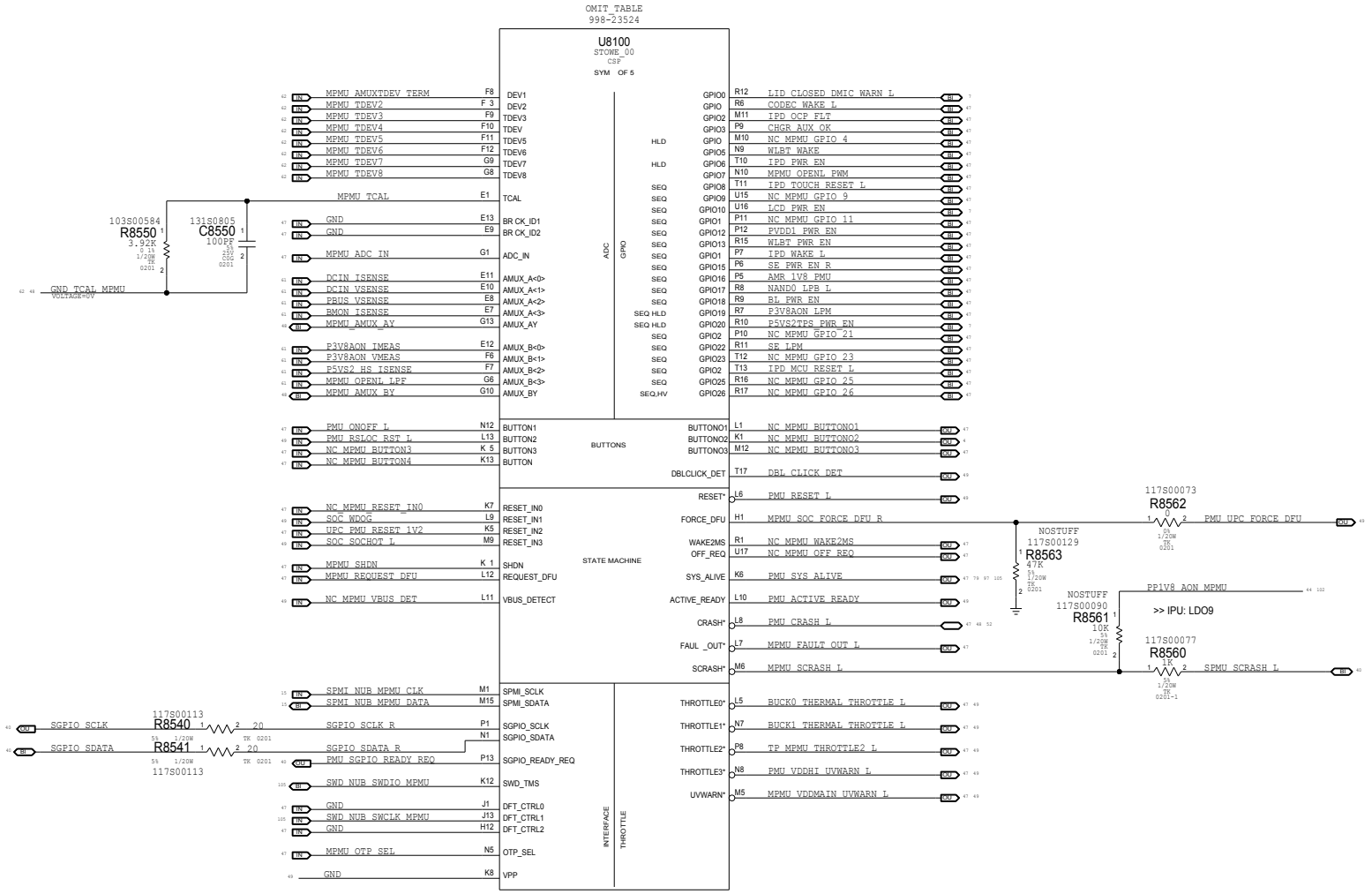
CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

BOM_COST_GROUP=SOC POWER

PAGE TITLE	MPMU: MISC CKT, VSS
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
NOTICE OF PROPRIETARY PROPERTY	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 84 OF 801
	SHEET 45 OF 121

www.repairlap.com

*** OK2INTEGRATE ***



PAGE TITLE	MPMU: GPIO
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 85 OF 801
	SHEET 46 OF 121

www.repairlap.com

A MPMU GPIO Aliases

IO OTP SETTINGS (WIP), IF NOT OTP IT WILL BE CONFIGURED AS SW OVERRIDE..
SUPPLY:LDO9 (1.8V AON), BUCK13 (1.25V S2), BUCK3 (1.8V S2), SLDO9B (1.2V AON)
IO TYPE: INPUT, OUTPUT OPEN DRAIN, OR OUTPUT PUSH PULL
PULLS: IPU, IPD, NONE

GPIO0: LDO9B IN NONE	LID_CLOSED_DMIC_WARN_L	LID_CLOSED_DMIC_WARN_L
GPIO1: LDO9 IN IPU	CODEC_WAKE_L	CODEC_WAKE_L
GPIO2: LDO9 IN IPD	IPD_OCP_FLT	IPD_OCP_FLT
GPIO3: BUCK13 IN IPD	CHGR_AUX_OK	CHGR_AUX_OK
GPIO4: -WIP- IN IPU	NC_MPMU_GPIO_4	NC_MPMU_GPIO_4
GPIO5: BUCK13 IN IPD	WLBT_WAKE	WLBT_WAKE
GPIO6: LDO9 PP NONE	IPD_PWR_EN	IPD_PWR_EN
GPIO7: LDO9 IN IPD > NEEDS OVERRIDE?	MPMU_OPENL_PWM	MPMU_OPENL_PWM
GPIO8: LDO9 OD NONE	IPD_TOUCH_RESET_L	IPD_TOUCH_RESET_L
GPIO9: LDO9 IN IPD > NEEDS OVERRIDE?	NC_MPMU_GPIO_9	NC_MPMU_GPIO_9
GPIO10: LDO9 PP NONE	LCD_PWR_EN	LCD_PWR_EN
GPIO11: LDO9 PP NONE	NC_MPMU_GPIO_11	NC_MPMU_GPIO_11
GPIO12: LDO9 OD NONE	PVDD1_PWR_EN	PVDD1_PWR_EN
GPIO13: -WIP- PP NONE	WLBT_PWR_EN	WLBT_PWR_EN
GPIO14: LDO9 IN NONE	IPD_WAKE_L	IPD_WAKE_L
GPIO15: LDO9 PP NONE	SE_PWR_EN_R	SE_PWR_EN_R
GPIO16: LDO9 IN IPD > NEEDS OVERRIDE?	AMR_1V8_PMU	AMR_1V8_PMU
GPIO17: BUCK13 PP NONE	NAND0_LPB_L	NAND0_LPB_L
GPIO18: LDO9 PP NONE	BL_PWR_EN	BL_PWR_EN
GPIO19: LDO9 PP IPD	P3V8AON_LPM	P3V8AON_LPM
GPIO20: LDO9 PP NONE	P5VS2TPS_PWR_EN	P5VS2TPS_PWR_EN
GPIO21: LDO9 IN IPD > NEEDS OVERRIDE?	NC_MPMU_GPIO_21	NC_MPMU_GPIO_21
GPIO22: LDO9 IN IPD > NEEDS OVERRIDE?	SE_LPM	SE_LPM
GPIO23: LDO9 IN IPD > NEEDS OVERRIDE?	NC_MPMU_GPIO_23	NC_MPMU_GPIO_23
GPIO24: LDO9 OD NONE	IPD_MCU_RESET_L	IPD_MCU_RESET_L
GPIO25: WIP PP NONE	NC_MPMU_GPIO_25	NC_MPMU_GPIO_25
GPIO26: LDO9 IN IPD > NEEDS OVERRIDE?	NC_MPMU_GPIO_26	NC_MPMU_GPIO_26

B MPMU Input Protection & Pull-Downs

P3V8AON_LPM	R8630 100K 5% 1/20W TK 020	117S00095
P5VS2TPS_PWR_EN	R8631 100K 5% 1/20W TK 0201 NOSTUFF	117S00095
MPMU_OTP_SEL PD FOR PORTABLES	R8622 0 0% 1/20W TK 0201	117S00073
MPMU_ADC_IN	R8610 1M 5% 1/20W TK 0201	117S00096
MPMU_IBAT	R8611 1M 5% 1/20W TK 0201	117S00096
MPMU_REQUEST_DFU	R8612 100K 5% 1/20W TK 0201	117S00095
MPMU_SHDN	R8613 10K 5% 1/20W TK 0201	117S00090
MPMU_VBAT	R8614 1M 5% 1/20W TK 0201	117S00096
IPD_PWR_EN	R8616 100K 5% 1/20W TK 0 01	117S00095

C MPMU Pull-Ups

PP1V8_AON_MPMU	R8620 10K 5% 1/20W TK 0201	117S00090
PMU_CRASH_L	R8621 100K 5% 1/20W TK 0201	117S00095
MPMU_FAULT_OUT_L	R8623 10K 5% 1/20W TK 0201	117S00090
PMU_ONOFF_L	R8624 10K 5% 1/20W TK 0201	117S00090
PMU_RSLOC_RST_L	R8625 100K 5% 1/20W TK 0201 NOSTUFF	117S00095
IPD_TOUCH_RESET_L	R8626 100K 5% 1/20W TK 0201 NOSTUFF	117S00095
IPD_MCU_RESET_L		
PP1V25_S2	R8640 10K 5% 1/20W TK 0201 NOSTUFF	117S00090
PMU_SYS_ALIVE		
PP1V25_AWAKE_IO	PP8600 PUMP SE	
BUCK0_THERMAL_THROTTLE_L	PP8601 PUMP SE	
BUCK1_THERMAL_THROTTLE_L	R8653 10K 5% 1/20W TK 0201	117S00090
TP_MPMU_THROTTLE2_L	PP8602 PUMP SE	
PMU_VDDHI_UVWARN_L	PP8603 PUMP SE	
MPMU_VDDMAIN_UVWARN_L		

D MPMU Open Coil Test

MPMU_OPENL_PWM — R8660 10K 1/20W 5% 0201 (117S00090) — MPMU_OPENL_LPF — OUT

C8660 1000PF 10% 25V X7R 0201 (132S00052)

D MPMU Misc Aliases

GND
GND
GND
GND

NC_MPMU_LDO1_EN
NC_MPMU_OFF_REQ
NC_MPMU_WAKE2MS

VLDORTC2 IS PLANNED FOR B0, AND CURRENTLY NOT IMPLEMENTED

GND

PMU_CLK32K_WLBT
NC_PPVOUT_MPMU_VLDO1

E MPMU VDD_MAIN Sense

PPVDD_MPMU_VDD_MAIN_SNS — XW8661 998-14727 (NO_XNET_CONNECTION=1) — PP3V8_AON — OUT

PPVDD_MPMU_VDD_MAIN_SNS

F MPMU VDD_BOOST Sense

IN PBUS_DIV_SNS — PBUS_DIV_SNS — OUT

G MPMU Button and Reset Aliases

PMU_ONOFF_L	PMU_ONOFF_L
NC_MPMU_BUTTON3	NC_MPMU_BUTTON3
NC_MPMU_BUTTON4	NC_MPMU_BUTTON4
NC_MPMU_BUTTON01	NC_MPMU_BUTTON01
NC_MPMU_BUTTON02	NC_MPMU_BUTTON02
NC_MPMU_BUTTON03	NC_MPMU_BUTTON03
NC_MPMU_RESET_IN0	NC_MPMU_RESET_IN0
UPC_PMU_RESET_1V2	UPC_PMU_RESET_1V2

BOM_COST_GROUP=SOC POWER

PAGE TITLE: MPMU: ALIAS, PULLS

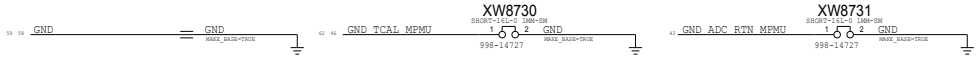
Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D
REVISION: 5.0.0
BRANCH: dvt-1
PAGE: 86 OF 801
SHEET: 47 OF 121

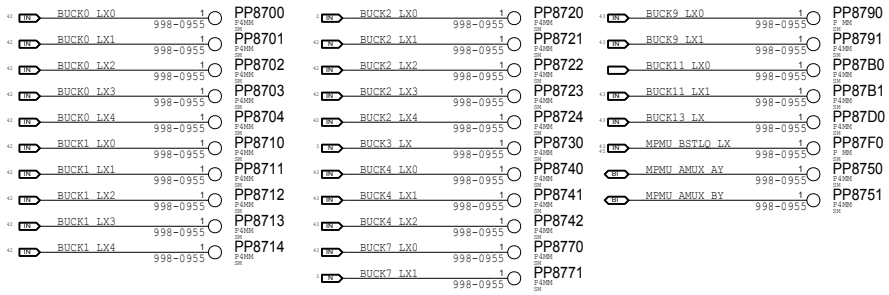
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OF AGREES TO THE FOLLOWING: THIS DOCUMENT CONFIDENCE NOT TO REPRODUCE OR COPY IN WHOLE OR PART. ALL RIGHTS RESERVED

www.repairlap.com

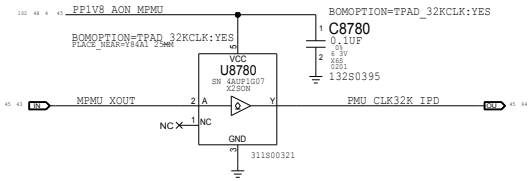
A MPMU Quiet GND Connections



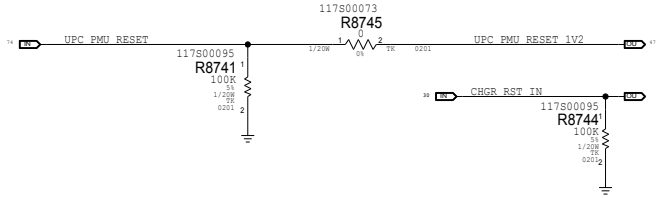
B MPMU Probe Points



D Buffer 32kHz Clock to Trackpad

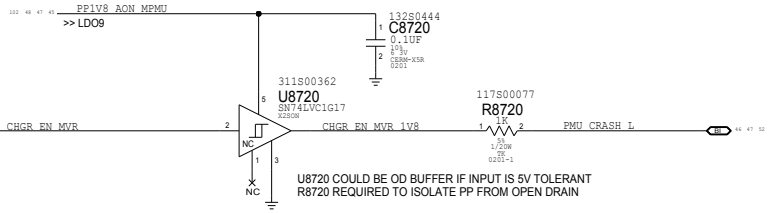


C MPMU Charger Reset Circuit



E Early Crash PMU signal

rdar /8 737 1



BOM_COST_GROUP=SOC POWER

PAGE TITLE
MPMU: SUPPORT

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS PROVIDED BY THE FOLLOWING
THIS DOCUMENT IS NOT TO BE REPRODUCED OR COPIED
IN WHOLE OR IN PART
ALL RIGHTS RESERVED

DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	87 OF 801
SHEET	48 OF 121

www.repairlap.com

A MPMU Misc Aliases

44	PMU_RSLOC_RST_L	PMU_RSLOC_RST_L (MAKE_BASE=TRUE)	47 93 97
43	NC_MPMU_XIN	NC_MPMU_XIN (MAKE_BASE=TRU)	
44	SOC_WDOG	SOC_WDOG (MAKE_BASE=TRU)	7
44	SOC_SOCHOT_L	SOC_SOCHOT_L (MAKE_BASE=TRUE)	7
44	PMU_RESET_L	PMU_RESET_L (MAKE_BASE=TRUE)	7 97
44	PMU_ACTIVE_READY	PMU_ACTIVE_READY (MAKE_BASE=TRUE)	7 74 97 105
44	DBL_CLICK_DET	DBL_CLICK_DET (MAKE_BASE=TRU)	9
44	PMU_UPC_FORCE_DFU	PMU_UPC_FORCE_DFU (MAKE_BASE=TR E)	97 106
47 44	BUCK0_THERMAL_THROTTLE_L	BUCK0_THERMAL_THROTTLE_L (MAKE_BASE=TRUE)	9
47 44	BUCK1_THERMAL_THROTTLE_L	BUCK1_THERMAL_THROTTLE_L (MAKE_BASE=TRUE)	9
47 44	TP_MPMU_THROTTLE2_L	TP_MPMU_THROTTLE2_L (MAKE_BASE=TRUE)	
47 44	PMU_VDDHI_UVWARN_L	PMU_VDDHI_UVWARN_L (MAKE_BASE=TRUE)	9
47 44	MPMU_VDDMAIN_UVWARN_L	MPMU_VDDMAIN_UVWARN_L (MAKE_BASE=TRUE)	9
37	MPMU_VDDMAIN_UVWARN_L		
44	NC_MPMU_VBUS_DET	NC_MPMU_VBUS_DET (MAKE_BASE=TRUE)	
44	GND	(MAKE_BASE=TRUE)	

B SPMU Misc Aliases

41 40	SPMU_VDDMAIN_UVWARN_L	SPMU_VDDMAIN_UVWARN_L (MAKE_BASE=TRUE)	SPMU_VDDMAIN_UVWARN_L 9
40	GND	(MAKE_BASE=T E)	

C PMU AMR Test

117S00073

R8820

0

05 IN AMR_1V8 — 1 — 2 — AMR_1V8_PMU OUT 47

0%
1/20W
TK
0201

BOM_COST_GROUP=SOC POWER

PAGE TITLE

PMU: SUPPORT - FF

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 88 OF 801

SHEET 49 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING
THIS DOCUMENT CONFIDENCE
NOT TO REPRODUCE OR COPY
NOR TO REVEAL PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

Intentionally Blank

PAGE TITLE

Apple Inc.

DRAWING NUMBER 051-09343

SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 121 OF 801

SHEET 50 OF 121

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT WHERE THE PARTIES OR AGREES TO THE FOLLOWING

I. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II. NOT TO REPRODUCE OR COPY IT

III. NOT TO RELEASE PUBLISH IT IN WHOLE OR PART

IV. ALL RIGHTS RESERVED

www.repairlap.com

* OK2INTEGRATE *

5V_S2 voltage regulator (Low power option)

SET ONE OPTION FOR THE MLCC CAPS

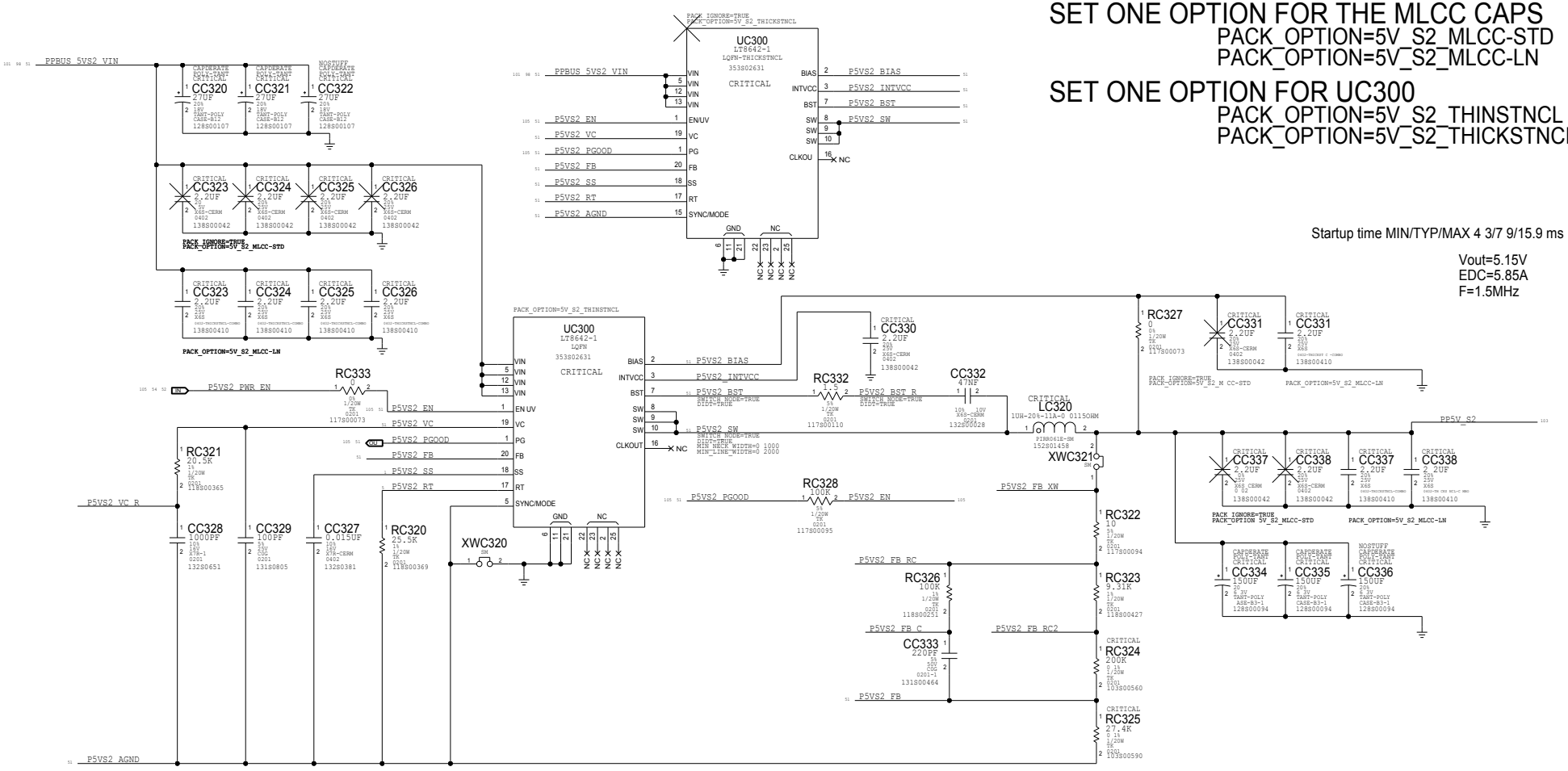
PACK_OPTION=5V_S2_MLCC-STD
PACK_OPTION=5V_S2_MLCC-LN

SET ONE OPTION FOR UC300

PACK_OPTION=5V_S2_THINSTNCL
PACK_OPTION=5V_S2_THICKSTNCL

Startup time MIN/TYP/MAX 4 3/7 9/15.9 ms

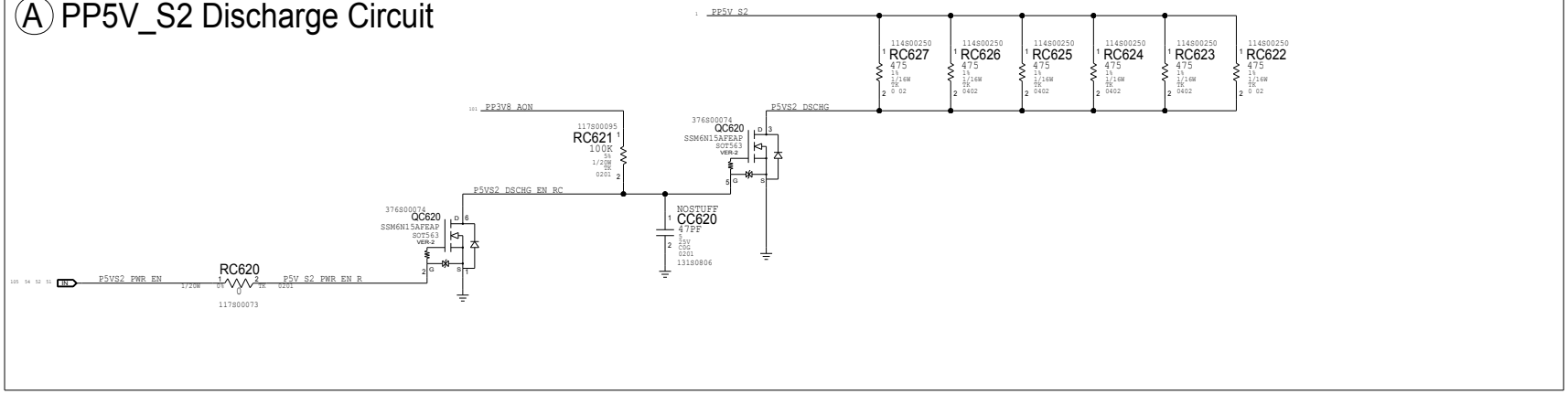
Vout=5.15V
EDC=5.85A
F=1.5MHz



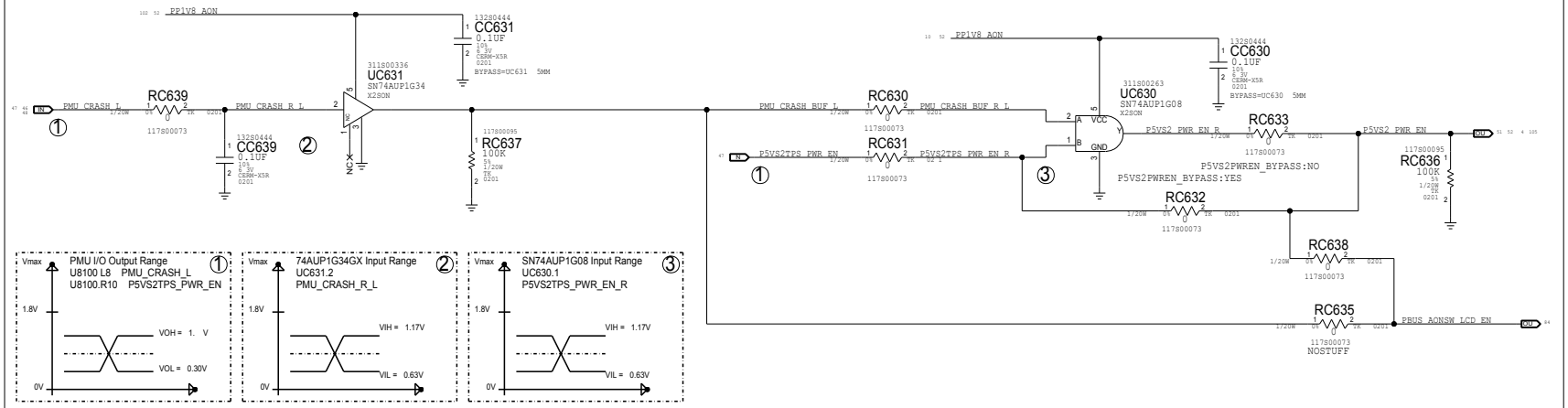
PAGE TITLE	POWER: 5V S2
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 123 OF 801
	SHEET 51 OF 121

www.repairlap.com

A PP5V_S2 Discharge Circuit



B P5VS2_PWR_EN Control Logic



BOM_COST_GROUP=PLATFORM POWER

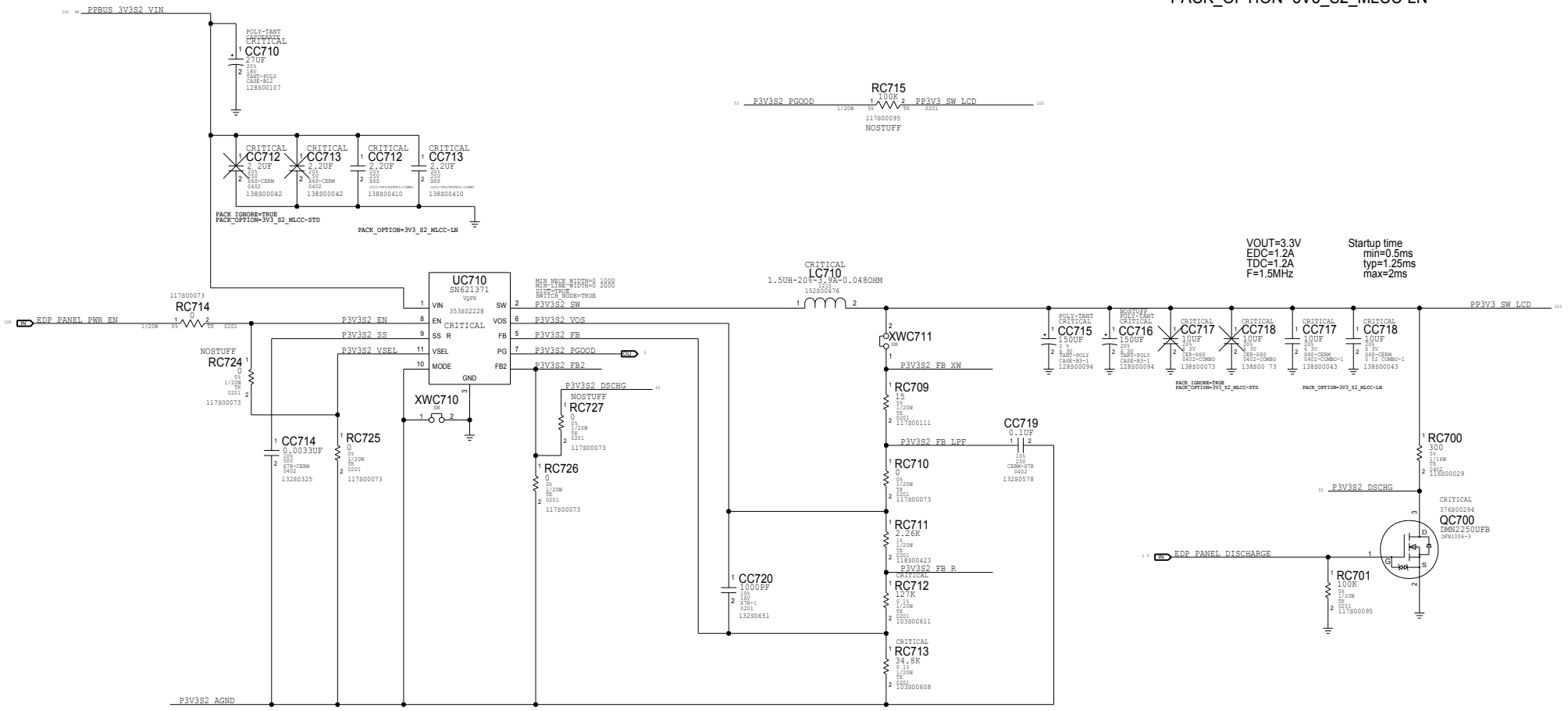
PAGE TITLE	POWER: 5V, 3V3 Support
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 126 OF 801
	SHEET 52 OF 121

www.repairlap.com

* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR MLCC CAPS
PACK_OPTION=3V3_S2_MLCC-STD
PACK_OPTION=3V3_S2_MLCC-LN



BOM_COST_GROUP=PLATFORM POWER

POWER: 3V3 S2

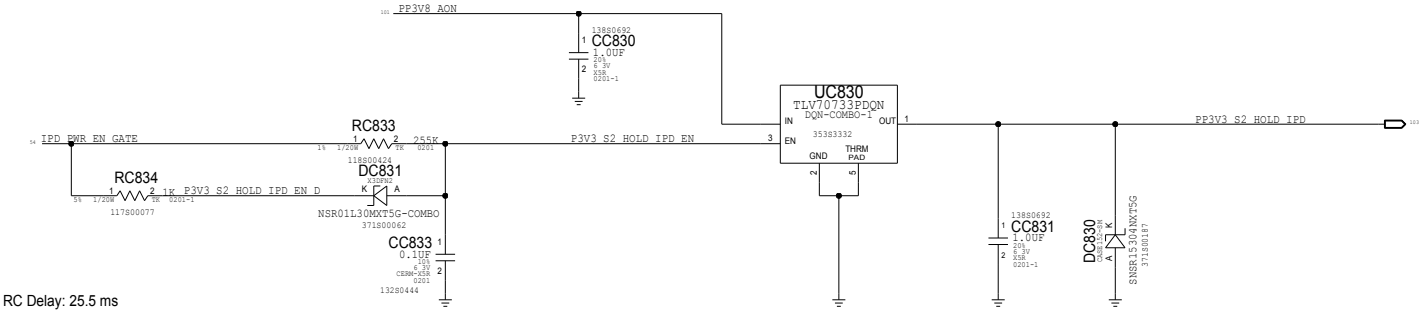
Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 127 OF 801
SHEET 53 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO BY THE FOLLOWING THIS DOCUMENT CONTAINS CONFIDENCE INFORMATION. NO REPRODUCE OR COPY IN WHOLE OR PART WITHOUT PRIOR WRITTEN PERMISSION. ALL RIGHTS RESERVED.

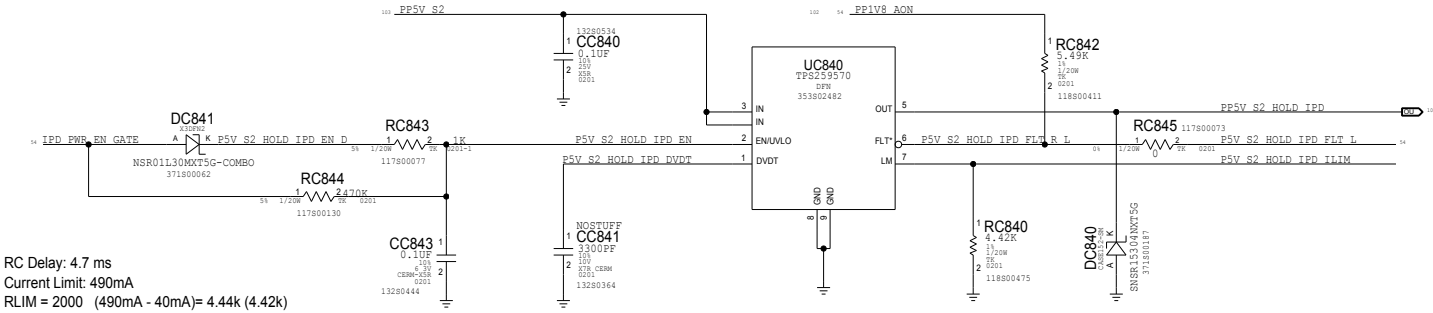
www.repairlap.com

A PP3V3_S2_HOLD_IPD LDO



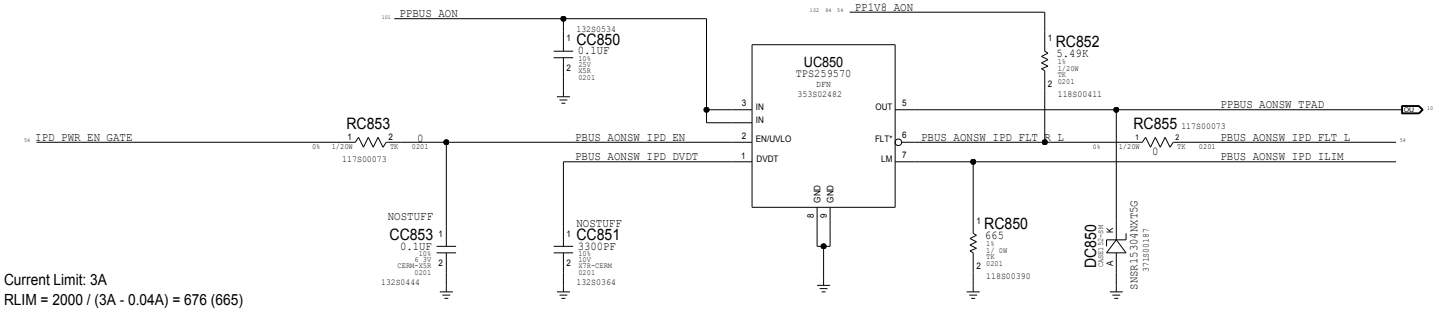
RC Delay: 25.5 ms
Current Limit: 350mA
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X2203GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

B PP5V_S2_HOLD_IPD Load Switch & e-Fuse



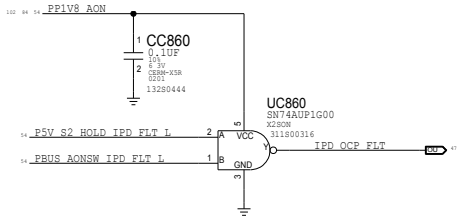
RC Delay: 4.7 ms
Current Limit: 490mA
RLIM = 2000 (490mA - 40mA)= 4.44k (4.42k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X2203GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

C PPBUS_AONSW_IPD Load Switch & e-Fuse

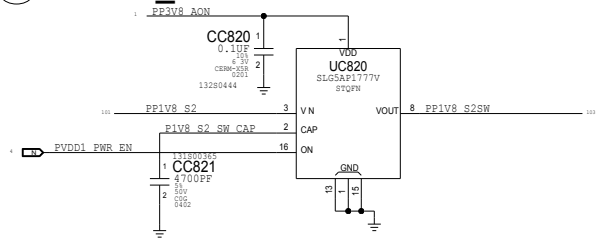


Current Limit: 3A
RLIM = 2000 / (3A - 0.04A) = 676 (665)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))

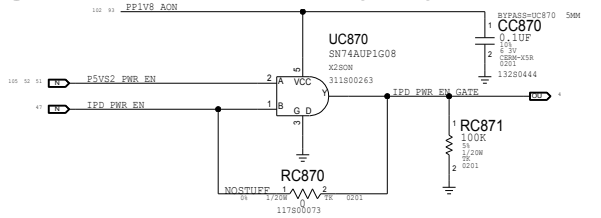
D IPD_OCP_FLT Control Logic



E PP1V8_S2SW Load Switch



F IPD_PWR_EN Gating Logic



BOM_COST_GROUP=PLATFORM_POWER

10/25/2022

PAGE TITLE: Power: Load Switches

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D
REVISION: 5.0.0
BRANCH: dvt-1
PAGE: 128 OF 801
SHEET: 54 OF 121

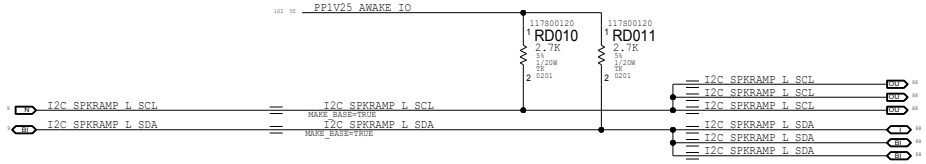
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE STATED HEREIN, THE RECEIPT OF THIS DOCUMENT OR THE INFORMATION CONTAINED HEREIN DOES NOT CONFER OR IMPLY TO THE RECEIPT OR ANY OTHER PERSON OR ENTITY THE RIGHT TO REPRODUCE OR COPY, REPRODUCE, REPUBLISH, OR PUBLISH IN WHOLE OR PART, ALL RIGHTS RESERVED.

www.repairlap.com

A AP_I2C0 - I2C Interface (Unused)

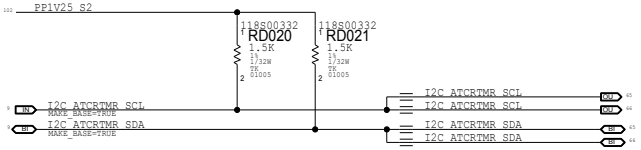
B AP_I2C1 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	1	400 kHZ	0X38	0X71	Left SpkrAmp A
AP	1	400 kHZ	0X39	0X73	Left SpkrAmp B
AP	1	400 kHZ	0X3A	0X75	Left SpkrAmp C



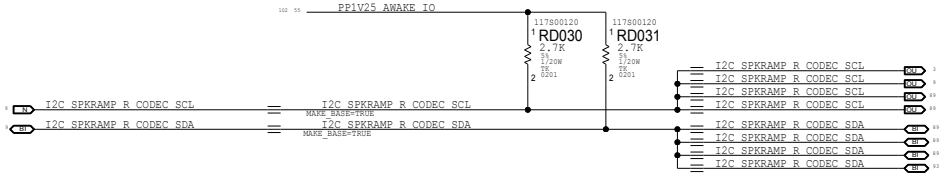
C AP_I2C2 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	2	100 kHZ/400 kHz	0X18	0X31	RT13 Port 0
AP	2	100 kHZ/400 kHz	0X19	0X33	RT13 Port 1



D AP_I2C3 - I2C Interface

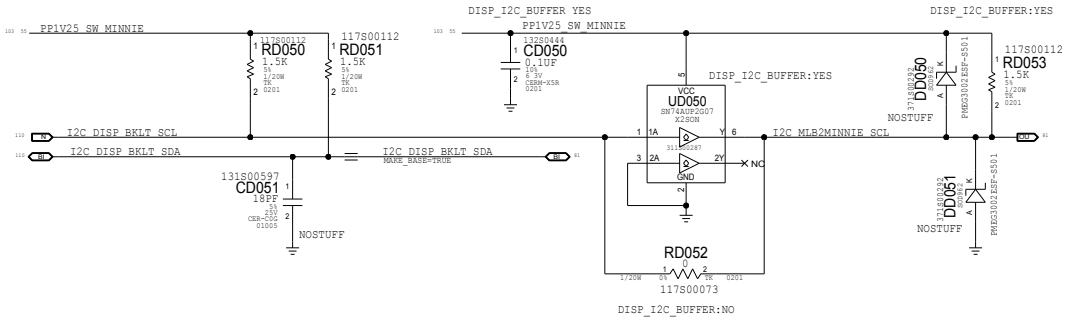
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	3	400 kHZ	0X3B	0X77	Right SpkrAmp D
AP	3	400 kHZ	0X3C	0X79	Right SpkrAmp E
AP	3	400 kHZ	0X3D	0X7B	Right SpkrAmp F
AP	3	400 kHZ	0X4B	0X97	CODEC



E AP_I2C4 - I2C Interface (Unused)

F DISP_I2C - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
DISP	0	100 kHZ	0X2F	0X5F	Minnie Bklt Drvr



BOM_COST_GROUP=SENSORS

PAGE TITLE: I2C: AP, DISP

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 130 OF 801

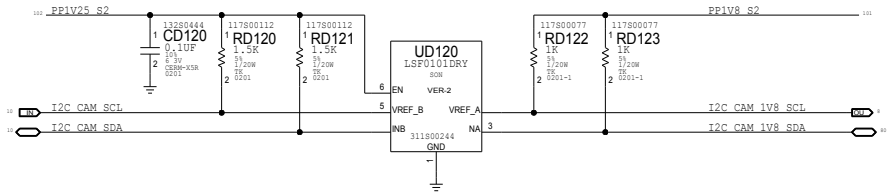
SHEET: 55 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: THIS DOCUMENT CONFIDENTIAL. NO REPRODUCE OR COPY. NO TRANSMIT OR PUBLISH IN WHOLE OR PART. ALL RIGHTS RESERVED.

www.repairlap.com

A ISP_I2C0 - I2C Interface

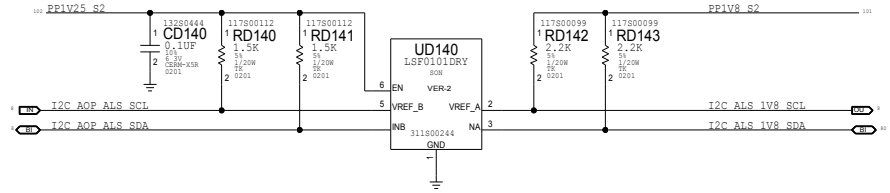
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
ISP	0	400 kHz	0X10	0X21	Camera PMIC
ISP	0	400 kHz	0X36	0X6D	Image Sensor



B ISP_I2C1 - I2C Interface (Unused)

C AOP_I2CM0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AOP	0	400 kHz	0X48	0X91	TMP108
AOP	0	400 kHz	0X29	0X53	TETRA2 ALS



D AOP_I2CM1 - I2C Interface (Unused)

E AOP_I2CM2 - I2C Interface (Unused)

F SEP_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SEP	0	400 kHz/1 MHz	0X71	0XE3	SEP Custom App
SEP	0	400 kHz/1 MHz	0X51	0XA3	SEP EEPROM App

I2C Pull-Ups at EEPROM (U1950)

BOM_COST_GROUP=SENSORS

PAGE TITLE: I2C: ISP, AOP, SEP

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 131 OF 801

SHEET: 56 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: (I) TO MAINTAIN IS DOCUMENT IN CONFIDENCE; (II) NOT TO REPRODUCE OR COPY IT; (III) NOT TO RELEASE, PUBLISH IT IN WHOLE OR PART; (IV) ALL RIGHTS RESERVED.

www.repairlap.com

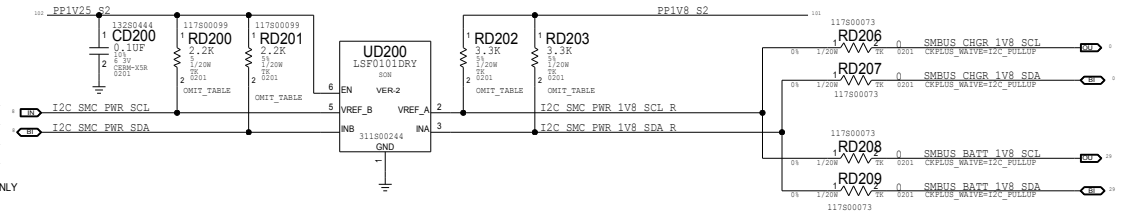
A SMC_I2C0 - I2C Interface (Unused)

I2CM0 Aliases on CSA 406

B SMC_I2C1 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEV CE
SMC	1	100 kHz	0X09	0X13	Mandola Charger
SMC	1	100 kHz	0X0B	0X17	Battery BMU
SMC	1	100 kHz	0X40	0X81	INA233 - U201
SMC	1	100 kHz	0X44	0X89	INA233 - U202
SMC	1	100 kHz	0X40	0X81	INA236 - U201
SMC	1	100 kHz	0X41	0X83	INA236 - U202
SMC	1	100 kHz	0X42	0X85	INA236 - U203
SMC	1	100 kHz	0X43	0X87	INA236 - U204
SMC	1	100 kHz	0X20	0X41	SMC Fixture IO Expander

INY ONLY
TINY ONLY
MEGA ONLY
MEGA ONLY
MEGA ONLY
MEGA ONLY
FACTORY ONLY

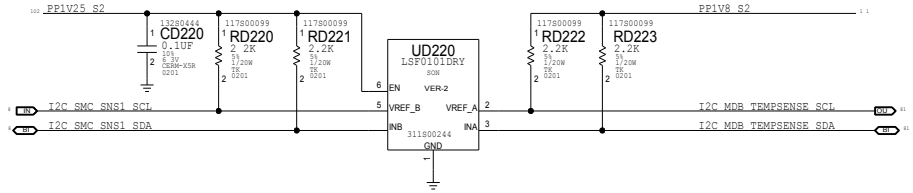


PAR #	Q	DESCRIP ON	REFERENCE DES GNA OR S)	BOM OP ION
117800099	2	RES,TK,2 2K OHM,5%,1/20W,0201	RD200,RD201	I2C_PWR_PU TINY
117800123	2	RES,TK,3 3K OHM,5%,1/20W,0201	RD202,RD203	I2C_PWR_PU TINY

PAR #	Q	DESCR P ON	REFERENCE DES GNA OR( )	BOM OP ION
117800090	2	RES TK,10K OHM,5%,1/20W,0201	RD200,RD201	I2C_PWR_PU MEGA
117800087	2	RES,TK,4 7K OHM,5%,1/20W,0201	RD202,RD203	I2C_PWR_PU MEGA

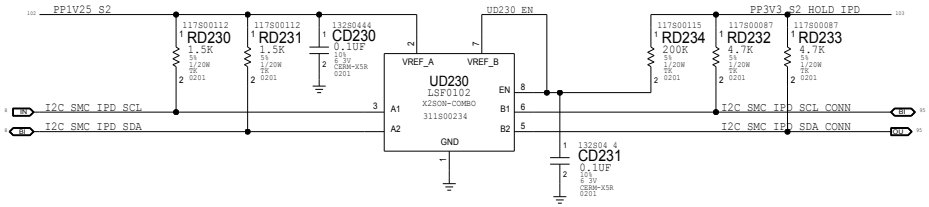
C SMC_I2C2 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	2	100 kHz	0X48	0X91	MDB - TMP468

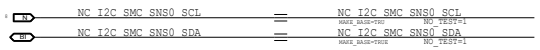


D SMC_I2C3 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	3	100 kHz	0X4C	0X99	PALM - TempSense



E SMC_I2C4 - I2C Interface (Unused)



BOM_COST_GROUP=SENSORS

PAGE TITLE: I2C: SMC

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 132 OF 801

SHEET: 57 OF 121

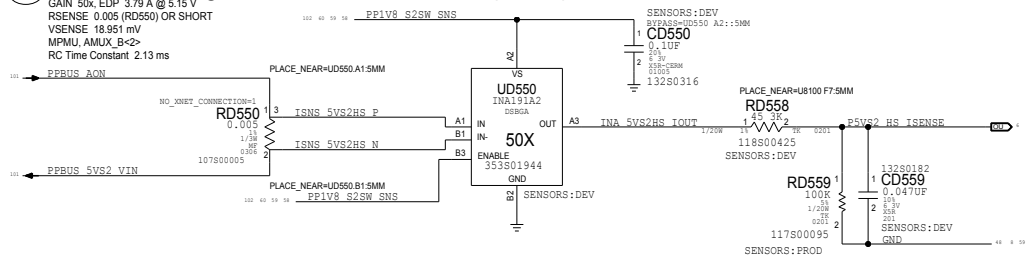
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO IN THE FOLLOWING WRITTEN DOCUMENT, THIS DOCUMENT CONTAINS CONFIDENCE
NOT TO BE REPRODUCED OR COPIED
NOT TO BE RELEASED OR PUBLISHED IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

A 5V S2 VR High Side Current Sensor (IO5R)

GAIN 50x, EDP 3.79 A @ 5.15 V
RSENSE 0.005 (RD550) OR SHORT
VSENSE 18.951 mV
MPMU, AMUX_B<2>
RC Time Constant 2.13 ms

LTSpice:

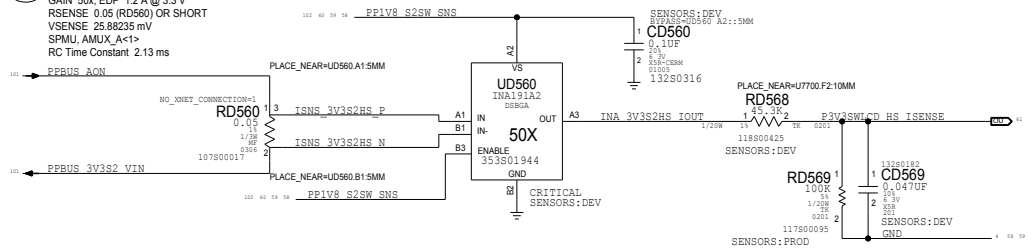


$X2203GHUB/mlb/sim/ltspice/io5r_p5vs2_hs_isense/io5r_p5vs2_hs_isense.asc

B 3V3 SW LCD VR High Side Current Sensor (IO3R)

GAIN 50x, EDP 1.2 A @ 3.3 V
RSENSE 0.05 (RD560) OR SHORT
VSENSE 25.88235 mV
SPMU, AMUX_A<1>
RC Time Constant 2.13 ms

LTSpice:

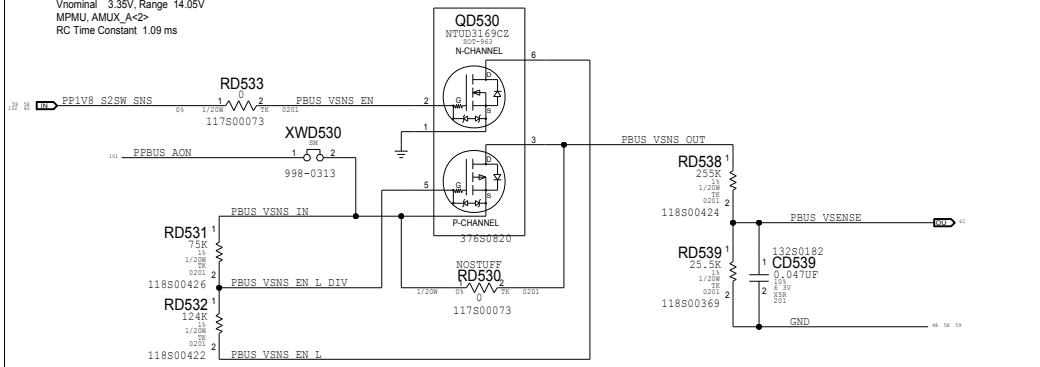


$X2203GHUB/mlb/sim/ltspice/io3r_p3v3s2_hs_isense/io3r_p3v3s2_hs_isense asc

C PPBUS Voltage Sensor (VP0R)

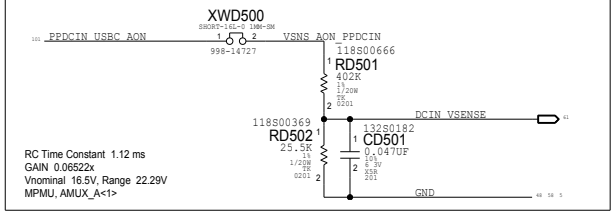
GAIN 0 10119x
Vnominal 3.35V, Range 14.05V
MPMU, AMUX_A<2>
RC Time Constant 1.09 ms

LTSpice:



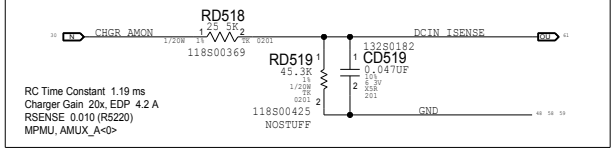
$X2203GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_diodesinc.asc
$X2203GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_onsemi.asc

D DCIN Voltage Sensor (VD0R)



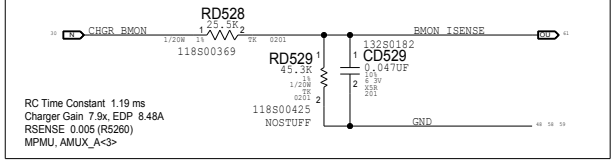
RC Time Constant 1.12 ms
GAIN 0.06522x
Vnominal 16.5V, Range 22.29V
MPMU, AMUX_A<1>

E DCIN Current Sensor (ID0R)



RC Time Constant 1.19 ms
Charger Gain 20x, EDP 4.2 A
RSENSE 0.010 (R5220)
MPMU, AMUX_A<0>

F BMON Current Sensor (IPBR)



RC Time Constant 1.19 ms
Charger Gain 7.9x, EDP 8.48A
RSENSE 0.005 (R5260)
MPMU, AMUX_A<3>

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER HIGH SIDE (1/2)

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO THE FOLLOWING
1. DO NOT COPY
2. DO NOT REPRODUCE OR COPY
3. DO NOT RELEASE PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

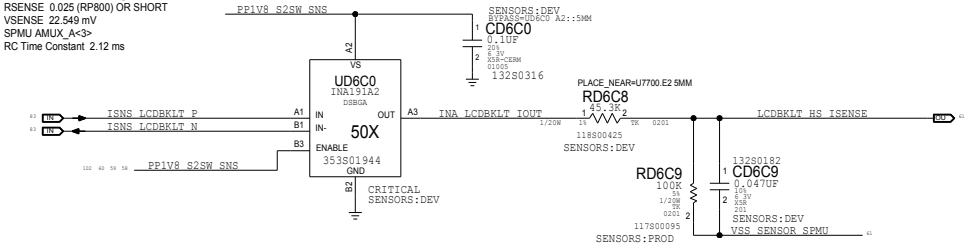
DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	135 OF 801
SHEET	58 OF 121

www.repairlap.com

A LCD Backlight High Side Current Sensor (IBLR)

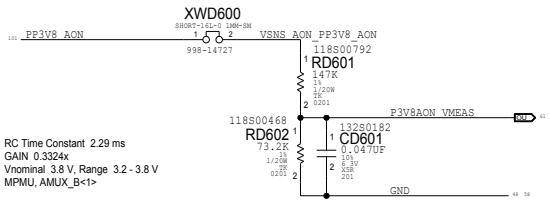
LTSpice:

GAIN 50X, EDP 0.150 A @ 46 V
RSENSE 0.025 (RP800) OR SHORT
VSENSE 22.549 mV
SPMU AMUX_A<3>
RC Time Constant 2.12 ms



$X2203GHUB/mlb/sim/ltspice/iblr_lcdbklt_hs_isense/iblr_lcdbklt_hs_isense.asc

C Iceman Voltage Sensor (VMVC)



RC Time Constant 2.29 ms
GAIN 0.3324x
Vnominal 3.8 V, Range 3.2 - 3.8 V
MPMU, AMUX_B<1>

D Iceman LS Current Sensor (IMVC)

See CSA 59

RC Time Constant 21.22 ms
EDP 30 A
MPMU, AMUX_B<0>

BOM_COST_GROUP=SENSORS

PAGE TITLE	SENSORS: POWER HIGH SIDE (2/2)
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 136 OF 801
	SHEET 59 OF 121

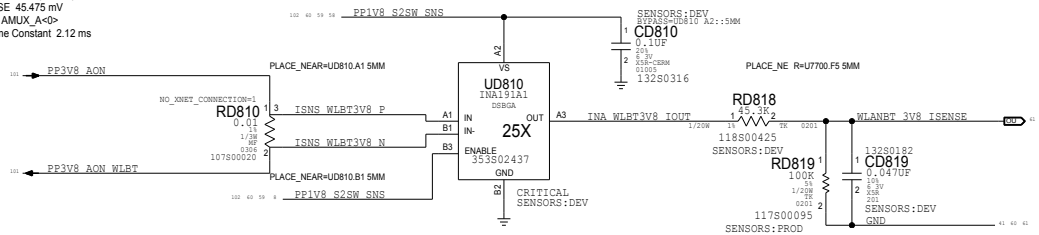
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (1) TO MAINTAIN IS DOCUMENT IN CONFIDENCE (2) NOT TO REPRODUCE OR COPY IT (3) NOT TO RELEASE OR PUBLISH IT IN WHOLE OR PART. ALL RIGHTS RESERVED.

www.repairlap.com

A WLAN BT 3V8 AON Current Sensor (IW3C)

LTSpice:

GAIN 25x, EDP 1.819 A @ 3.8 V
RSENSE 0.01 (RD810) OR SHORT
VSENSE 45.475 mV
SPMU AMUX_A<0>
RC Time Constant 2.12 ms

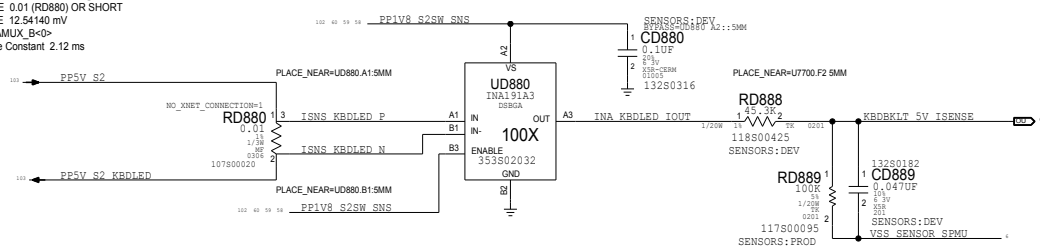


$X2203GHUB/mlb/sim/ltspice/iw3c_wlanbt_3v3_isense/iw3c_wlanbt_3v3_isense.asc

B Keyboard LED 5V Current Sensor (IKBC)

LTSpice:

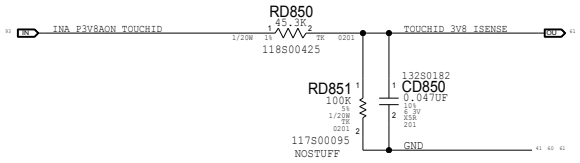
GAIN 100X, EDP 0.183 A @ 30 V
RSENSE 0.01 (RD880) OR SHORT
VSENSE 12.54140 mV
SPMU AMUX_B<0>
RC Time Constant 2.12 ms



$X2203GHUB/mlb/sim/ltspice/ikbc_kbdbklt_5v_isense/ikbc_kbdbklt_5v_isense asc

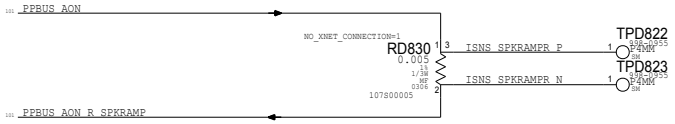
C TouchID Current Sensor (IIDR)

GAIN 200X, EDP 0.200 A @ 3.8 V
RSENSE 0.035 (RT505 on KBDB)
VSENSE 7.000 mV, Range 0.214 A
SPMU AMUX_A<2>
RC Time Constant 10 ms



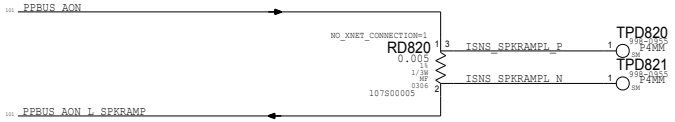
D Right Speaker Amplifier Current Sensor (Ixxx)

GAIN 100X, EDP 2.6 A
RSENSE 0.005 (RD820) OR SHORT
VSENSE 13 mV, RANGE 3.3 A



E Left Speaker Amplifier Current Sensor (Ixxx)

GAIN 100X, EDP 2.6 A
RSENSE 0.005 (RD820) OR SHORT
VSENSE 13 mV, RANGE 3.3 A



BOM_COST_GROUP=SENSORS

10/26/2022

PAGE TITLE: SENSORS: POWER LOW SIDE

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 138 OF 801

SHEET: 60 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING
1. COMMUNICATION DOCUMENT CONFIDENCE
2. NO REPRODUCE OR COPY
3. NO REVEAL PUBLISH IN WHOLE OR PART
4. ALL RIGHTS RESERVED

www.repairlap.com

A ADC Input Aliases

LEADER PMU AMUX ALIAS

DCIN_ISENSE	MAKE_BASE=TRUE	=	DCIN_ISENSE
DCIN_VSENSE	MAKE_BASE=TRUE	=	DCIN_VSENSE
PBUS_VSENSE	MAKE_BASE=TRUE	=	PBUS_VSENSE
BMON_ISENSE	MAKE_BASE=TRUE	=	BMON_ISENSE
P3V8AON_IMEAS	MAKE_BASE=TRUE	=	P3V8AON_IMEAS
P3V8AON_VMEAS	MAKE_BASE=TRUE	=	P3V8AON_VMEAS
P5VS2_HS_ISENSE	MAKE_BASE=TRUE	=	P5VS2_HS_ISENSE
MPMU_OPENL_LPF	MAKE_BASE=TRUE	=	MPMU_OPENL_LPF

FOLLOWER PMU AMUX ALIAS

WLANBT_3V8_ISENSE	MAKE_BASE=TRUE	=	WLANBT_3V8_ISENSE
P3V3SWLCD_HS_ISENSE	MAKE_BASE=TRUE	=	P3V3SWLCD_HS_ISENSE
TOUCHID_3V8_ISENSE	MAKE_BASE=TRUE	=	TOUCHID_3V8_ISENSE
LCDBKLT_HS_ISENSE	MAKE_BASE=TRUE	=	LCDBKLT_HS_ISENSE
KBDBKLT_5V_ISENSE	MAKE_BASE=TRUE	=	KBDBKLT_5V_ISENSE
SPMU_AMUXTDEV_TERM	MAKE_BASE=TRUE	=	SPMU_AMUXTDEV_TERM
SPMU_AMUXTDEV_TERM	MAKE_BASE=TRUE	=	SPMU_AMUXTDEV_TERM
SPMU_OPENL_LPF	MAKE_BASE=TRUE	=	SPMU_OPENL_LPF

B SOC Sense Lines

VSNS_ABSMIN_PCPU	MAKE_BASE=TRUE	=	PPE0A8 (P4MM, SM)	998-0955
VSNS_VSS_1	MAKE_BASE=TRUE	=	PPE0A9 (P4MM, SM)	998-0955
VSNS_VDD2H_1	MAKE_BASE=TRUE	=	PPE0AA (P4MM, SM)	998-0955
VSNS_VSS_2	MAKE_BASE=TRUE	=	PPE0AB (P4MM, SM)	998-0955
VSNS_VDD2H_2	MAKE_BASE=TRUE	=	PPE0AC (P4MM, SM)	998-0955
VSNS_VDDQ_S1	MAKE_BASE=TRUE	=	PPE0AD (P4MM, SM)	998-0955
VSNS_VDD_PCPU	MAKE_BASE=TRUE	=	PPE0A1 (P4MM, SM)	998-0955
VSNS_VSS_PCPU	MAKE_BASE=TRUE	=	PPE0A2 (P4MM, SM)	998-0955
VSNS_VDD_GPU	MAKE_BASE=TRUE	=	PPE0A3 (P4MM, SM)	998-0955
VSNS_VSS_GPU	MAKE_BASE=TRUE	=	PPE0A4 (P4MM, SM)	998-0955
VSNS_VDD_SOC	MAKE_BASE=TRUE	=	PPE0A5 (P4MM, SM)	998-0955
VSNS_VDD_ECPU	MAKE_BASE=TRUE	=	PPE0A6 (P4MM, SM)	998-0955
VSNS_VDD_DISP	MAKE_BASE=TRUE	=	PPE0A7 (P4MM, SM)	998-0955

998-0955 PPE0AE (P4MM, SM) — PLACE_NEAR=PPE0A3:2MM

998-0955 PPE0AF (P4MM, SM)

C Unused MPMU AMUX/TDEV Termination

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.

MPMU_AMUXTDEV_TERM = MPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)

RE010 100K 5% 1/20W 75 0201 117S00095

D Unused SPMU AMUX/TDEV Termination

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.

SPMU_AMUXTDEV_TERM
SPMU_AMUXTDEV_TERM
SPMU_AMUXTDEV_TERM
SPMU_AMUXTDEV_TERM
= SPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)

RE020 100K 5% 1/20W 75 0201 117S00095

E I/V Sensor Ground Reference Aliases

FOLLOWER PMU ADC Ground Alias

VSS_SENSOR_SPMU
VSS_SENSOR_SPMU
= VSS_SENSOR_SPMU (MAKE_BASE=TRUE) — XWE020 (SM, 998-0313) — GND

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: POWER SUPPORT

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 140 OF 801

SHEET: 61 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. BY ACCEPTANCE OF THE FOLLOWING THE RECIPIENT AGREES TO THE FOLLOWING
1. THIS DOCUMENT CONTAINS CONFIDENCE
2. NO REPRODUCE OR COPY
3. NO OTHER USE, PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

A Leader PMU TDEV1 (Txxx)

MPMU_AMUXTDEV_TERM — MPMU_AMUXTDEV_TERM

B Leader PMU TDEV2 (Tm0B)

Location: Ambient

THMSNS_MPMU2_P — XWE121 — MPMU_TDEV2

107S00460 RE121 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE121.1:2MM 131S0805 CE121 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.F13:5MM

THMSNS_MPMU2_N — XWE122 — THMSNS_MPMU_VSS

C Leader PMU TDEV3 (TIOP)

Location: Thunderbolt Proximity

THMSNS_MPMU3_P — XWE131 — MPMU_TDEV3

107S00460 RE131 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE131.1:2MM 131S0805 CE131 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.F9:5MM

THMSNS_MPMU3_N — XWE132 — THMSNS_MPMU_VSS

D Leader PMU TDEV4 (TW0P)

Location: Wireless Proximity

THMSNS_MPMU4_P — XWE141 — MPMU_TDEV4

107S00460 RE141 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE1 1.1:2MM 131S0805 CE141 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.F10:5MM

THMSNS_MPMU4_N — XWE142 — THMSNS_MPMU_VSS

E Leader/Follower PMU VSS Connection

PLACE_NEAR=U8100.J11:5MM

XWE100

THMSNS_MPMU_VSS — GND_TCAL_MPMU

998-0313

PLACE_NEAR=U7700.C6:5MM

XWE1A0

THMSNS_SPMU_VSS — GND_TCAL_SPMU

998-0313

F Leader PMU TDEV5 (TPMP)

Location: Leader PMU Proximity

MPMU_TDEV5

107S00460 RE151 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=U81 0.F11:5MM 131S0805 CE151 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1

GND_TCAL_MPMU

G Leader PMU TDEV6 (T5SP)

Location: PP5V_S2 (UC300)

THMSNS_MPMU6_P — XWE161 — MPMU_TDEV6

107S00460 RE161 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE161. :2MM 131S0805 CE161 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.F12:5MM

THMSNS_MPMU6_N — XWE162 — THMSNS_MPMU_VSS

H Leader PMU TDEV7 (TCHP)

Location: Charger Proximity

THMSNS_MPMU7_P — XWE171 — MPMU_TDEV7

107S00460 RE171 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE171.1:2MM 131S0805 CE171 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.G9:5MM

THMSNS_MPMU7_N — XWE172 — THMSNS_MPMU_VSS

I Leader PMU TDEV8 (TMVR)

Location: Main VR (PP3V8_AON_VDDMAIN)

THMSNS_MPMU8_P — XWE181 — MPMU_TDEV8

107S00460 RE181 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE181.1:2MM 131S0805 CE181 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.G8:5MM

THMSNS_MPMU8_N — XWE182 — THMSNS_MPMU_VSS

J Follower PMU TDEV1 (Txxx)

SPMU_AMUXTDEV_TERM — SPMU_AMUXTDEV_TERM

K Follower PMU TDEV2 (TH0T)

Location: NAND Proximity

THMSNS_SPMU2_P — XWE1C1 — SPMU_TDEV2

107S00460 RE1C1 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE1C1. 2MM 131S0805 CE1C1 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U7700.J1: MM

THMSNS_SPMU2_N — XWE1C2 — THMSNS_SPMU_VSS

L Follower PMU TDEV3 (Txxx)

SPMU_AMUXTDEV_TERM — SPMU_AMUXTDEV_TERM

M Follower PMU TDEV4 (TSCD)

Location: SOC Proximity

THMSNS_SPMU4_P — XWE1E1 — SPMU_TDEV4

107S00460 RE1E1 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE1E1.1:2MM 131S0805 CE1E1 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U7700.G2:5MM

THMSNS_SPMU4_N — XWE1E2 — THMSNS_SPMU_VSS

N Follower PMU TDEV5 (TPSP)

Location: Follower PMU Proximity

THMSNS_SPMU5_P — XWE1F1 — SPMU_TDEV5

107S00460 RE1F1 10K-1% 0201-2 NO_XNET_CONNECTION=1

PLACE_NEAR=XWE1F1.1:2MM 131S0805 CE1F1 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 PLACE_NEAR=U7700.J2:5MM

THMSNS_SPMU5_N — XWE1F2 — THMSNS_SPMU_VSS

BOM_COST_GROUP=SENSORS

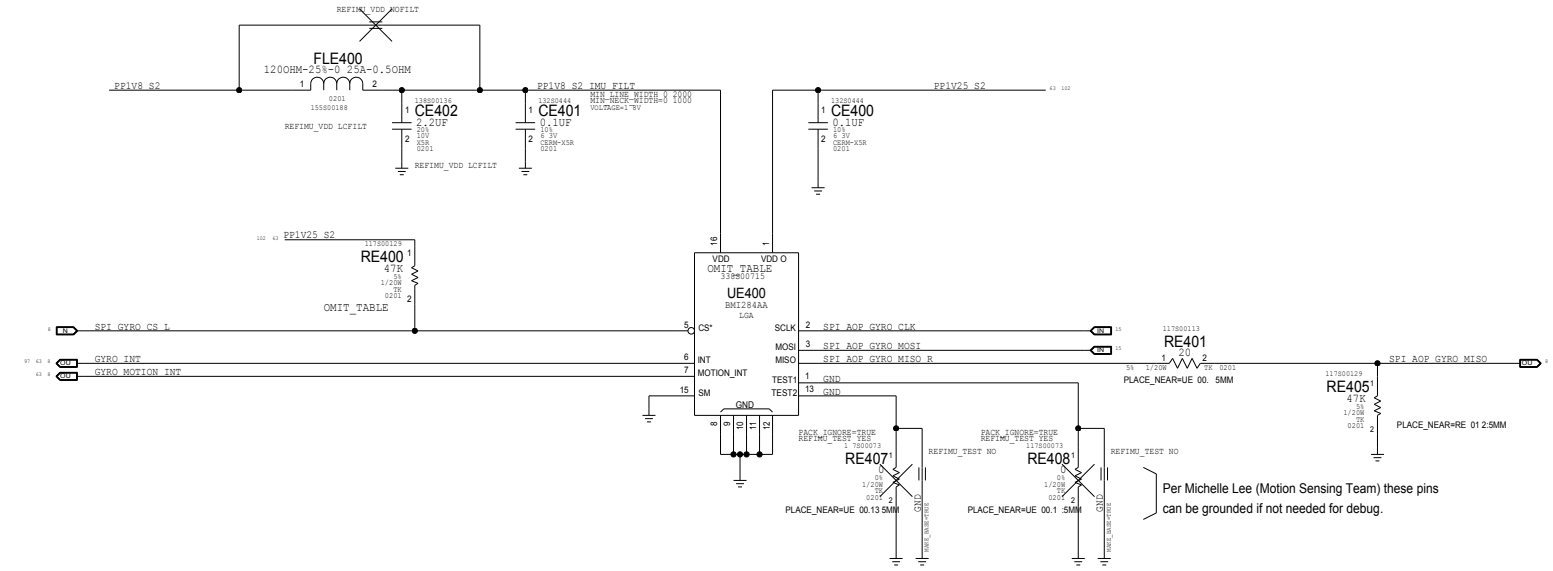
PAGE TITLE	SENSORS: THERMAL
Apple Inc.	DRAWING NUMBER 051-09343 — SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: 1. TO MAINTAIN IN DOCUMENT IN CONFIDENCE. 2. NO REPRODUCE OR COPY. 3. NO OTHER USE. PUBLISH IN WHOLE OR PART. ALL RIGHTS RESERVED	BRANCH dvt-1
	PAGE 141 OF 801
	SHEET 62 OF 121

www.repairlap.com

*** OK2INTEGRATE ***

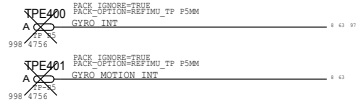
A Sovereign Accelerometer and Gyroscope

Datasheet Radar:



MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: https://www.bosch-sensortec.com/products/motion-sensors/imus/
Radar: rdar://61521702 (Sovereign: Datasheet)

B Test Points



C Sovereign BOM Options

PART #	Q	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC,SOVEREIGN,BMI284,AA,LGA16	UE400	CRITICAL	REFIMU_IC BMI284
338S00849	1	IC,SOVEREIGN2,BMI286,AA,LGA16	UE400	CRITICAL	REFIMU_IC BMI286
117S00129	1	RES,TK,47K OHM,5%,1/20W,0201	RE400	CRITICAL	REFIMU_RE400 47K
118S00521	1	RES,TK,30K OHM,1%,1/20W,0201	RE400	CRITICAL	REFIMU_RE400 30K

PAGE TITLE: SENSORS: MOTION

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

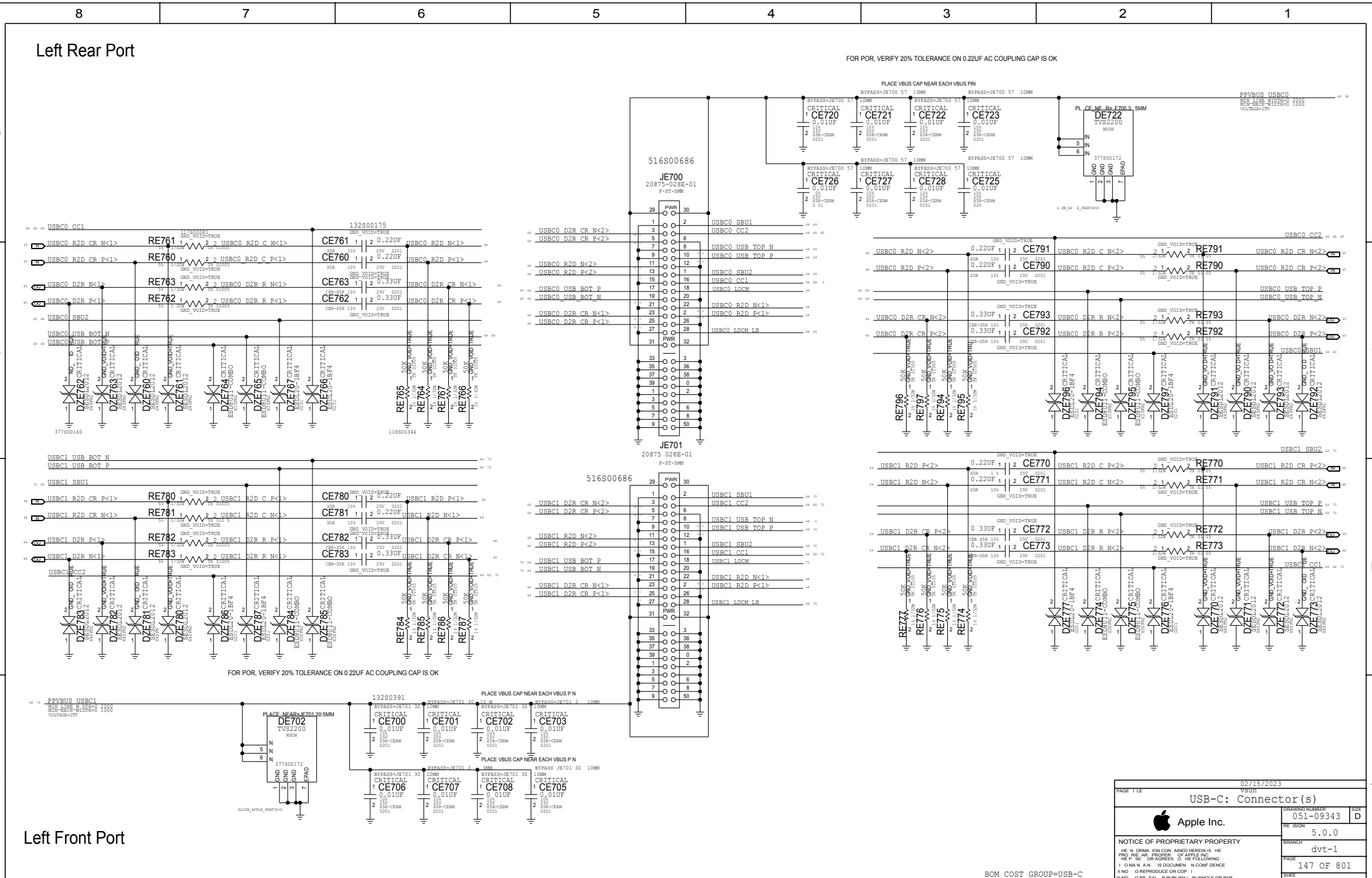
BRANCH: dvt-1

PAGE: 144 OF 801

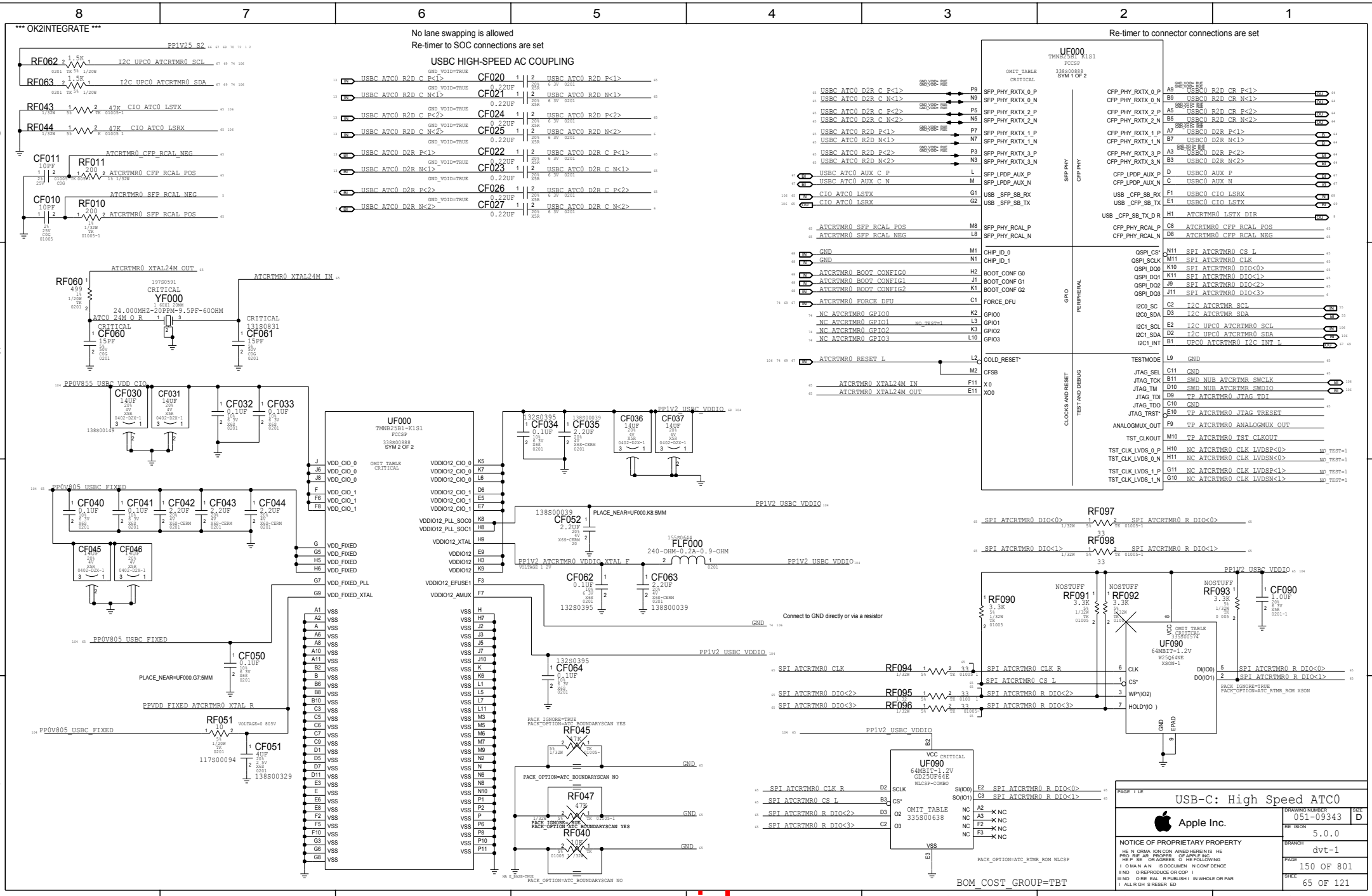
SHEET: 63 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT WHERE OTHERWISE AGREED TO IN WRITING THE FOLLOWING INFORMATION IS DOCUMENT CONFIDENTIAL. (I) NO REPRODUCTION OR COPY, (II) NO DISCLOSURE TO ANY THIRD PARTY, (III) NO PUBLICATION IN WHOLE OR PART. ALL RIGHTS RESERVED.

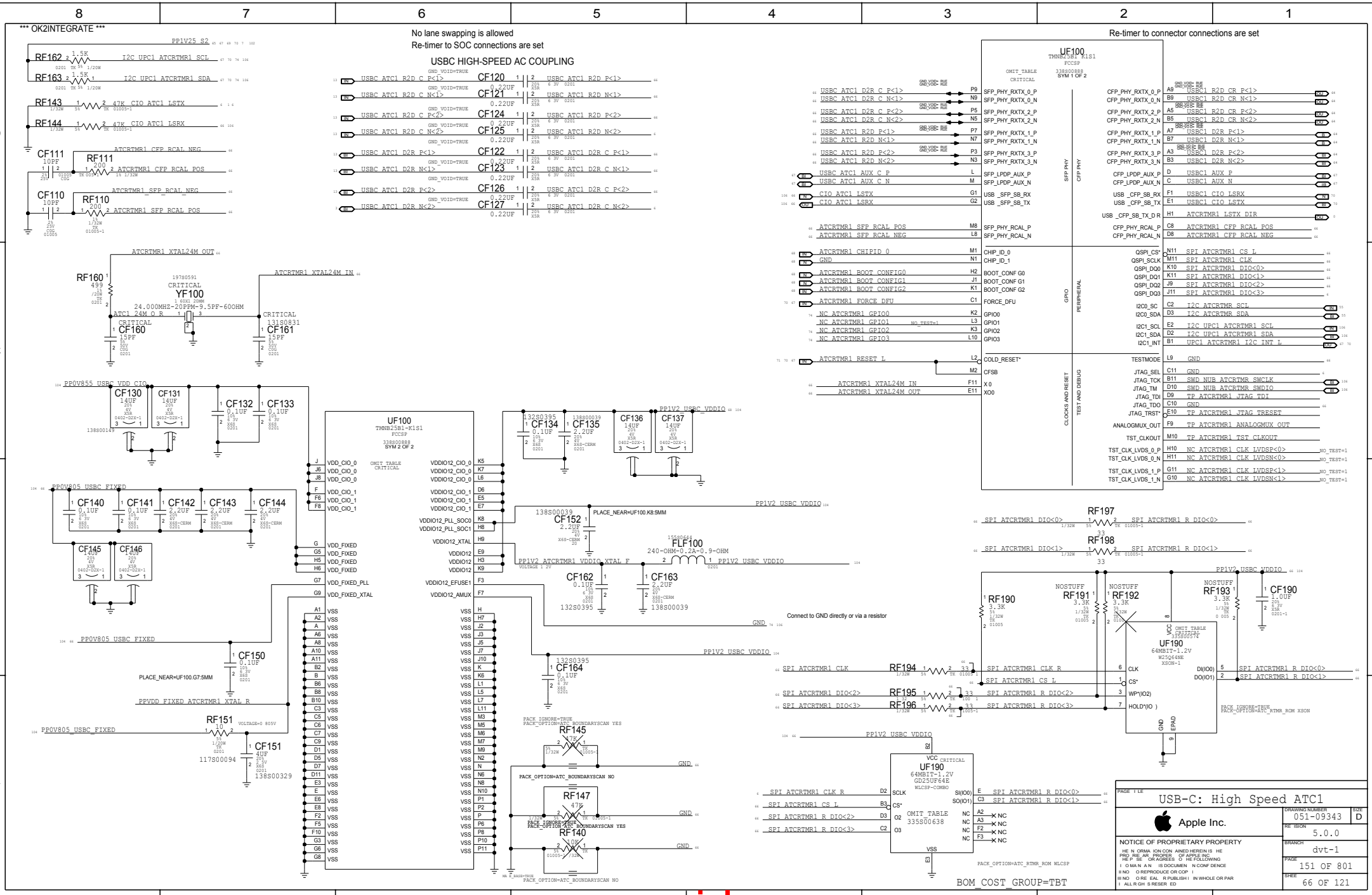
www.repairlap.com



www.repairlap.com

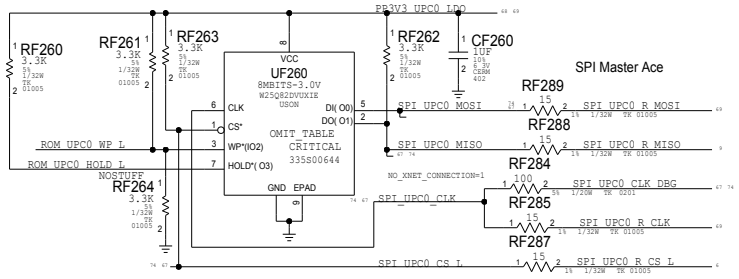


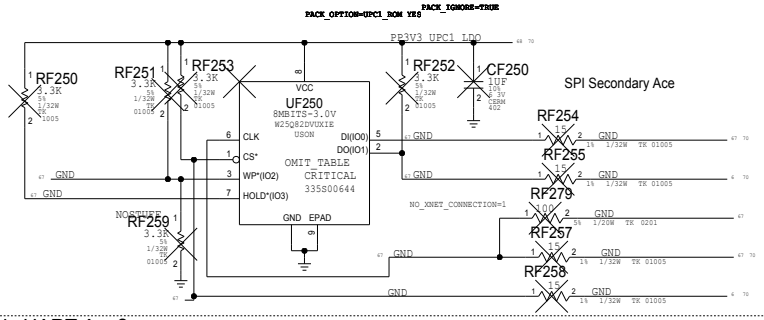
www.repairlap.com



www.repairlap.com

*** REFERENCE ONLY ***





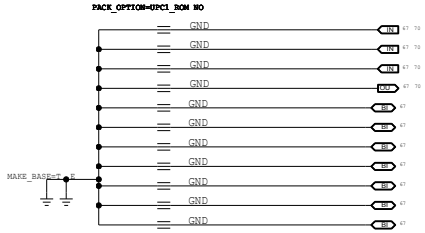
UPC1 Dedicated ROM and UART Debug chain possible pack_options:

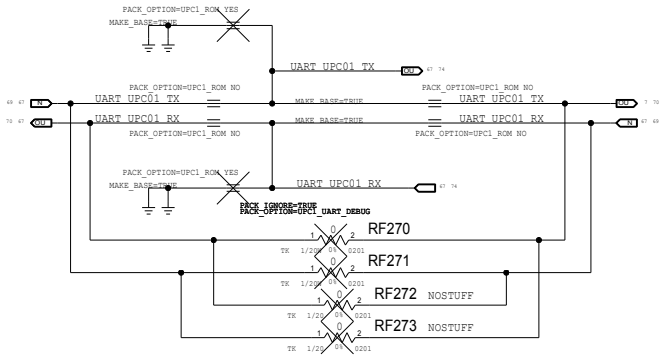
1. UPC1 may need its own ROM and need a fall-back method to no ROM for UPC1
   pick: "UPC1_ROM:YES" , "UPC1_UART_DEBUG" and "UPC1_UART_PD:NO"

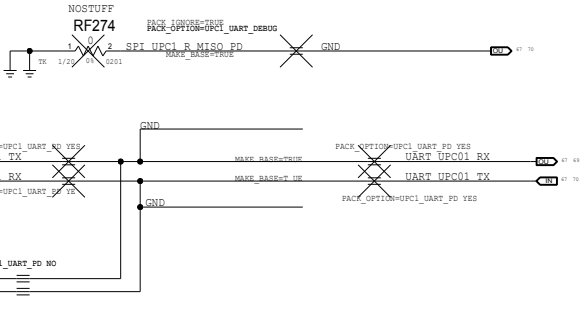
2. UPC1 needs its own ROM and do not need a fall-back method to no ROM for UPC1
   pick: "UPC1_ROM:YES" and "UPC1_UART_PD:YES"

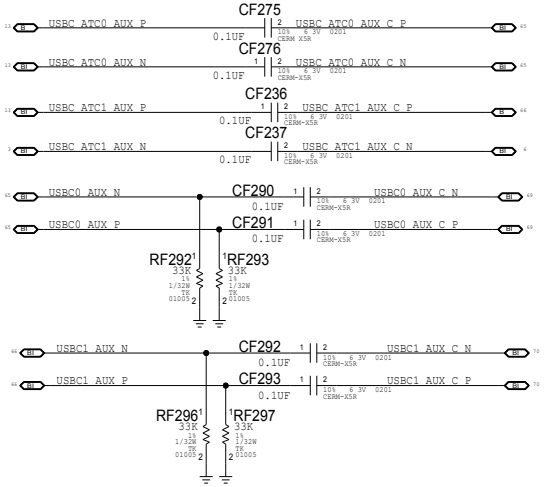
3. UPC1 does not need its own ROM
   pick: "UPC1_ROM:NO" and "UPC1_UART_PD:NO"

Ace 1 is UART Ace?









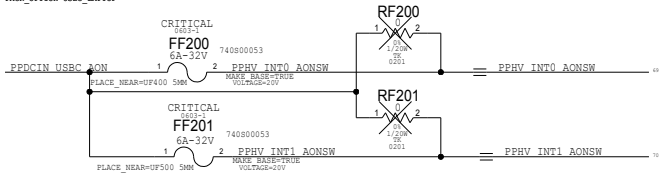
HV POWER ALIASES

Fuses for laptop charging.

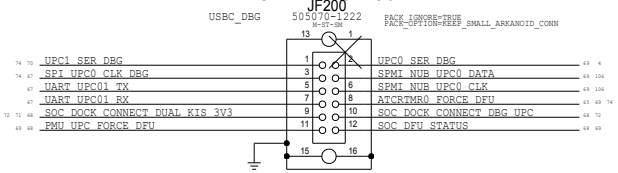
PACK_OPTION=USBC_LAPTOP

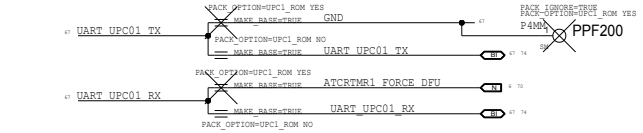
PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

Desktops only need connection for programming OTP.

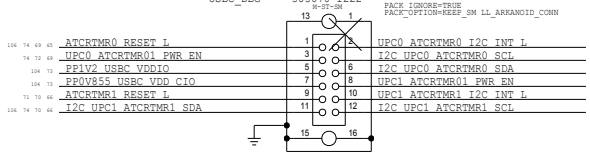


ACE ARKANOID CONN

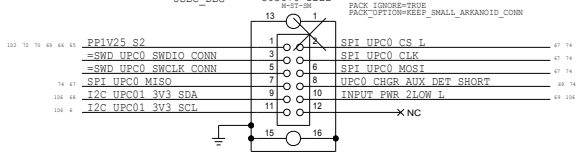




BRIDGE ARKANO D CONN



AARDVARKANO D CONN UPC0



BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: Support 1 ATC01
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 152 OF 801
	SHEET 67 OF 121

www.repairlap.com

*** REFERENCE ONLY ***

UPC 0 is the Debug Port

ATC0 / UPC0 / RTMR0

SWD_SOC_SWCLK
SWD_SOC_SWDIO
UART_DEBUGPRT_R2D
UART_DEBUGPRT_D2R
PD_UPC0_DBG_R
PMU_ACTIVE_READY
SOC_DFU_STATUS
UPC0_SOC_FORCE_DFU
SOC_DOCK_CONNECT_DBG_UPC
INT_I2C_EUSBLS0_L
UPC0_SOC_FORCE_DFU
I2C_UPC01_3V3_SCL
I2C_UPC01_3V3_SDA

RF321 100K 1/32W PD_UPC0_DBG_R

PD_UPC0_GPIO11

RF311 100K PD_UPC0_GPIO5
RF312 100K PD_UPC0_GPIO6
RF313 100K PD_UPC0_GPIO11

UPC 1 GPIOs

ATC1 / UPC1 / RTMR1

RF300 100K PD_UPC1_DBG_R

PD_UPC1_DBG_R
PMU_ACTIVE_READY
SOC_DFU_STATUS
UPC1_SOC_FORCE_DFU
SOC_DOCK_CONNECT_DUAL_KIS_3V3
INT_I2C_EUSBLS1_L
I2C_UPC01_3V3_SCL
I2C_UPC01_3V3_SDA

RF301 100K PD_UPC1_GPIO5
RF302 100K PD_UPC1_GPIO6
RF304 100K PD_UPC1_GPIO11
RF305 100K PD_UPC1_GPIO16

ATCRTMR Boot Config

[2 0] [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed

RF380 10K ATCRTMR0_BOOT_CONFIG2
RF381 10K ATCRTMR0_BOOT_CONFIG1
RF382 10K ATCRTMR0_BOOT_CONFIG0
NOSTUFF
LFKA_TEST_MODE:NO

RF383 10K ATCRTMR1_BOOT_CONFIG2
RF384 10K ATCRTMR1_BOOT_CONFIG1
RF385 10K ATCRTMR1_BOOT_CONFIG0
NOSTUFF
LFKA_TEST_MODE:NO

PP1V2_USBC_VDDIO

LFKA_TEST_MODE:YES
RF386 10K
RF387 10K
RF388 10K NOSTUFF
ATCRTMR0_BOOT_CONFIG2
ATCRTMR0_BOOT_CONFIG1
ATCRTMR0_BOOT_CONFIG0

LFKA_TEST_MODE:YES
RF389 10K
RF390 10K
RF391 10K NOSTUFF
ATCRTMR1_BOOT_CONFIG2
ATCRTMR1_BOOT_CONFIG1
ATCRTMR1_BOOT_CONFIG0

ATCRTMR CHIP ID NEEDS TO FOLLOW SOC ATC INDEX

ATCRTMR0 CH P 0X00

GND
GND

ATCRTMR1 CHIP 0X01

PP1V2_USBC_VDDIO
XWF3000
ATCRTMR1_CHIPID_0
GND

PAR #	Q	DESCRIP ION	REFERENCE ESIGNA OR(S)	CRI CAL	BOM OP ION
117800067	2	RES,TK,0 OHM,1/32W,01 05	RF332,RF334	CRITICAL	SYS_BOOT_PWR:DEFAULT_500mA
117800067	2	RES,TK,0 OHM,1/32W,01005	RF333,RF335	CRITICAL	SYS_BOOT_PWR:DISABLED

STRAP0/BUSPOWER

PP3V3_UPC0_LDO
PP3V3_UPC1_LDO

RF332 10K PACK_OPTION=USBC_LAPTOP
RF334 10K PACK_OPTION=USBC_LAPTOP
RF333 20K PACK_OPTION=USBC_LAPTOP
RF335 20K PACK_OPTION=USBC_LAPTOP

PACK_OPTION=USBC_DESKTOP
UPC0_STRAP0_BUSPOWER
UPC1_STRAP0_BUSPOWER

Unused ports

RF32A 100K PD_UPC1_USBP3_RP
RF31A 100K PD_UPC0_USBP3_RP

Connections for Laptops (USBC power in)
PACK_OPTION=USBC_LAPTOP

USBC0_CC1
USBC0_CC2
USBC1_CC1
USBC1_CC2

Connections for Desktops (No USBC power in)
PACK_OPTION=USBC_DESKTOP

LDCM

PACK_OPTION=LDCM ENABLED
PACK_OPTION=LDCM DISABLED

GND
GND
GND
GND
USBC0_LDCM_CAC_RDC
USBC0_LDCM_LB
USBC1_LDCM_CAC_RDC
USBC1_LDCM_LB

FOR FF TIE STRAP1 TO GND, FOR DEV HAVE HI/LO OPTION
Enables SPMI Interface to SoC
SPMI STRAP1 GND
I2C STRAP1 LDO_3V3

STRAPS Configurations

GND
GND

Connect PMU FORCE_DFU output here

STRAP2
PMU_UPC_FORCE_DFU
UPC0_SOC_FORCE_DFU

STRAP5
GND
GND

STRAP3 AND STRAP4 VARY BY SPMI BUS IMPLEMENTATION
UPC0 STRAP3 GND STRAP4 GND
UPC1 STRAP3 NC STRAP4 GND
UPC2 STRAP3 GND STRAP4 NC
UPC5 STRAP3 NC STRAP4 140K

NC_UPC1_I2C_ADDR
GND
GND
GND

Is UPCx_5V_EN being used?

UPC0_5V_EN
UPC1_5V_EN
RF350 100K
RF351 100K
PACK_OPTION=USBC01_VR5V_LOCAL_NO

BOM_COST_GROUP=USB-C

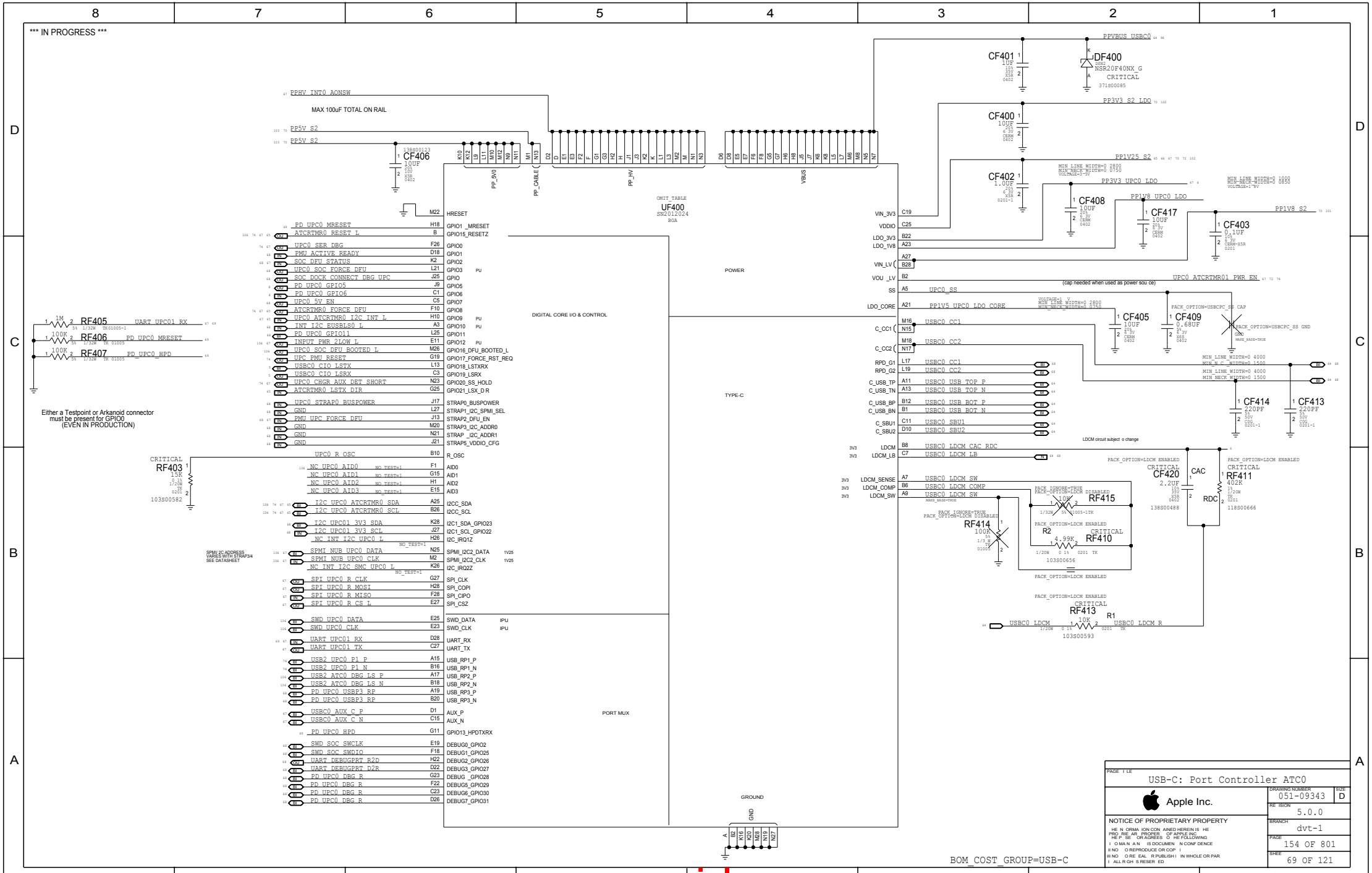
PAGE TITLE: USB-C: Support 2 ATC01

Apple Inc.

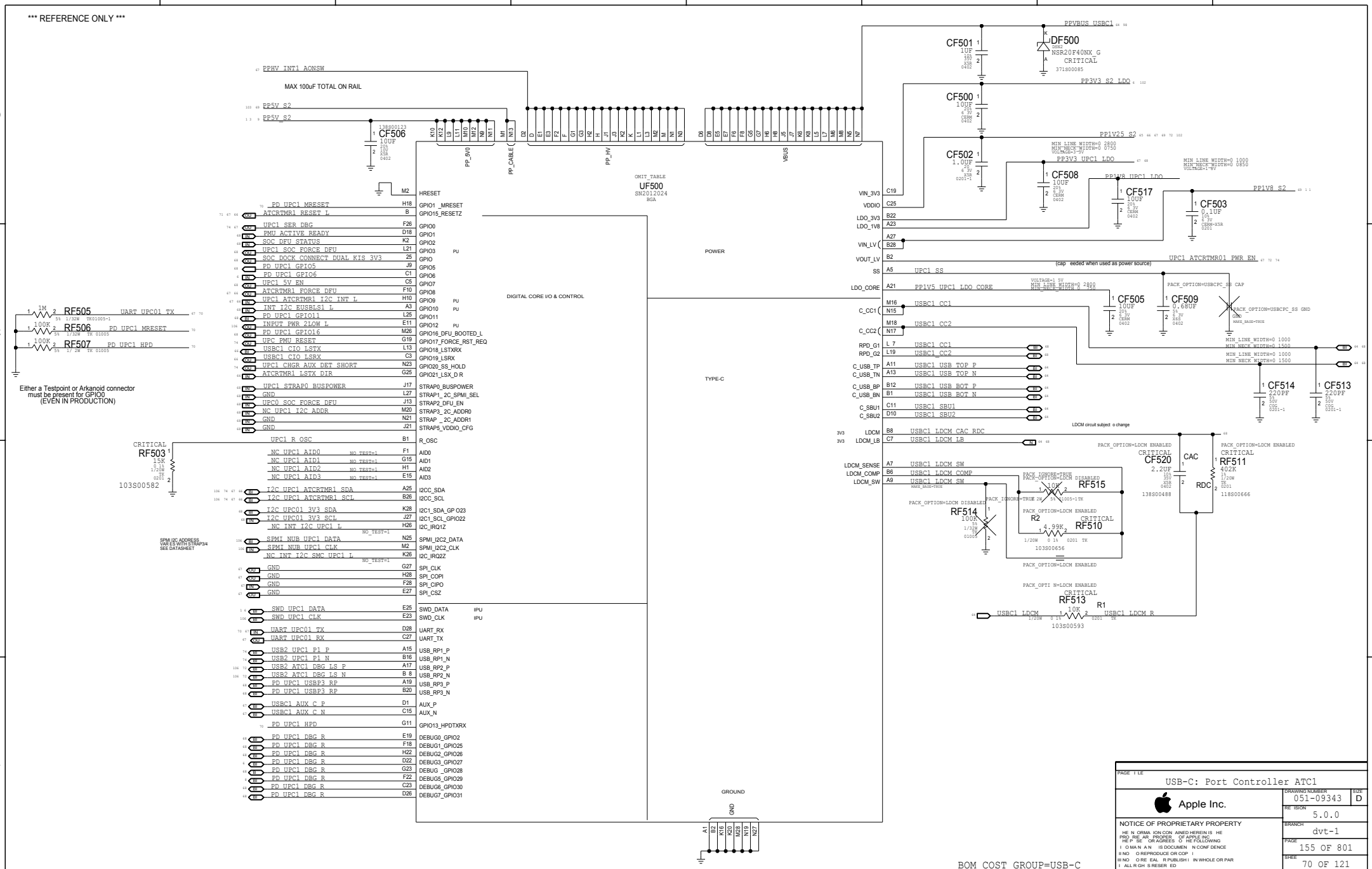
DRAWING NUMBER: 051-09343
SIZE: D
REVISION: 5.0.0
BRANCH: dvt-1
PAGE: 153 OF 801
SHEET: 68 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OF AGREES TO THE FOLLOWING
1 OMAN AN IS DOCUMEN N CONFIDENCE
II NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR
I ALL RIGHTS RESERVED

www.repairlap.com



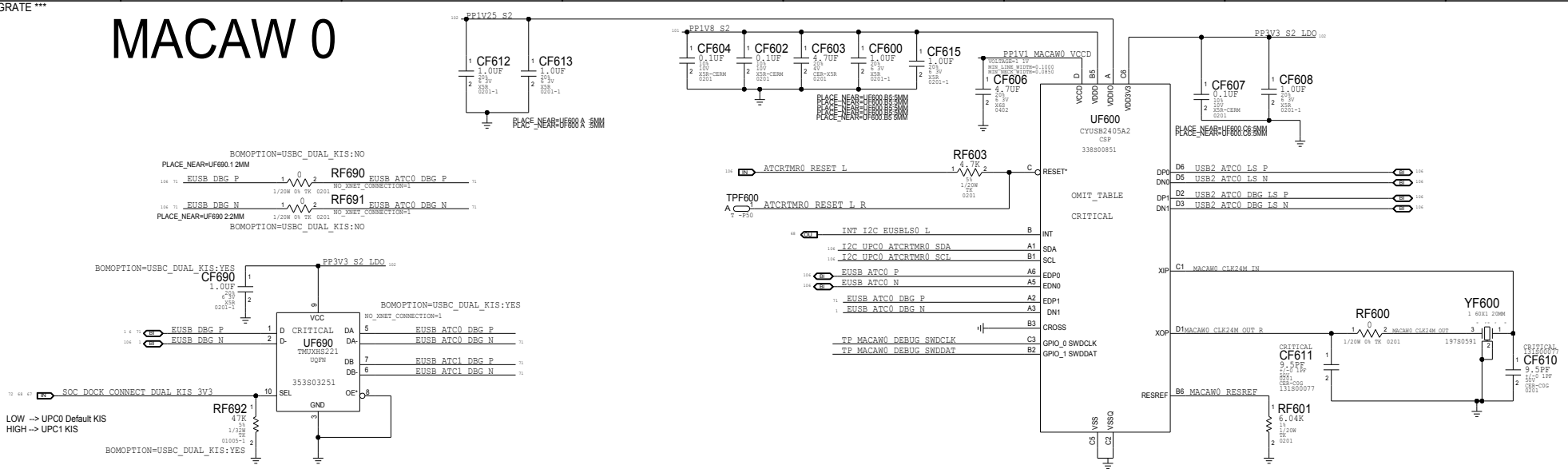
www.repairlap.com



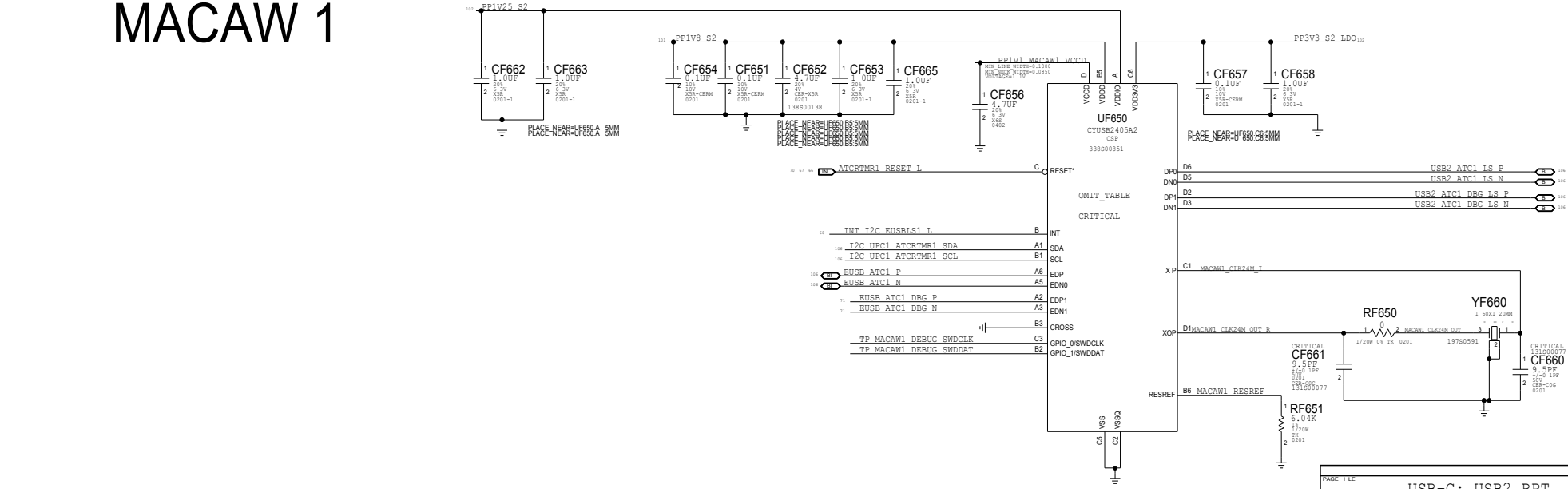
www.repairlap.com

*** OK2INTEGRATE ***

MACAW 0



MACAW 1



BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: USB2 RPT

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 156 OF 801

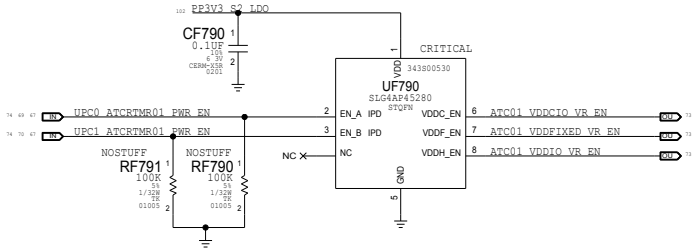
SHEET: 71 OF 121

www.repairlap.com

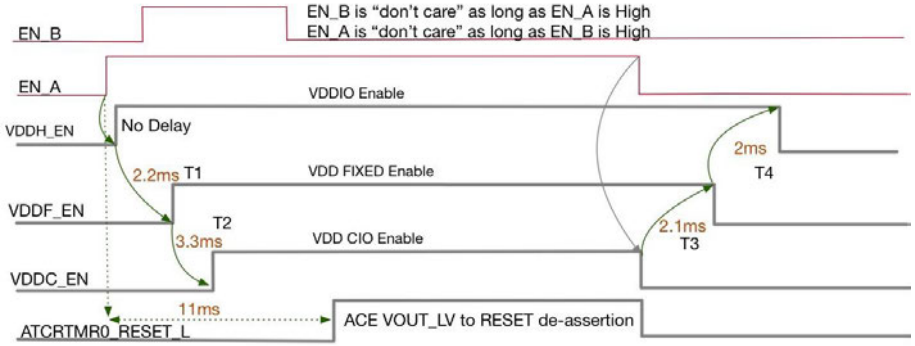
*** REFERENCE ONLY ***

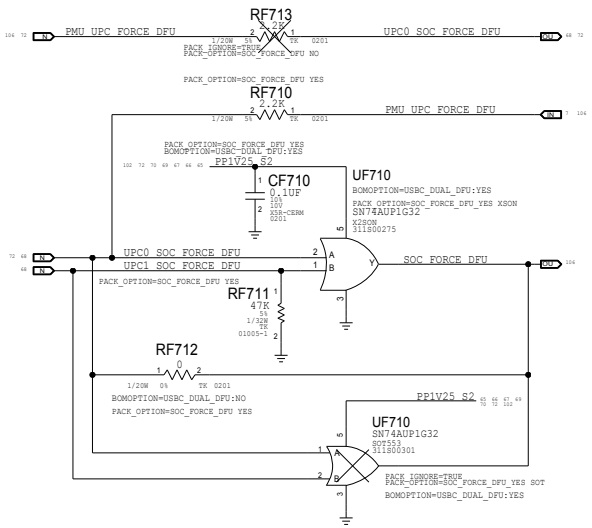
Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF400 VDDIO) same time or before System 1.8V (UF400 VIN_LV pin)
Power-up Sequence Requirements: 3.3_S2 to UF790 --> system 1.2V (UF400 VDDIO) same time or before system 1 8V (UF400) VIN_LV pin)
Power-down Sequence Requirements: The 1.8V first or at the same time as 1V2 --> 3V3_S2 needs to get disabled at minimum of 6ms from when 1V8 is discharged to below 300mV

The 3.3V needs to be HIGH before VIN_LV of Aces



Note1: As long as EN_A or EN_B are High, the outputs stay High
Note2: Outputs are an ORed and delayed version of EN_A or EN_B

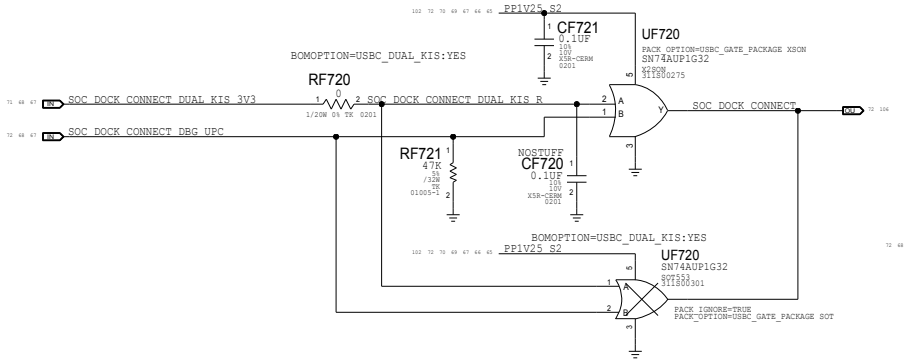


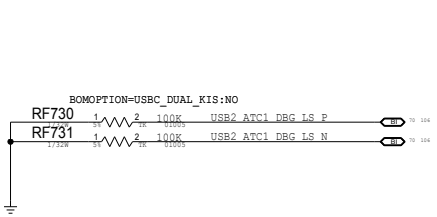


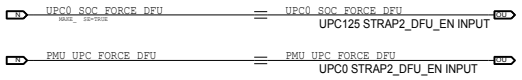
998-27825 FOR UPC*_AID SHOULD BE INCLUDED FOR EACH UPC ON DEV

DUAL KIS Connection

BOMOPTION=USBC_DUAL_KIS:YES







BOM_COST_GROUP=USB-C

USB-C: Support 3 ATC01

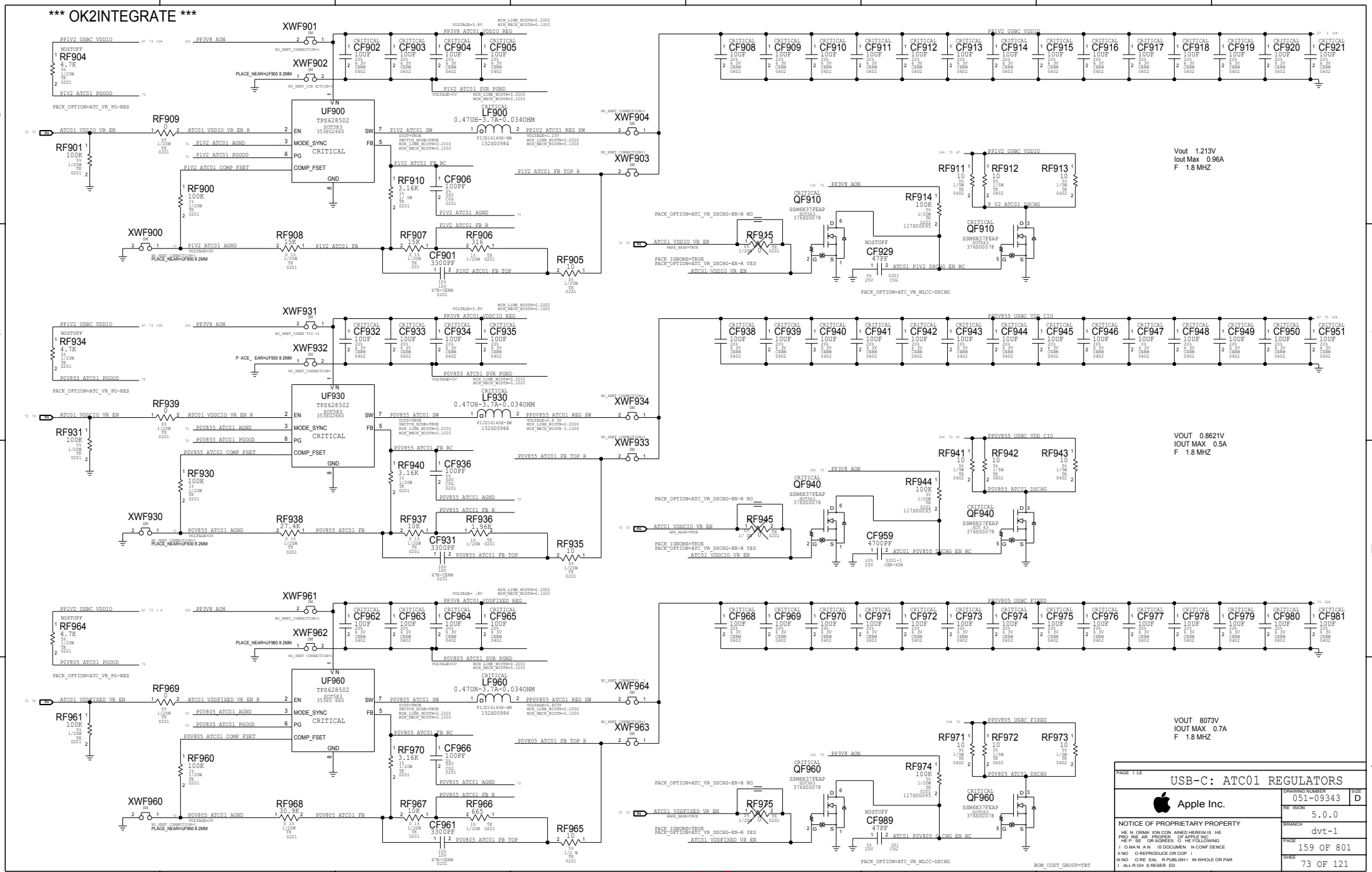
Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 157 OF 801
SHEET 72 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO THE FOLLOWING INFORMATION IS DOCUMENTED CONFIDENCE NO REPRODUCE OR COPY ALL RIGHTS RESERVED

www.repairlap.com

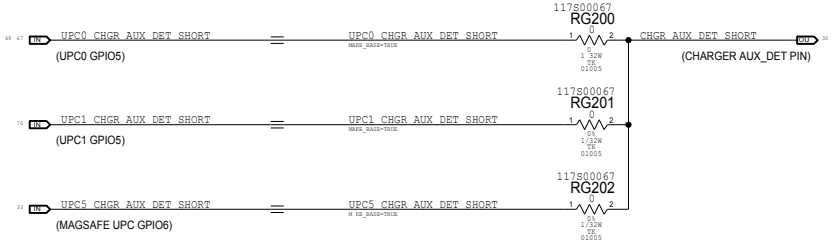
*** OK2INTEGRATE ***



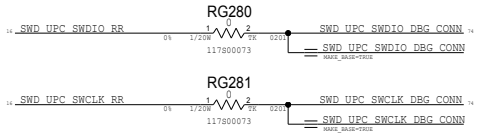
www.repairlap.com

A Charger AUX_DET Connections

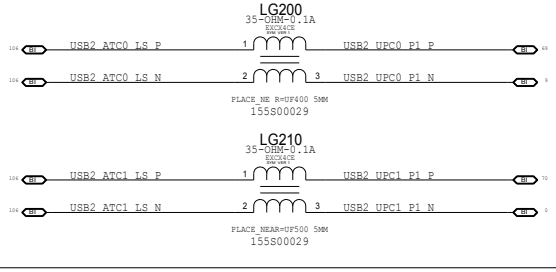
CHARGER AUX DET CONNECTIONS. <RDAR://70072178>
ALLOW ACE TO SEND A SIGNAL TO CHARGER
TO BLOCK SYSTEM CURRENT THROUGH ACE3 FETS DURING ACE3 SOFT START



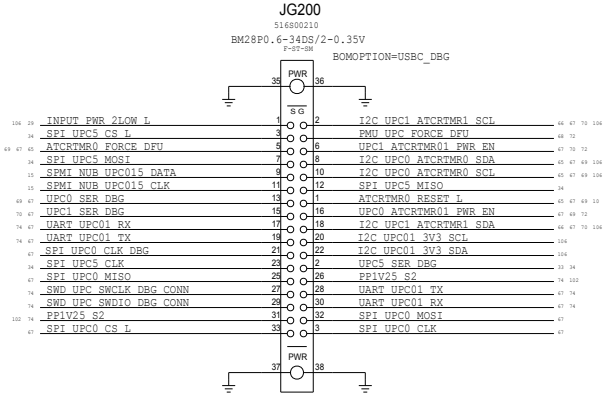
C USB-C SWDIO Aliases



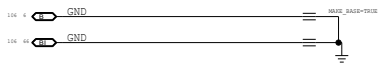
E USB 2.0 Common Mode Choke



B USB-C/MagSafe Debug Connector

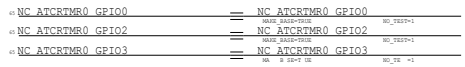


G RT13 VDDIO_EFUSE Connections

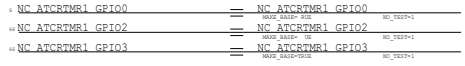


H NC UNUSED SIGNALS

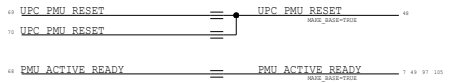
JTAG_SEL is hard grounded
TESTMODE is hard grounded



JTAG_SEL is hard grounded
TESTMODE is hard grounded



I ALIASES TO REST OF SYSTEM



BOM_COST_GROUP=USB-C

10/27/2022

PAGE TITLE: USB-C: PROJECT SUPPORT

Apple Inc.

DRAWING NUMBER: 051-09343 | SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 162 OF 801

SHEET: 74 OF 121

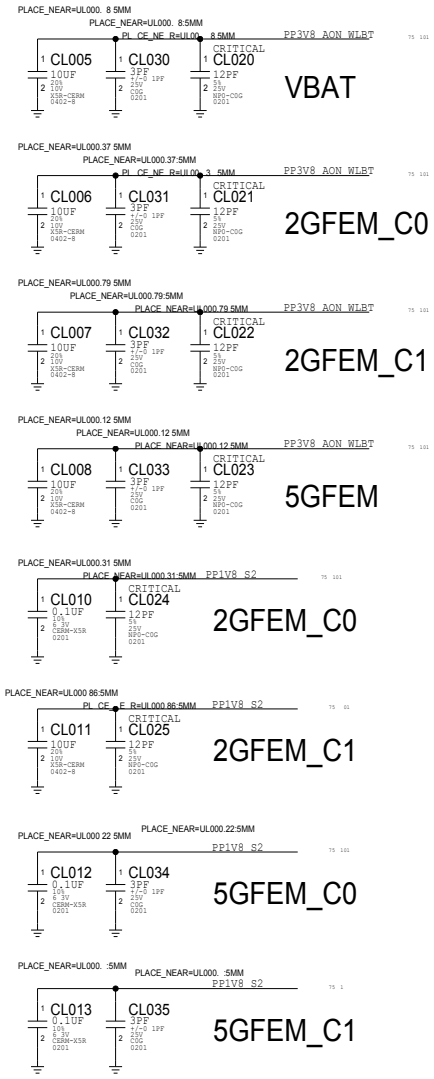
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO BY THE FOLLOWING THIS DOCUMENT CONTAINS CONFIDENCE INFORMATION. NO REPRODUCTION OR COPYING IS PERMITTED. NO PART OF THIS DOCUMENT MAY BE PUBLISHED IN WHOLE OR PART. ALL RIGHTS RESERVED.

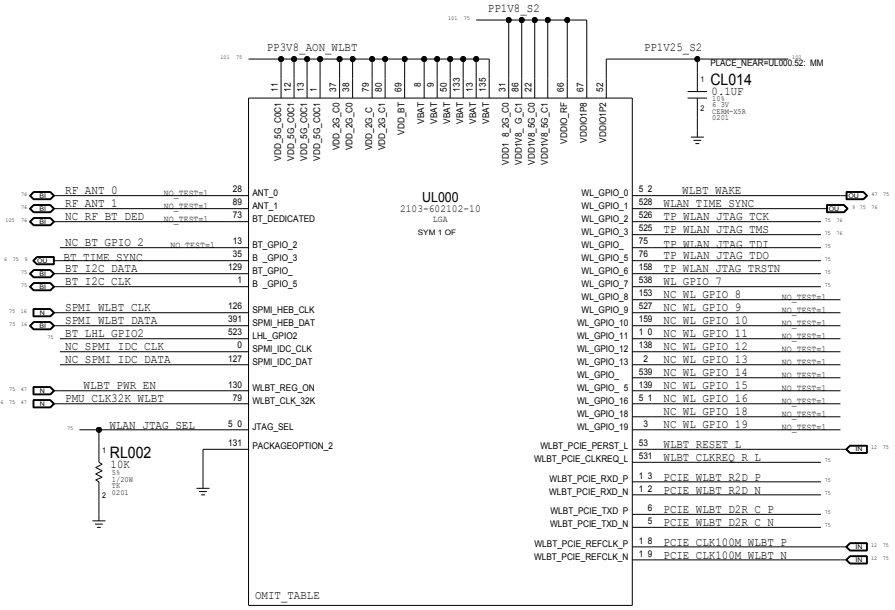
www.repairlap.com

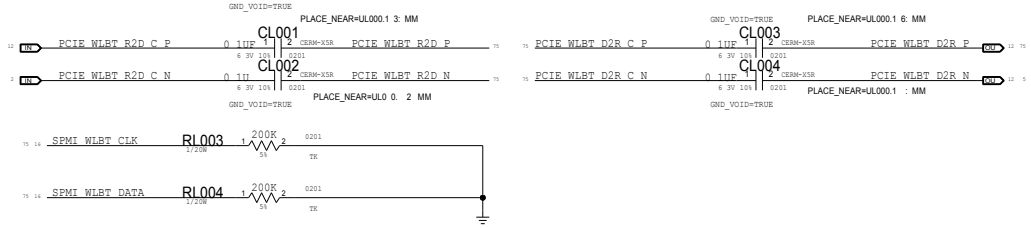
*** OK2INTEGRATE ***

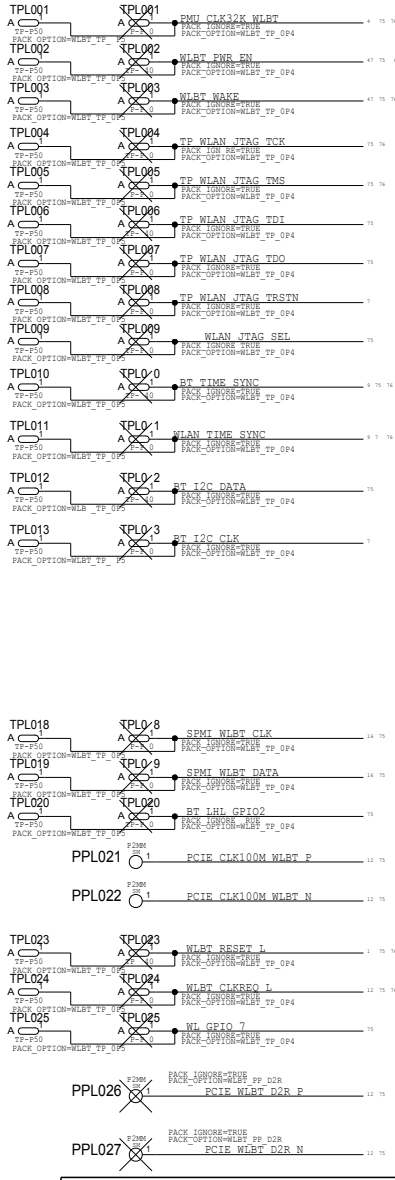
FOR SYSTEM NTEGRATION NFORMATION OF WILLAMETTE REFER TO
RDAR://PROBLEM/72432057

WILLAMETTE WIFI/BT MODULE









WILLAMETTE BOM TABLE:

PAR #	Q	DESCR P ION	REFERENCE DESIGNA OR( )	CRI ICAL	BOM OP ON
339801093		MO ULE,WLAN/BT,WILLAMETTE, E24.7	UL000	CRITICAL	

WLMT ALT BOM TABLE:

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S
339801206	339801093	ANY	UL000	AMKOR

RL001 1K 1/20W 5% 0201-1 TK

WLBT_CLKREQ_R_L — WLBT_CLKREQ_L

BOM_COST_GROUP=WIRELESS

PAGE TITLE: WIFI/BT: MODULE

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 200 OF 801

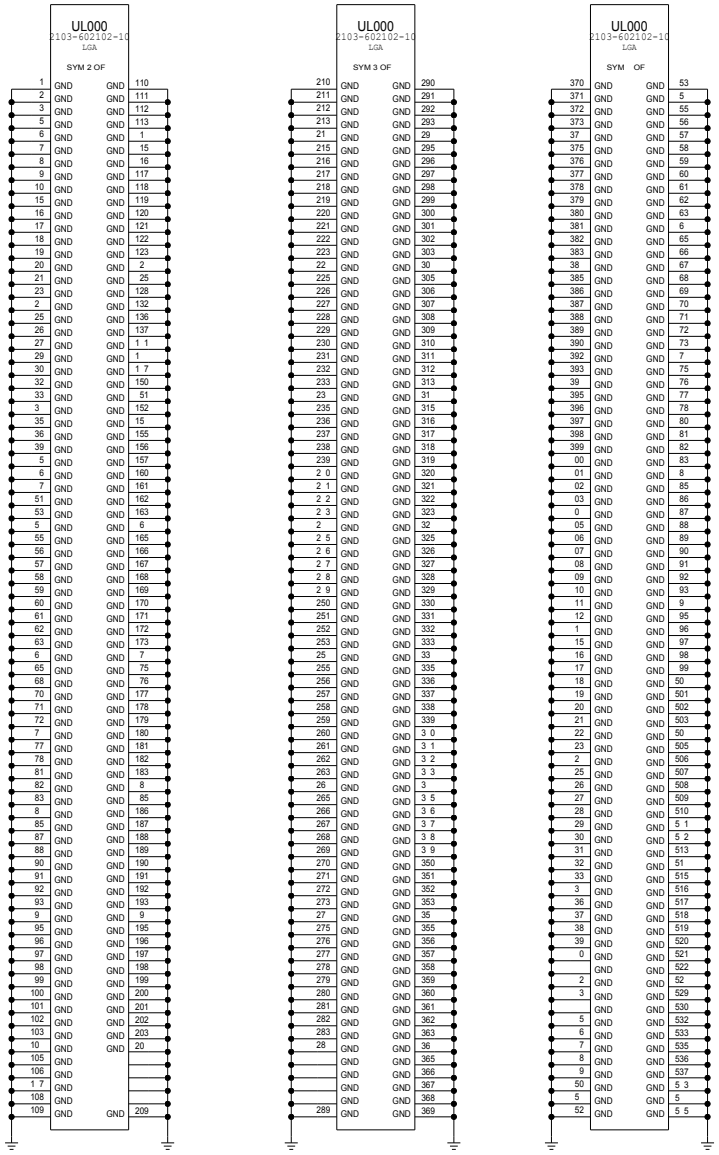
SHEET: 75 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE NFORMA ION CON AINED HEREIN IS HE PROPRI AR PROPER OF APPLE INC. HE POSES OR AGREES O HE FOLLOWING I O MA N A N HIS DOCUMEN N CONF D NCE II NO O R PRODUCE OR COP I III NO O R EAL OR PUBLISH I IN WHOLE OR PAR I ALL R GH S RE ER ED

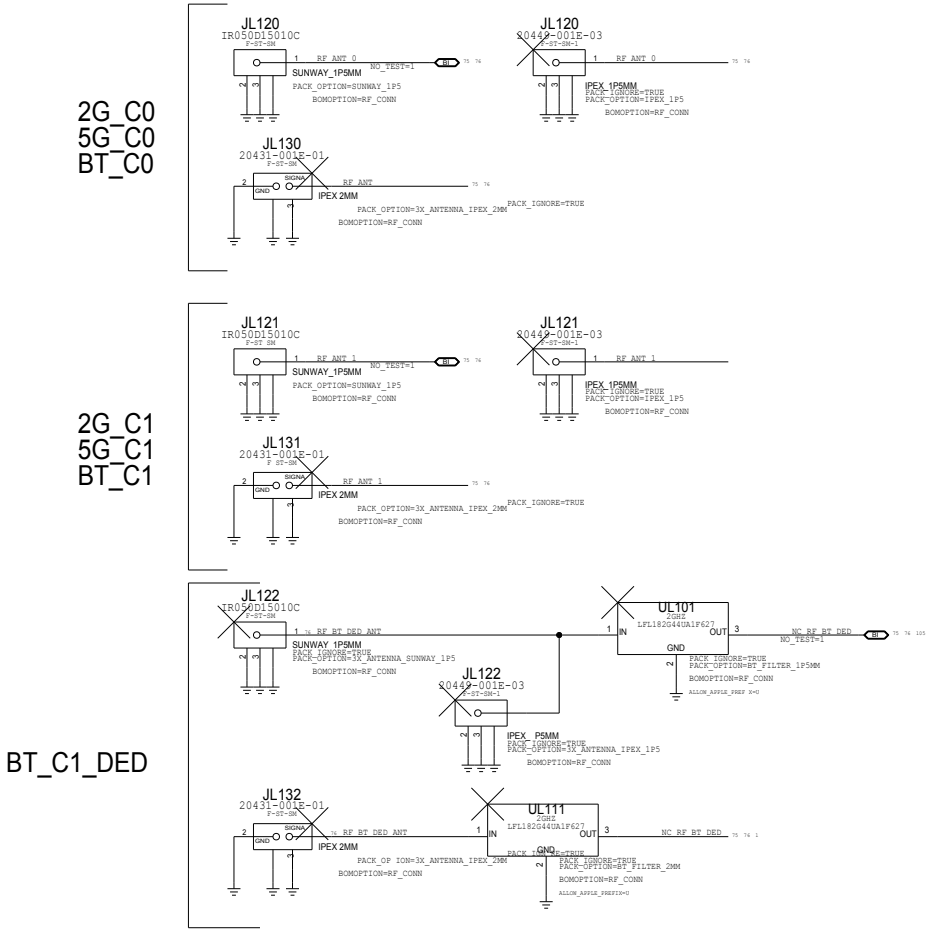
www.repairlap.com

*** OK2INTEGRATE ***

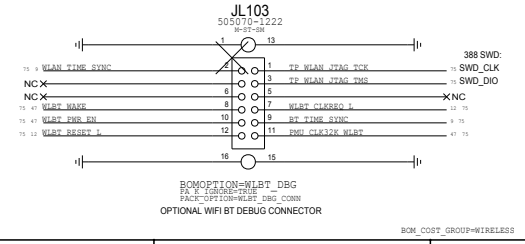
WILLAMETTE WIFI/BT MODULE GND



ANTENNA CONNECTORS



WLBT DEBUG CONNECTOR



PAGE TITLE: WIFI/BT: ANTENNA and GND

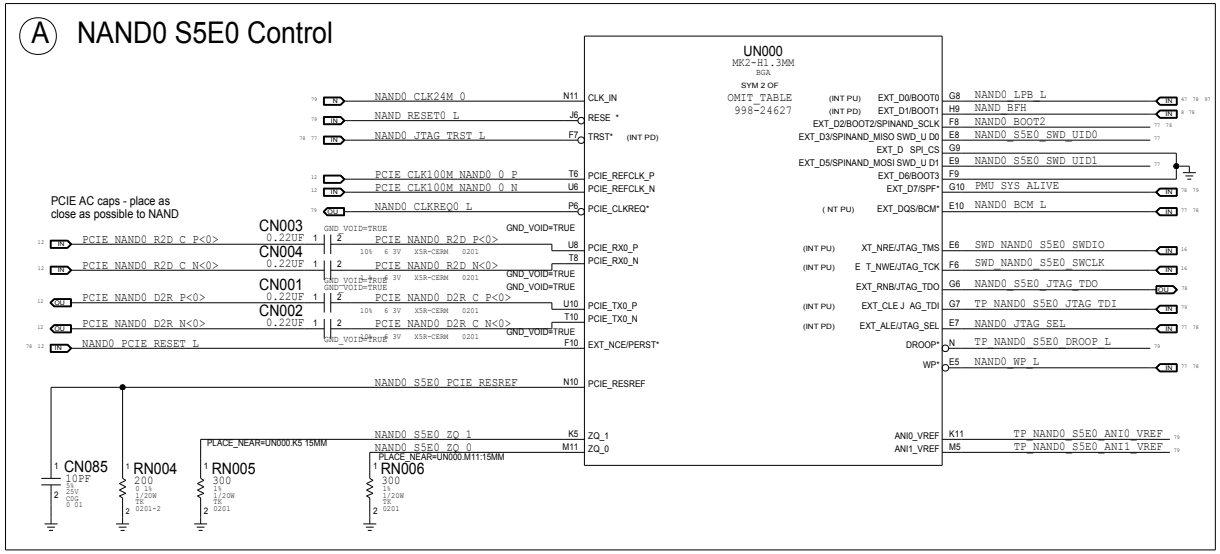
Apple Inc.

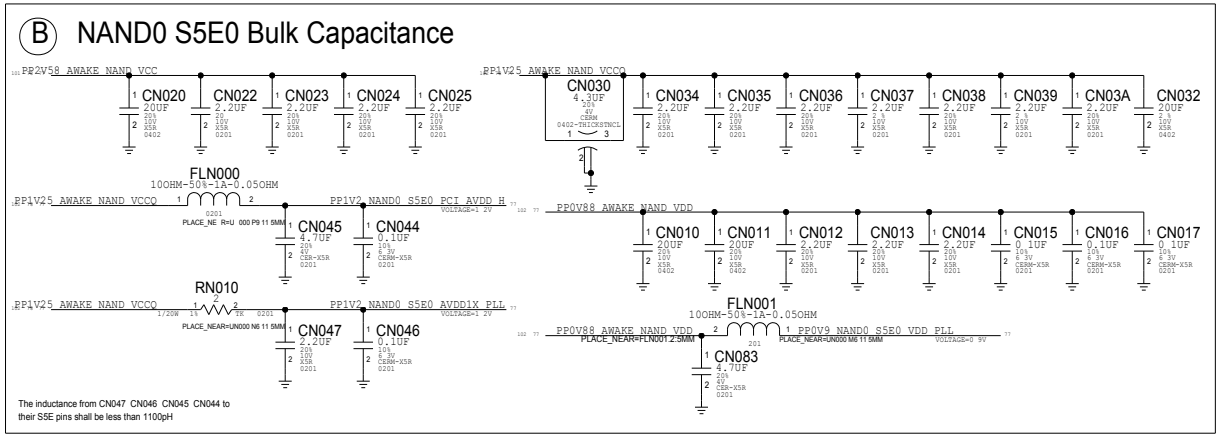
NOTICE OF PROPRIETARY PROPERTY

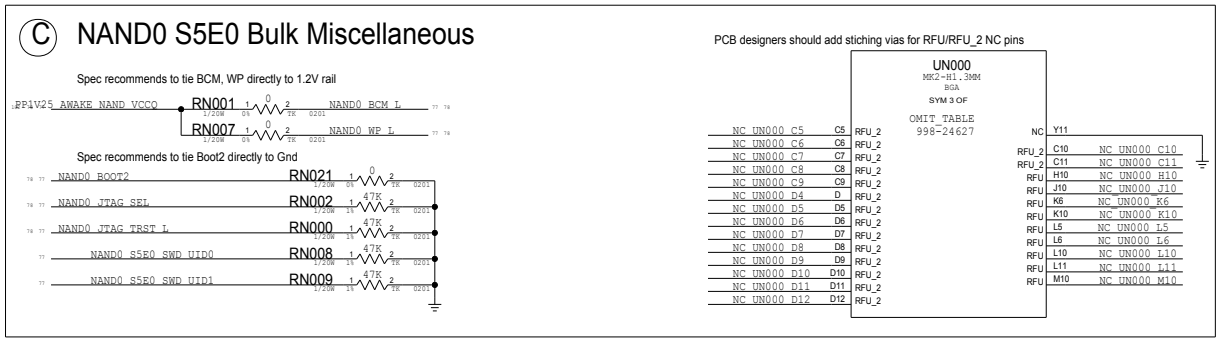
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (I) MAINTAIN DOCUMENT IN CONFIDENCE, (II) NOT REPRODUCE OR COPY, (III) NOT DISCLOSE IN WHOLE OR PART. ALL RIGHTS RESERVED.

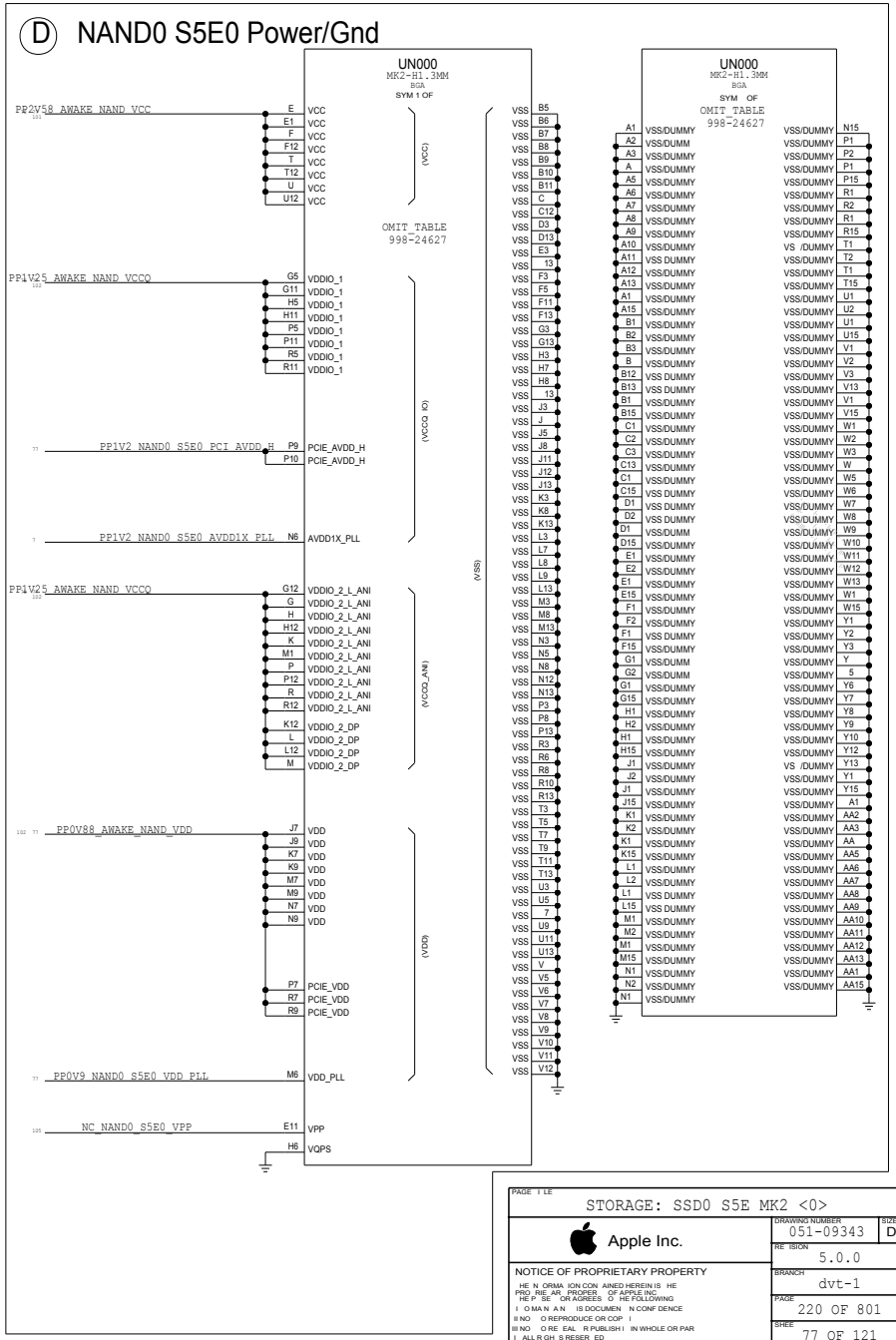
DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	201 OF 801
SHEET	76 OF 121

www.repairlap.com

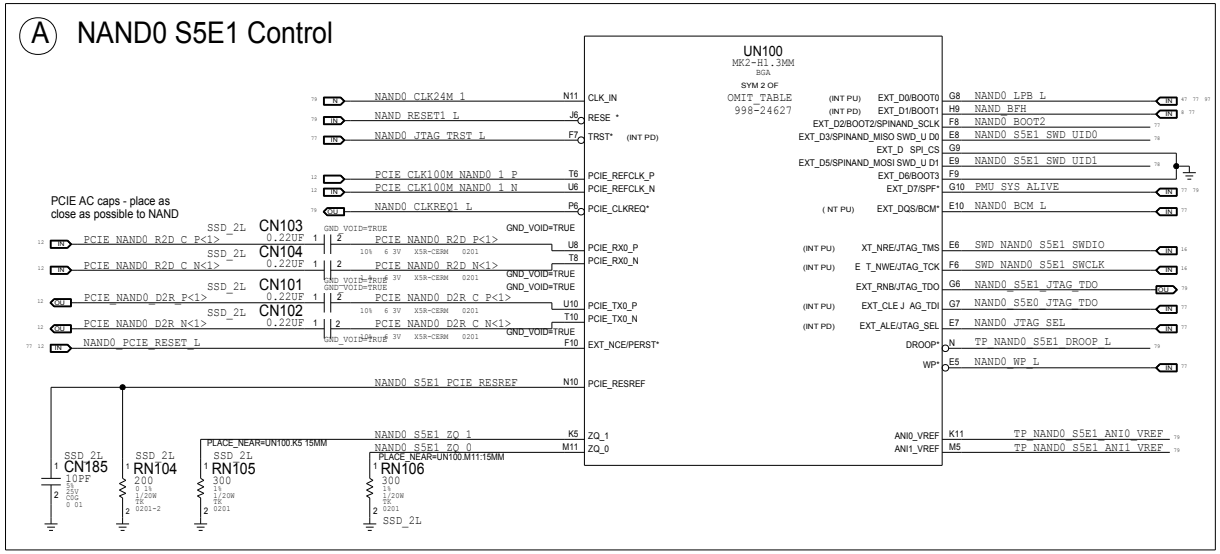


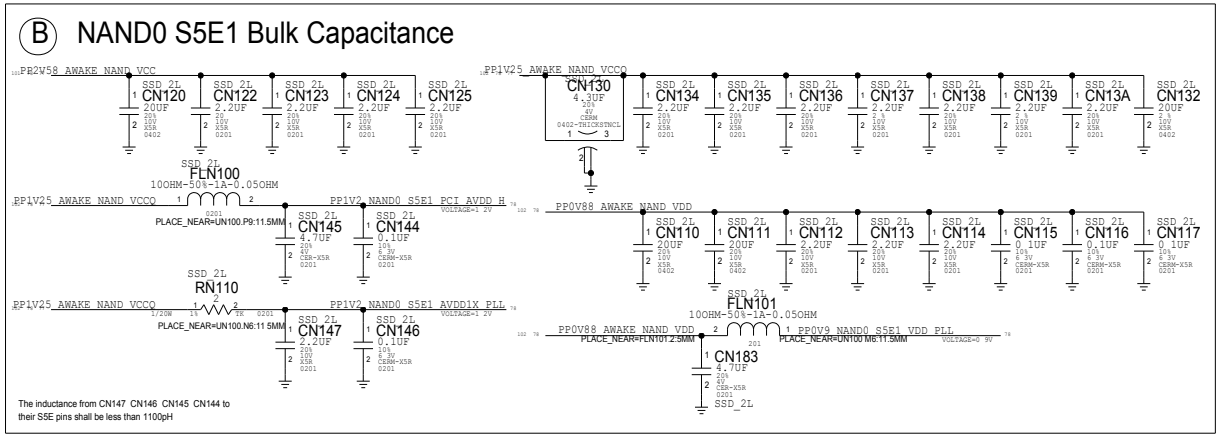


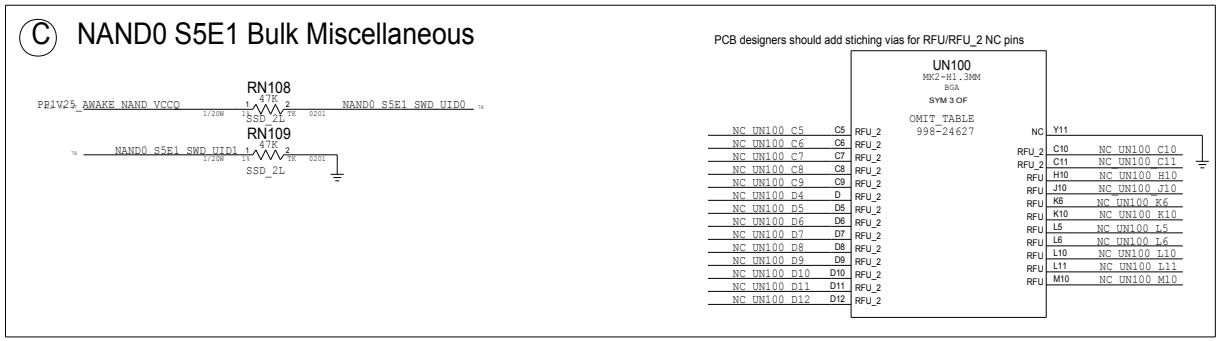


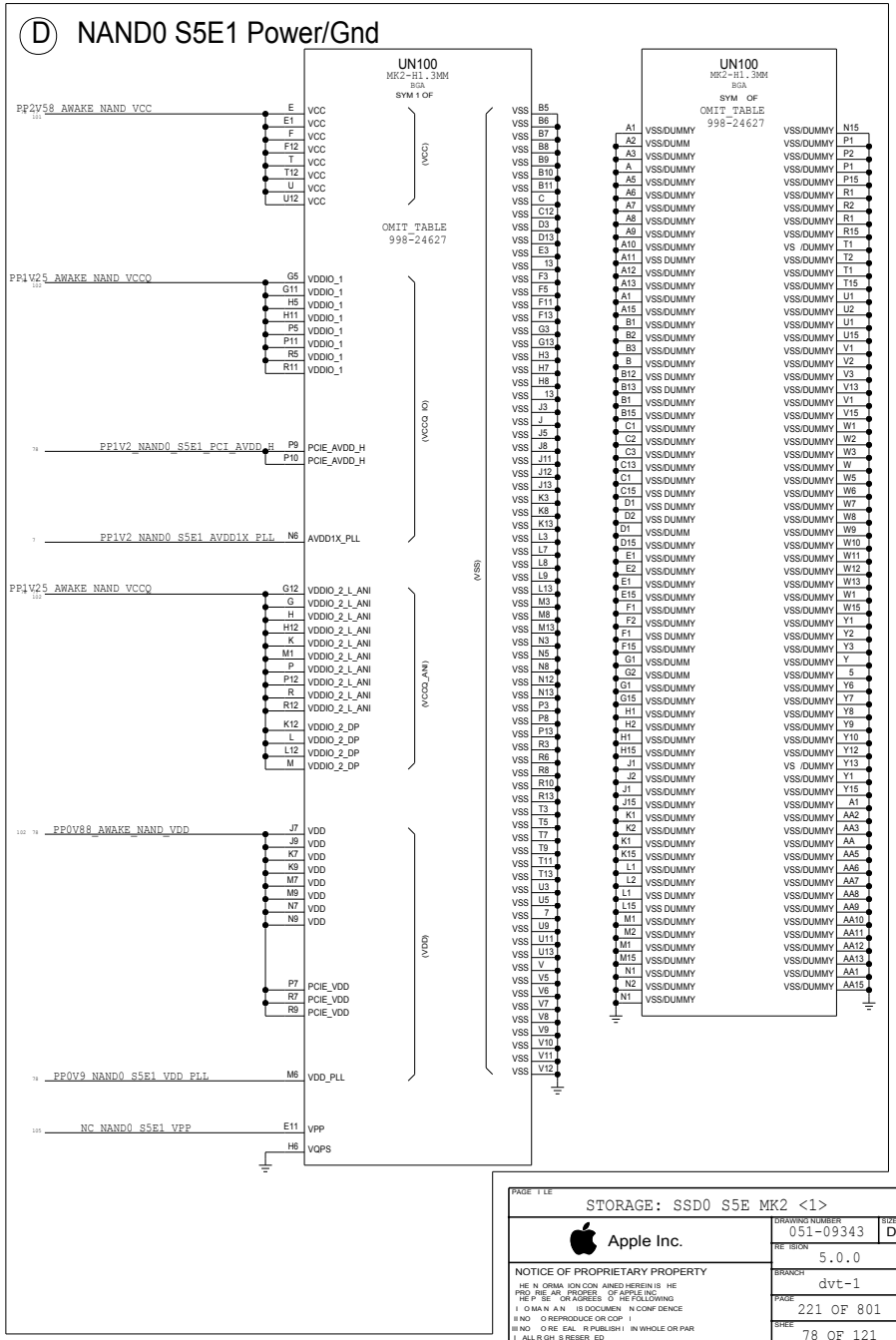


www.repairlap.com



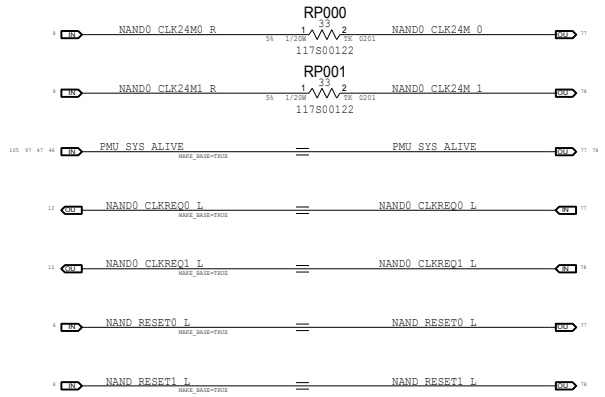




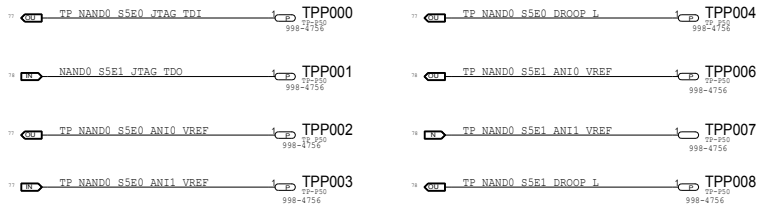


www.repairlap.com

A SSD Termination Resistors



B S5E Test Points



BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD Support

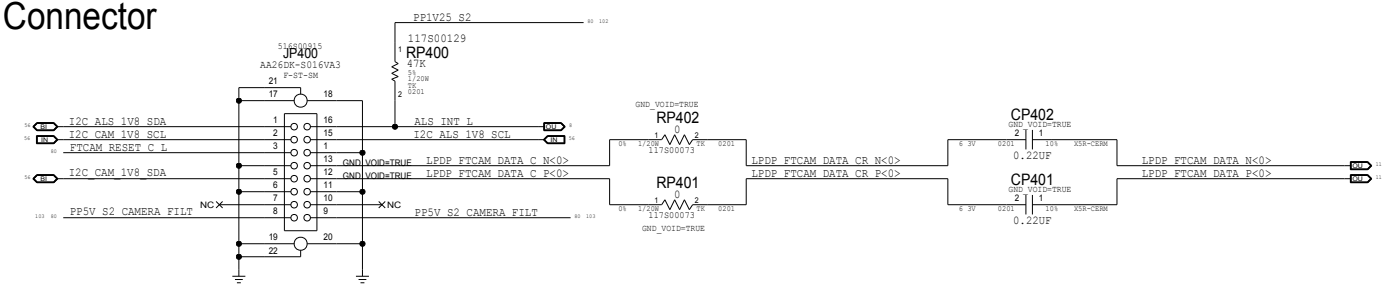
Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 230 OF 801
SHEET 79 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OF AGREES TO THE FOLLOWING: (I) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE, (II) NOT TO REPRODUCE OR COPY IT, (III) NOT TO RELEASE, PUBLISH IT IN WHOLE OR PART. ALL RIGHTS RESERVED.

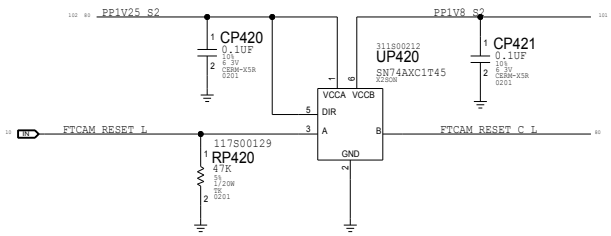
www.repairlap.com

A Camera Flex Connector

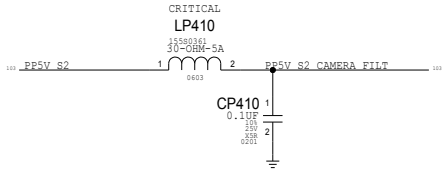


CAM TAIL FLEX CONNECTOR APN 516S00916

B Camera Reset Level Shifter



C Camera Power Filter(s)



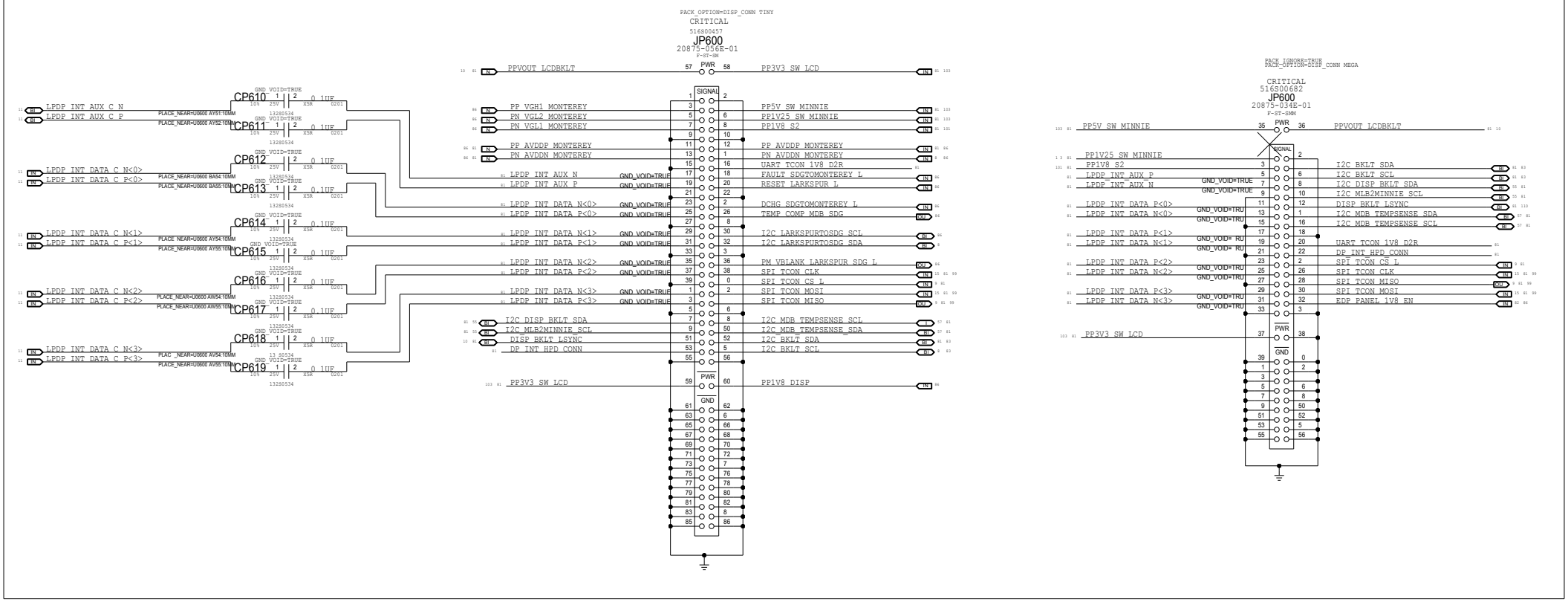
BOM_COST_GROUP=CAMERA

PAGE TITLE	CAMERA: FLEX CONNECTOR
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 234 OF 801
	SHEET 80 OF 121

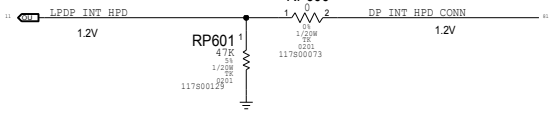
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING: THIS DOCUMENT CONFIDENCE. NO REPRODUCE OR COPY. NO REVEAL PUBLISH IN WHOLE OR PART. ALL RIGHTS RESERVED.

www.repairlap.com

A LCD Panel Interface

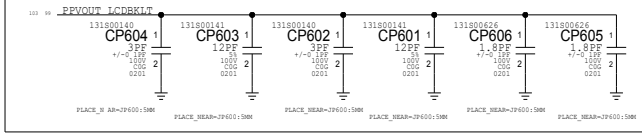


B LCD Panel Support

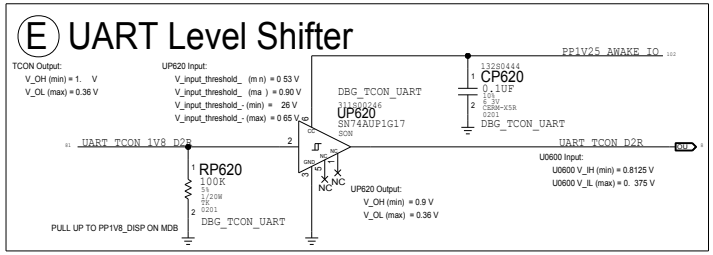


D LCD Panel Bypass

C LCD Panel Desense



E UART Level Shifter

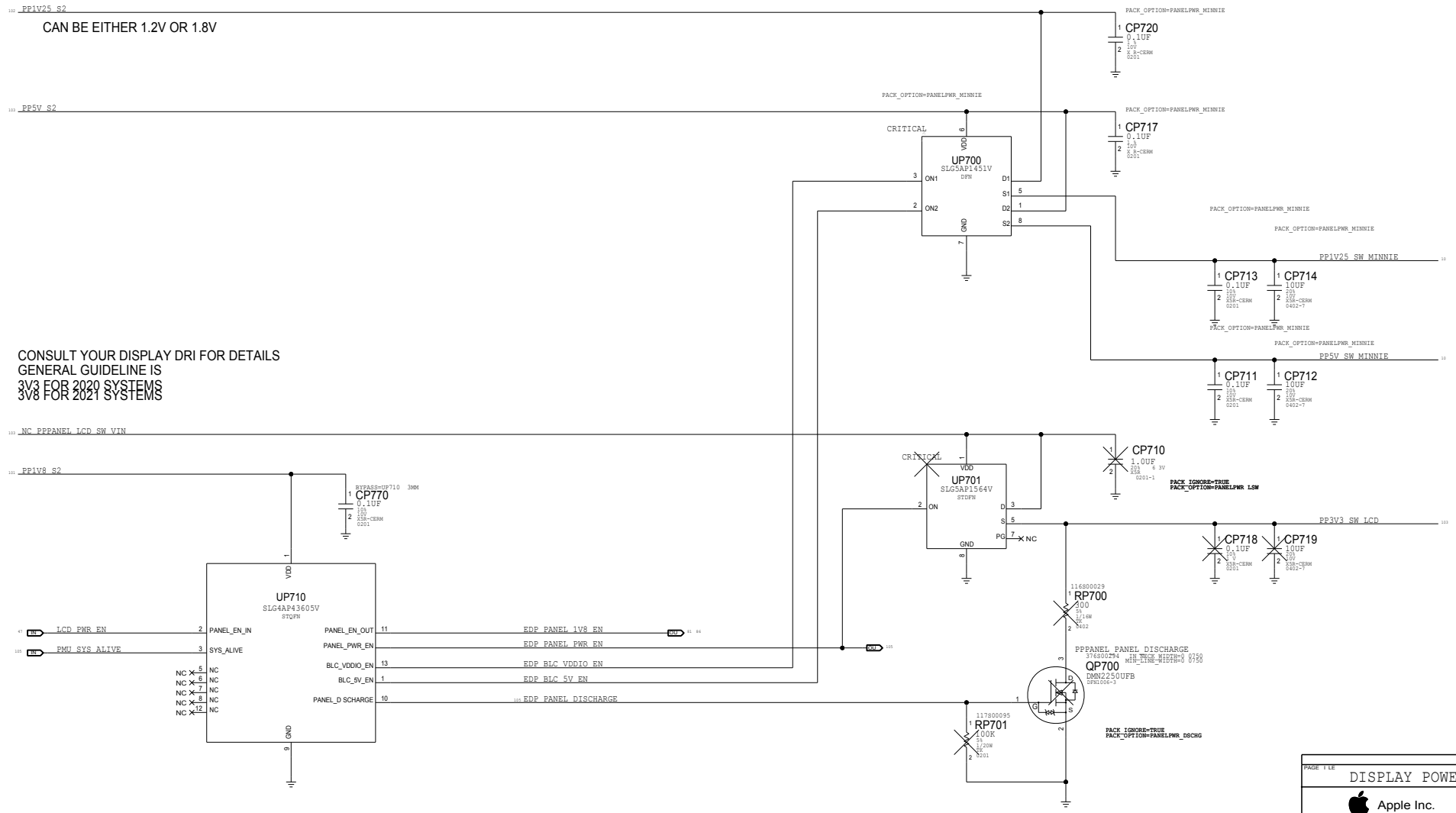


BOM_COST_GROUP=DISPLAY

PAGE TITLE	eDP Display Connector
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
NOTICE OF PROPRIETARY PROPERTY	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 236 OF 801
	SHEET 81 OF 121

www.repairlap.com

*** OK2INTEGRATE ***



PAGE TITLE
DISPLAY POWER SEQUENCER

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 237 OF 801

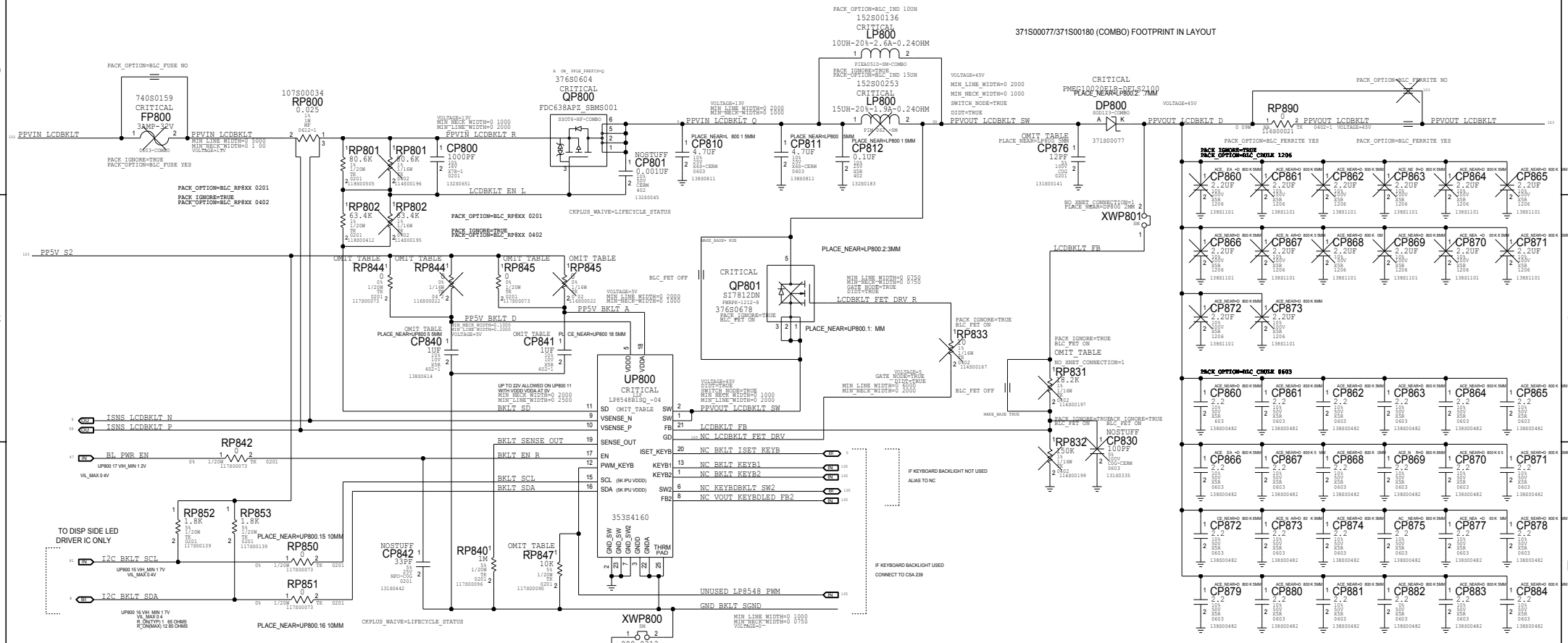
SHEET 82 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (1) MAINTAIN IS DOCUMENT IN CONFIDENCE (2) NOT REPRODUCE OR COPY IT (3) NOT DISCLOSE IT IN WHOLE OR PART. ALL RIGHTS RESERVED

www.repairlap.com

*** OK2INTEGRATE ***

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER



BEN IC VERSION TO MATCH VERS ON OF JERRY/MINNIE IC IS ON THE PANEL

PAR #	Q	DE CRIP ION	REFERENCE DE IGNA OR(S)	CRI ICAL	BOM OP ION
353S4160	1	IC,LP8548B1-04,DC/DC CVTR,BOOST,QFN- 4	UP800		BLC_BEN_IC:V4
353S02256	1	I LP8548B1A-07,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V7
353S02616	1	IC,LP 5488A-08,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V8

BACKLIGHT SWITCH NOD DESENSE OPTION

PAR #	Q	DE CRIP ION	REFERENCE DE IGNA OR(S)	CRI ICAL	BOM OP ION
131S00141	1	CAP,COG,12PF,5%,100V,0201	CP876		BLC_SW_NODE_DESENSE

10K F KEYBOARD PWM INPUT IS NOT PRESENT (X9 1, X1536)
100K IF KEYBOARD PWM NPUT S PRESENT (X1536)

PAR #	Q	DE CRIP ION	REFERENCE DE IGNA OR(S	CRI ICAL	BOM OP ION
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RP847		BLC_KBD_BOOST_USED NO
118S00251	1	RES TK,100K OHM,1%,1/20W,0201	RP847		BLC_KBD_BOOST_USED YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEDS PER STRING

PAR #	Q	DESCRIP ION	REFERENCE DESIGNA OR(S)	CRI ICAL	BOM OP ION
114S00197	1	RES,TK,18 2KOHM,1%,1/16W,0402	RP831		BLC_LEDS_PER_STRING:16
114S00198	1	RES,TK,28 7KOHM,1% 1/16W,0402	RP831		BLC_LEDS_PER_STRING:18

BOM OP ION FOR BLC 5V RC E LTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION.
AS COMPARED O BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR: /506825 2>

PAR #	Q	DESCRIP ION	REFERENCE DESIGNA OR(S)	CRI ICAL	BOM OP ION
117S00073	2	RES,TK,0 OHM,1A MAX,1/20W,0201	RP844,RP845		BLC_5V_SERIES:0_OHM_0201
118S00311	2	RES,TK,10 OHM,1%,1/20W,0201	RP844,RP845		BLC_5V_SERIES:10_OHM_0201
116S00022	2	RES,TK,0 OHM,2A MAX,1/16W,0402	RP844,RP845		BLC_5V_SERIES 0_OHM
114S00167	2	RES,TK,10 OHM,1%,1/ 6W,04 2	RP844,RP845		BLC_5V_SERIES 10_OHM
138S0614	2	CAP,CER,X5R,10UF,10%,10V,0402	CP840,CP841		BLC_5V_CAP:1_UF
138S0007	2	CAP,CER,X5R,4 7UF,20% 25V,0402	CP840,CP841		BLC_5V_CAP:4P7_UF

PAGE T LE
BEN: CONTROLLER

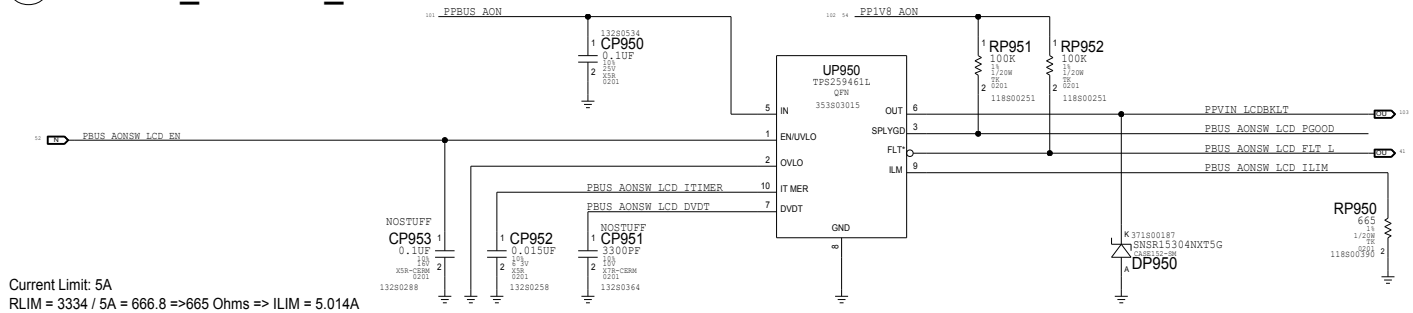
Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
RE ISION 5.0.0
BRANCH dvt-1
PAGE 238 OF 801
SHEE 83 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC HE P SE OR AGREES O HE FOLLOWING I O MA N A N IS DOCUMEN N CONF DENCE
III NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR I ALL R GH S RESER ED

www.repairlap.com

Ⓐ PPBUS_AONSW_LCD Load Switch & e-Fuse

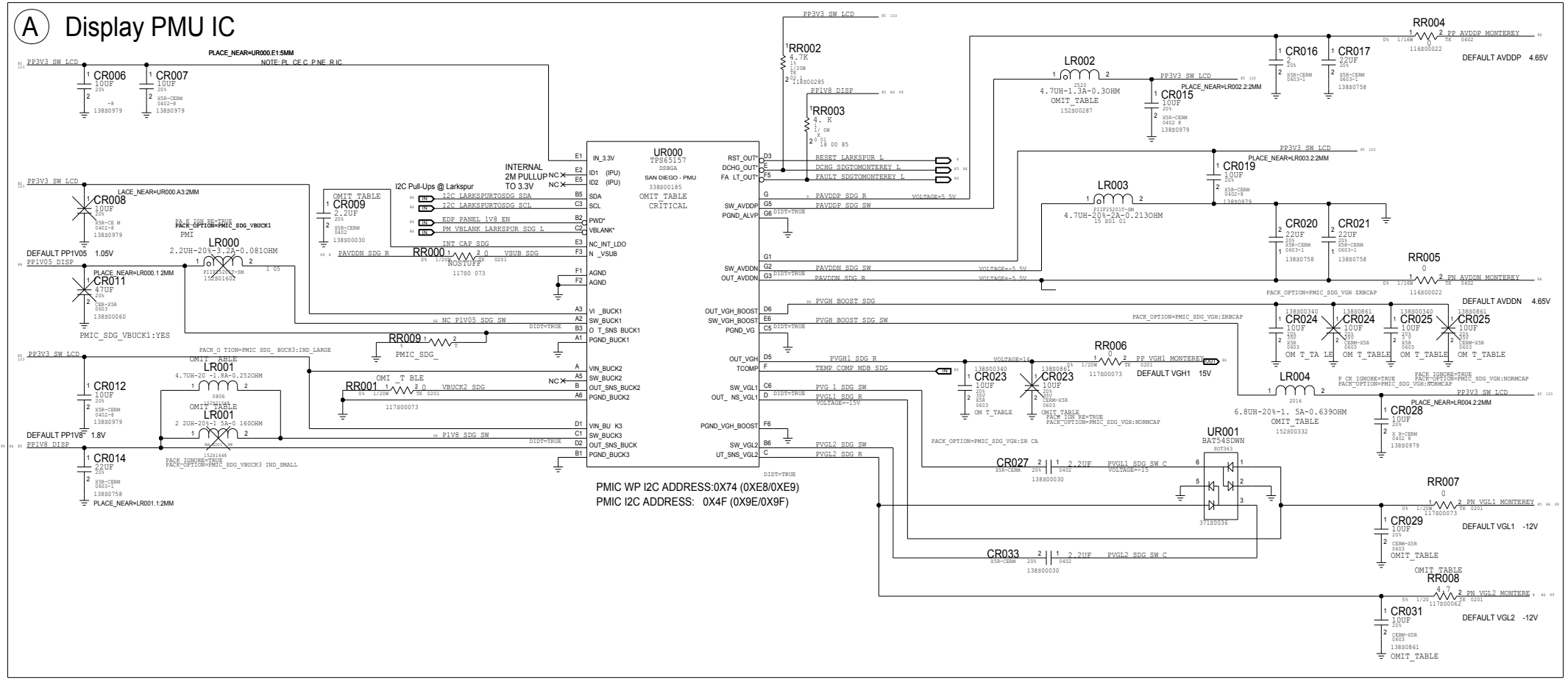


Current Limit: 5A
RLIM = 3334 / 5A = 666.8 =>665 Ohms => ILIM = 5.014A
/FLT Open Drain

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE	BEN: PBUS E-Fuse
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 239 OF 801
	SHEET 84 OF 121

www.repairlap.com



B BOMOPTIONs: TI vs. Intersil

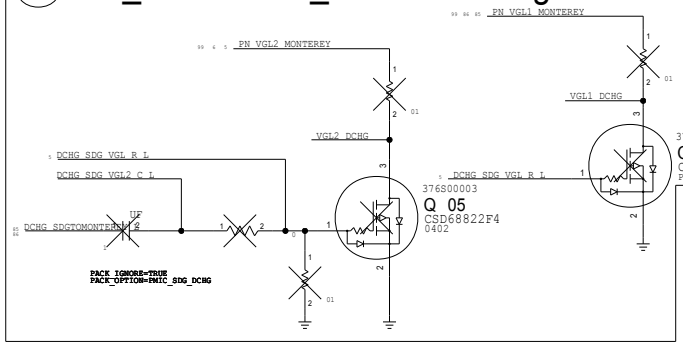
Texas Instruments Option Table

PA T#	QT	ESCRIPTION		
338S01021	1	IC,TPS65157BDSER,PMU,SAN DIEGO,BGA42	UR000	SDG_TI_PROG X2203
338S01020	1	IC,TPS65157B,PMU,SAN DIEGO,BG,DSBGA42	UR000	SDG_TI_PROG BLANK
152S00289	2	IND,4.7UH,2016,PIFA2016T-4R7MEN	LR001	SDG_TI
152S01601	1	IND,MLD,4.7UH,20%,2A,0.2130 M,2 20	LR002	SDG_TI
152S00332	1	IND,6.8UH,2016,PIFA2016T6R8 013	LR0 4	SDG_TI
138S0861	2	AP, ER,100F.20%,35V,X5R,0603	CR029,CR031	SDG_TI
138S0861	2	CAP,CER,100F.20%,35V,X5R,0603	CR024,CR025	PMIC_SDG_OUT6 NORMCAP
138S00340	2	CAP,CER,X5R,100F,20%,35V,0603,LOW NOISE	CR024,CR025	PMIC_SDG_OUT6 ZRBCAP
138S00030	1	CAP,CER,2.2UF.20%,35V,X5R,0402	CR009	SDG_TI
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	RR008	SDG_TI
138S0861	1	CAP,CER,100F.20%,35V,X5R,060	CR023	PMIC_SDG_VGH NORMCAP
138S00340	1	CAP,CER,X5R,100F,20%,35V,0603,L W OIS	CR023	PMIC_SDG_VGH ZRBCAP

Intersil Option Table

PA T#	QT	ESCRIPTION		B
338S00183	1	IC,ISL98669,SAN DIEGO,A1,CSP42	UR000	SDG_ISL
152S1648	2	IND,2.2UH,2016,WAWE20167R2M	LR001	SDG_ISL
152S00286	1	IND,2.2UH,2520,VLS252010HBX-2R2M	LR002	SDG_ISL
152S00483	1	IND,10UH,2016,LQH2MHH2R2M02	LR004	SDG_ISL
138S0709	2	C P,CER,4 7UF.10%,35V,X5R,0603	CR029,CR031	SDG_ISL
138S0709	2	C P,CER,4 7UF.10%,35V,X5R,0603	CR024,CR025	SDG_ISL
116S00022	1	RES,0 OHM,1A,0402	CR009	SDG_ISL
117S00062	1	RES,TK,4.7 OHM,5%,1/20W,0201	RR008	SDG_ISL
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	RR001	SDG_ISL

C PN_VGL1 & PN_VGL2 Discharge Circuit



PMU: SAN DIEGO

Apple In

DRAW NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 240 OF 801

SHEET 85 OF 121

www.repairlap.com

A Power Connections Alias

81	PP1V8_DISP M RE BASE=TRUE	PP1V8_DISP	85 99
	PP1V05_DISP MAKE_BAS =TRUE	PP1V05_DISP	85
81	PN_VGL1_MONTEREY MAKE_B SE=TRUE	PN_VGL1_MONTEREY	85 99
81	PN_VGL2_MONTEREY MAKE_BASE=TRUE	PN_VGL2_MONTEREY	85 99
81	PP_AVDDP_MONTEREY MAKE_BASE=TRUE	PP_AVDDP_MONTEREY	85
81	PN_AVDDN_MONTEREY M RE BASE=TRUE	PN_AVDDN_MONTEREY	85
81	PP_VGH1_MONTEREY MAK BASE=TRUE	PP_VGH1_MONTEREY	85
	NC_P1V05_SDG_SW MAKE_B SE=T UE	NC_P1V05_SDG_SW	85

B Signal Connections Alias

81	I2C_LARKSPURTOSDG_SDA MAKE_BASE=T U CRPLIS_WAIVE=I2C_PULLUP	I2C_LARKSPURTOSDG_SDA	85
	I2C Pull-Up @ Larkspur		
81	I2C_LARKSPURTOSDG_SCL MAKE_BASE=TRUE CRPLIS_WAIVE I2C_PULLUP	I2C_LARKSPURTOSDG_SCL	85
	I2C Pull-Up @ Larkspur		
82 81	EDP_PANEL_1V8_EN MA E BASE=TRUE	EDP_PANEL_1V8_EN	85
81	PM_VBLANK_LARKSPUR_SDG_L M GE_AS = RUE	PM_VBLANK_ARKSPUR_SDG_L	86
81	RESET_LARKSPUR_L MAKE_BAS TR	RESET_LARKSPUR_L	85
81	DCHG_SDGTOMONTEREY_L MAKE_BASE=TRUE	DCHG_SDGTOMONTEREY_L	85
81	FAULT_SDGTOMONTEREY_L MAKE_BASE=TRUE	FAULT_SDGTOMONTEREY_L	85
81	TEMP_COMP_MDB_SDG MA E_BASE=TRUE	TEMP_COMP_MDB_SDG	85

PAGE TITLE
PMU: SAN DIEGO SUPPORT

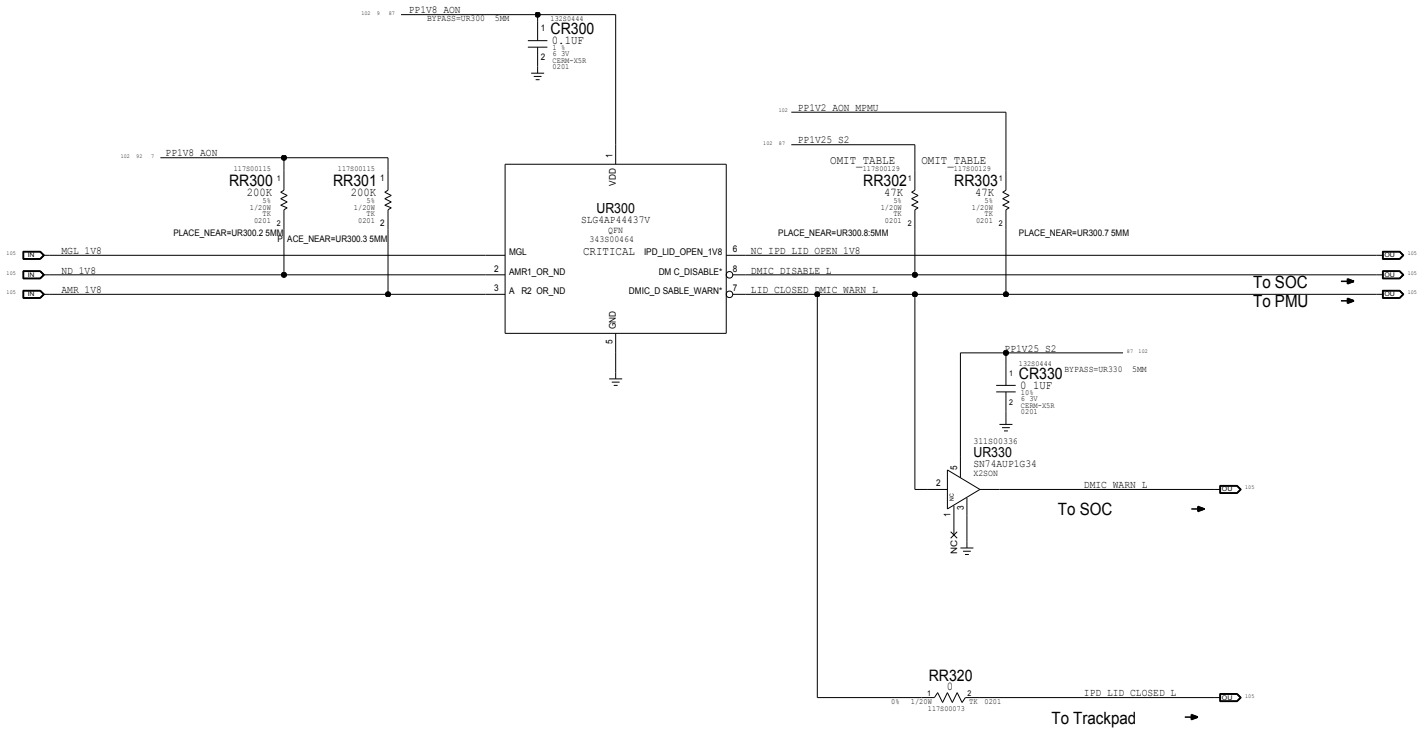
Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 241 OF 801
SHEET 86 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
2. NOT TO REPRODUCE OR COPY
3. NOT TO REVEAL, PUBLISH IN WHOLE OR PART
4. ALL RIGHTS RESERVED

www.repairlap.com

A Secure Disable SAK: AMR+LAS



B Secure Disable BOM Options

PAR #	Q	DE CR P ON	REFERENCE DES GNA OR	CRI ICAL	BOM OP ON
117800129	1	RES,TK,47K OHM,5%,1/20W,0201	RR302,RR303	CRITICAL	REFSECDIS_RR302 47K
118800521	1	RES,TK,30K OHM,1%,1/20W,0201	RR302,RR303	CRITICAL	REFSECDIS_RR302 30K

BOM_COST_GROUP=SOC

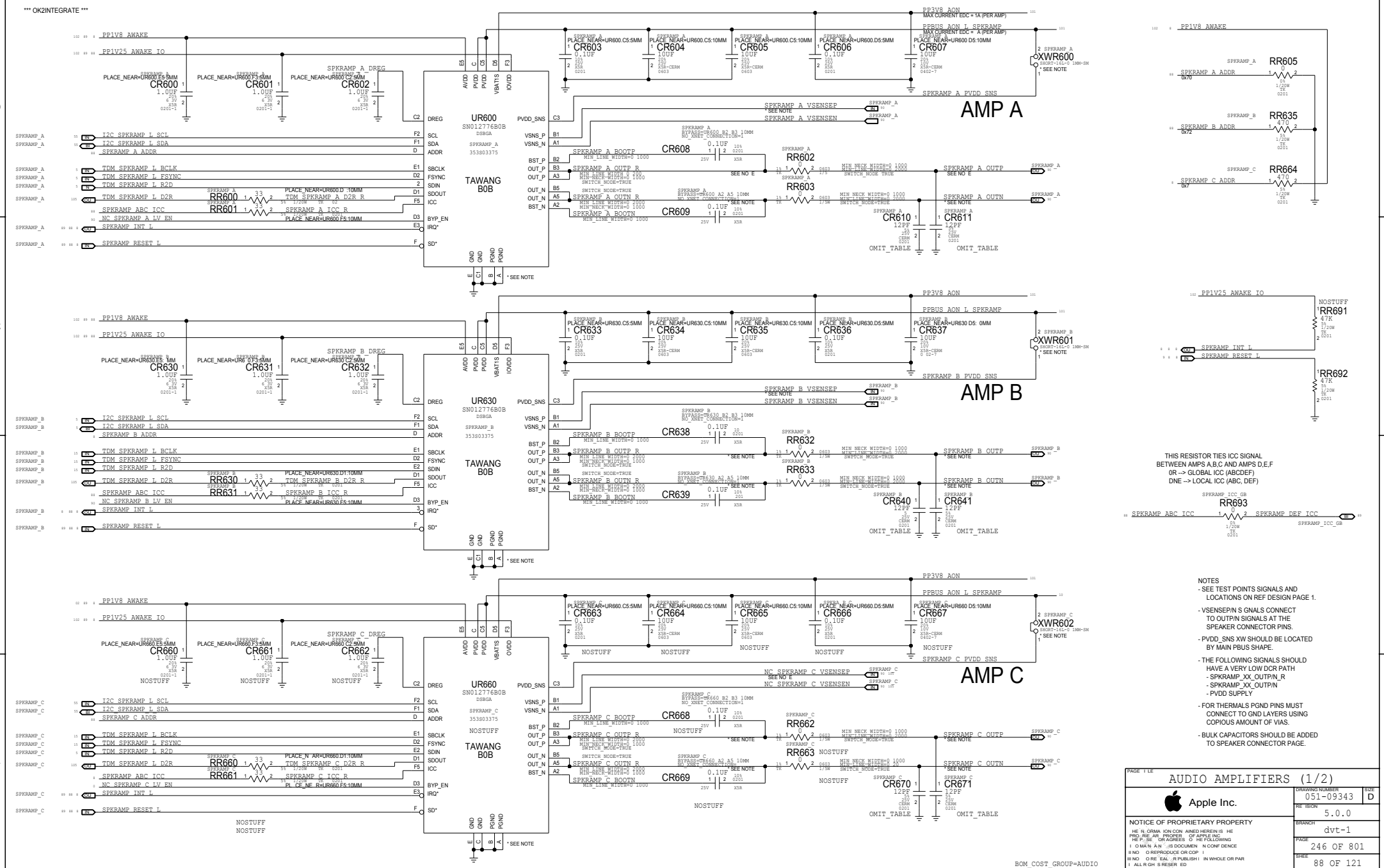
PAGE TITLE
SECDIS: SAK, AMR+LAS

Apple Inc.

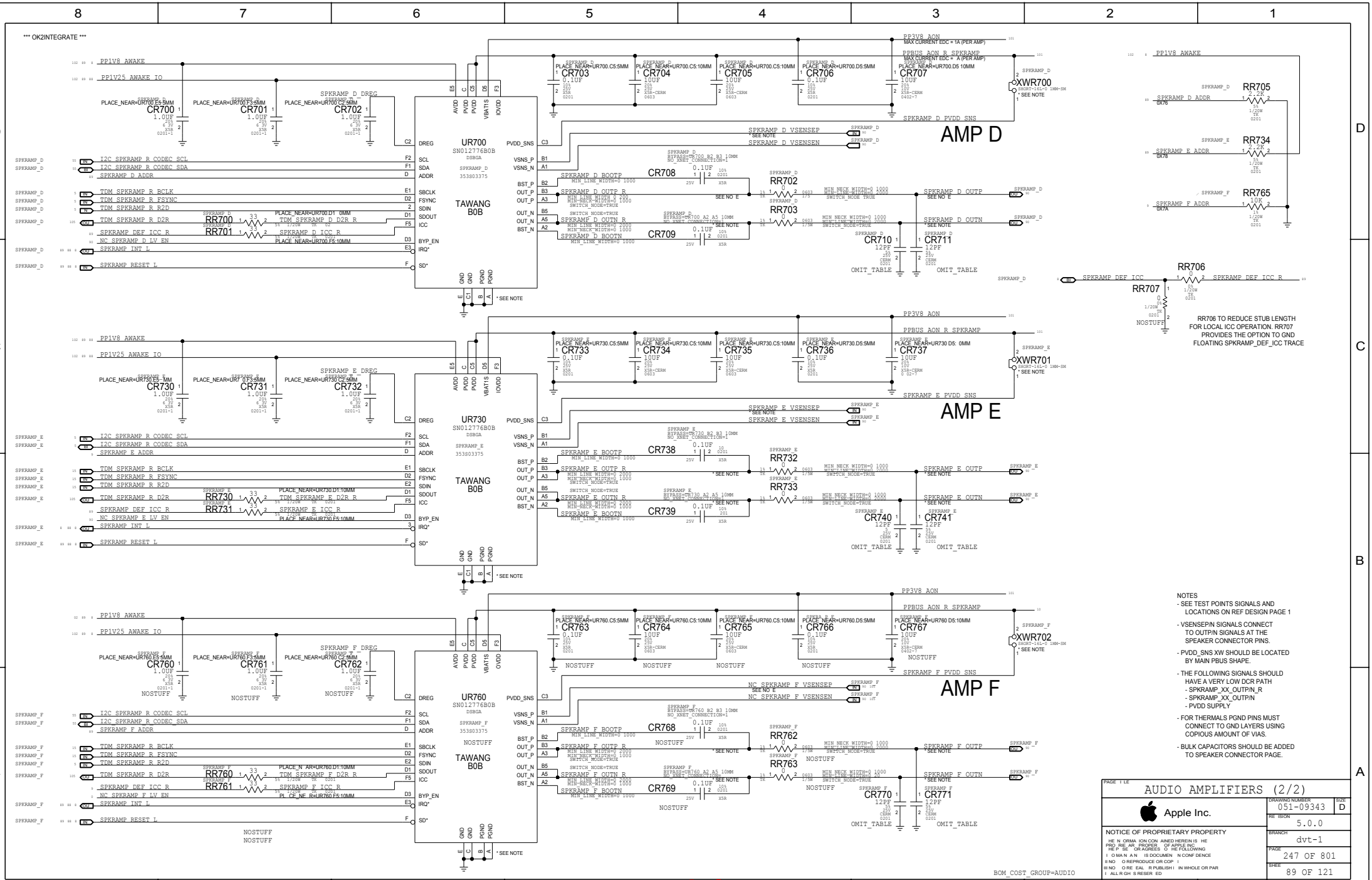
DRAWING NUMBER 051-09343 SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 243 OF 801
SHEET 87 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: (I) TO MAINTAIN IS DOCUMENT IN CONFIDENCE (II) NOT TO REPRODUCE OR COPY IT (III) NOT TO RELEASE PUBLISH IT IN WHOLE OR PART. ALL RIGHTS RESERVED

www.repairlap.com

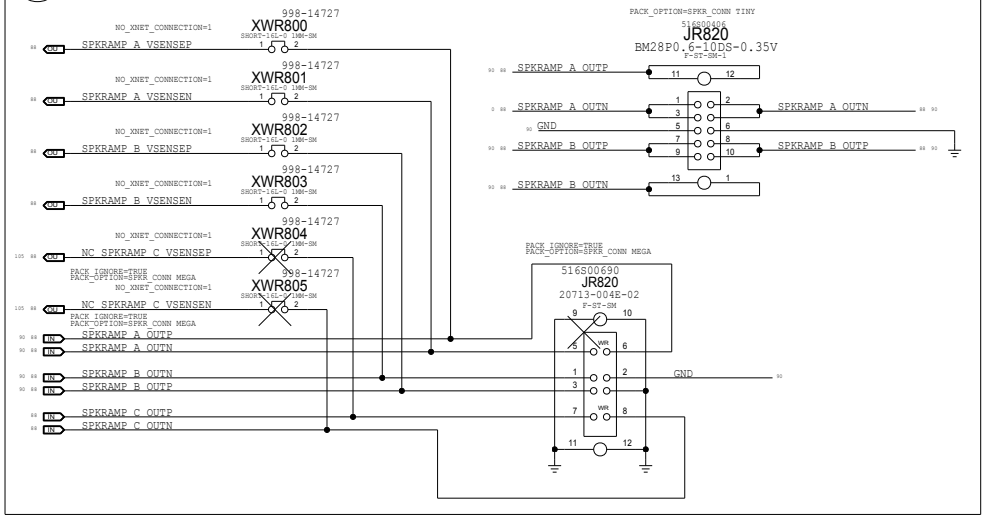


www.repairlap.com

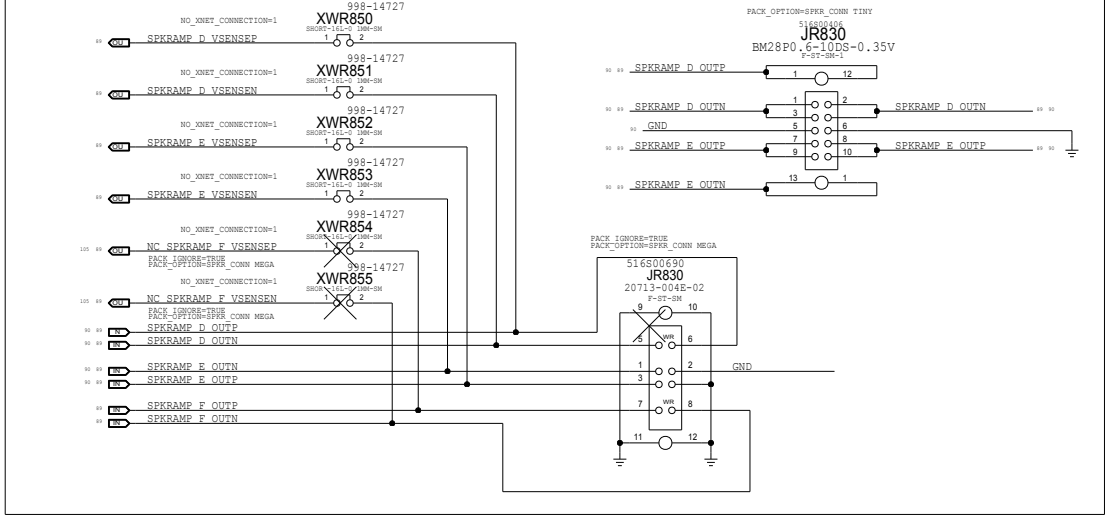


www.repairlap.com

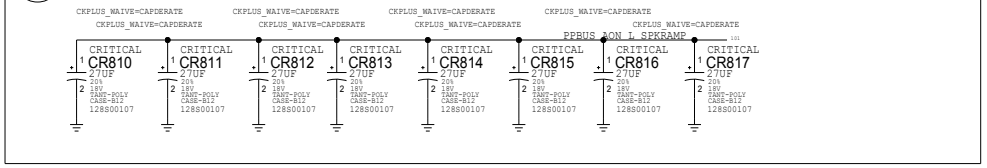
A LEFT SPEAKER CONNECTOR



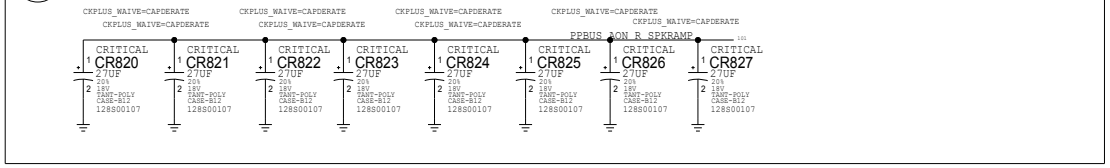
B RIGHT SPEAKER CONNECTOR



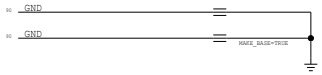
C LEFT SPEAKER AMP BULK CAP



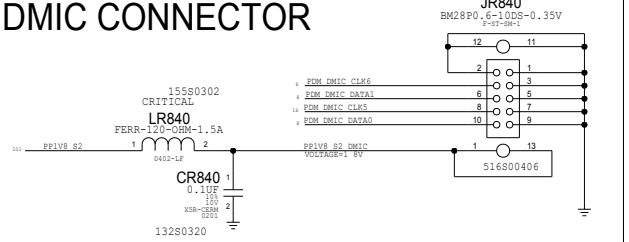
D RIGHT SPEAKER AMP BULK CAP



E SPKR_ID[1:0] protection



F DMIC CONNECTOR



G Unused TPs and MADI

H Desense Cap Table

PAR #	Q	DE CRIP ION	REFERENCE DE IGNA OR(S)	BOM OP ION
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR610,CR611	SPKRAMP_A_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR640,CR641	SPKRAMP_B_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR670,CR671	SPKRAMP_C_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR710,CR711	SPKRAMP_D_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR740,CR741	SPKRAMP_E_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR770,CR771	SPKRAMP_F_DESENSE

BOM_COST_GROUP=AUDIO

PAGE TITLE: Audio Connectors

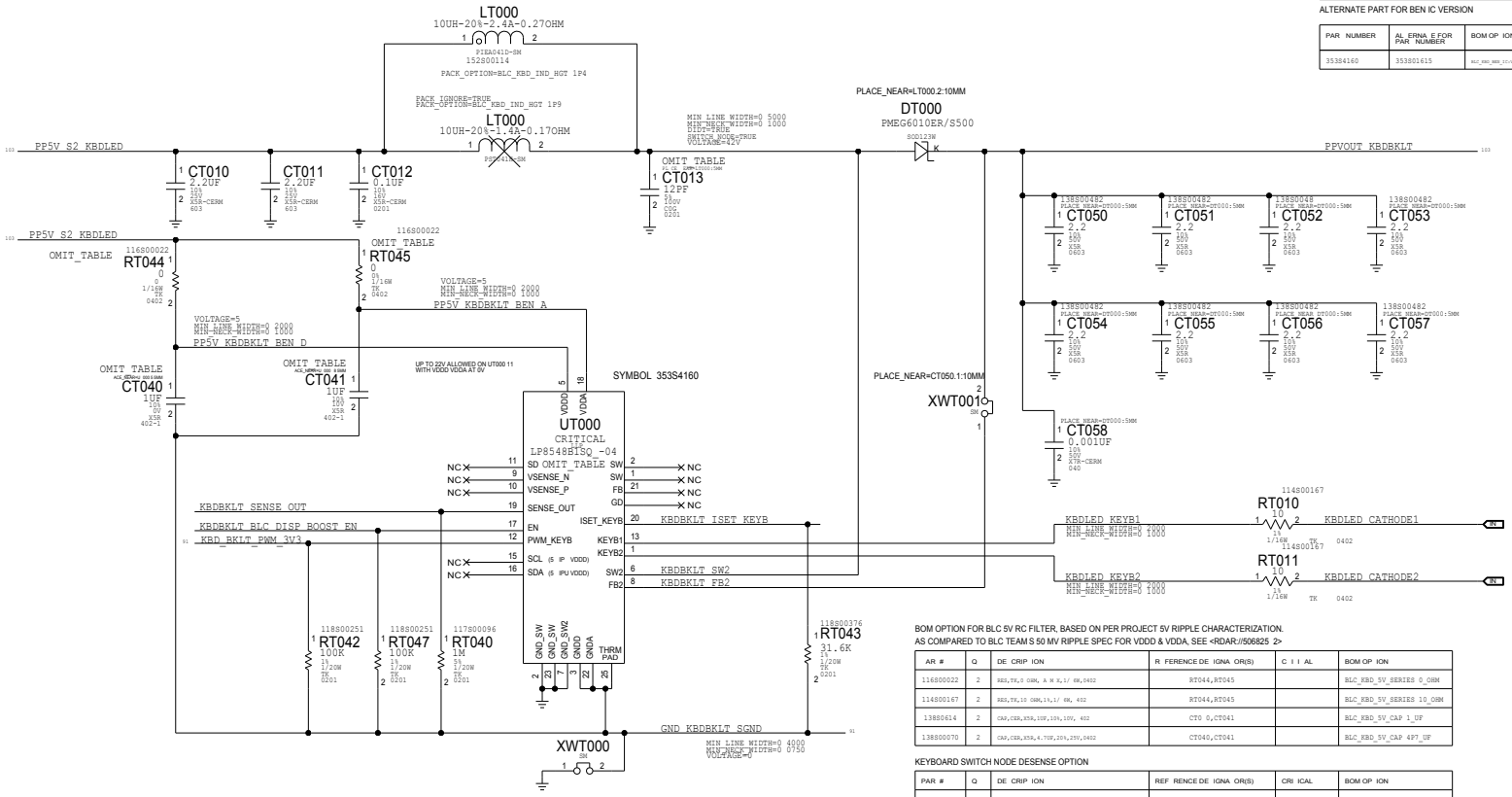
Apple Inc.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (1) MAINTAIN IS DOCUMENT IN CONFIDENCE (2) NOT REPRODUCE OR COPY IT (3) NOT RE-DISTRIBUTE IN WHOLE OR PART. ALL RIGHTS RESERVED

DRAWING NUMBER: 051-09343 SIZE: D
REVISION: 5.0.0
BRANCH: dvt-1
PAGE: 248 OF 801
SHEET: 90 OF 121

www.repairlap.com

A. BLC BEN - KEYBOARD LED DRIVER



BEN IC VERSION VS 6 DEPENDS ON WHICH VERSION OF JERRY IC S ON THE PANEL

AR #	Q	DE CRIP ION	REFERE CE DE IGNA OR(S)	CRI A	BOM OP ION
353S01615	1	IC,LP8548BI-04,DC/DC CVTR,BST,A12S,QFN-24	UT000		BLC_KBD_BEN_IC_V4
353S01685	1	IC,LP8548BI-06,DC/DC CVTR,BST,QFN24	UT000		BLC_KBD_BEN_IC_V6

ALTERNATE PART FOR BEN IC VERSION

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S
35384160	353S01615	BLC_KBD_BEN_IC/V6	ALL	RECOMMENDED BY LOGISA

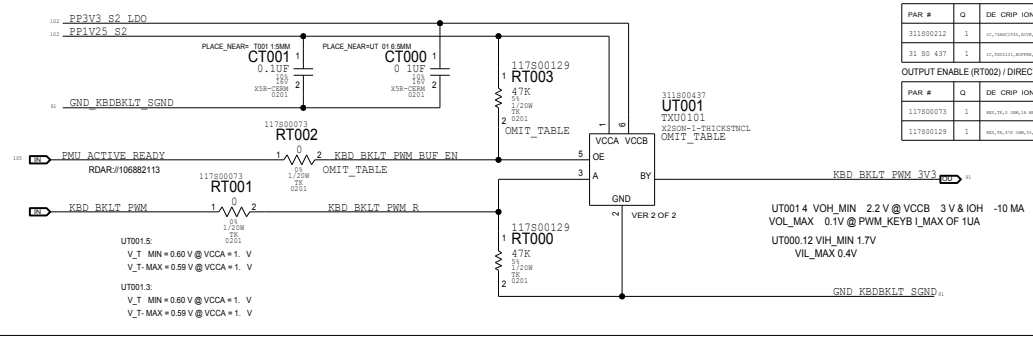
BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION.
AS COMPARED TO BLC TEAM S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR://506825 2>

AR #	Q	DE CRIP ION	R FERENCE DE IGNA OR(S)	C I I AL	BOM OP ION
116800022	2	RES,TK,0 OHM, A W 3,1/ 6W,0402	RT044,RT045		BLC_KBD_5V_SERIES 0_OHM
114800167	2	RES,TK,10 OHM,1%,1/ 6W, 402	RT044,RT045		BLC_KBD_5V_SERIES 10_OHM
13S80614	2	CAP,CER,X5R,10UF,10%,10V, 402	CT0 0,CT041		BLC_KBD_5V_CAP 1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CT040,CT041		BLC_KBD_5V_CAP 4P7_UF

KEYBOARD SWITCH NODE DESENSE OPTION

PAR #	Q	DE CRIP ION	REF RENCE DE IGNA OR(S)	CRI ICAL	BOM OP ION
131S00141	1	CAP,CGL,12P ,5%, 50V,0201	CT013		BLC_KBD_SW_NODE_DESENSE

B. BLC BEN - PWM LEVEL-TRANSLATOR



SOC TO BEN PWM LEVEL-SH FTER BOM TABLE:

PAR #	Q	DE CRIP ION	REFERENCE DE IGNA OR(S)	BOM OP ION
311S00212	1	IC,74AXC1T45,XCTR,1 BIT,2 SFLY,X2SON8	UT001	BLC_KBD_PWM SN74AX
31 S0 437	1	IC,TXU0101,BUFFER, -10K, 8,E CNS	UT001	BLC_KBD_PWM TXU0101

OUTPUT ENABLE (RT002) / DIRECTION (RT003) BOM TABLE: RDAR:/ 106882113

PAR #	Q	DE CRIP ION	REFERENCE DE IGNA OR(S)	BOM OP ION
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	RT002	BLC_KBD_PWM_OE CTL
117S00129	1	RES,TK,47K OHM,5%,1/20W,0201	RT003	BLC_KBD_PWM_OE HI

BOM_COST_GROUP=DISPLAY

PAGE TI LE
BLC: KEYBOARD BACKLIGHT

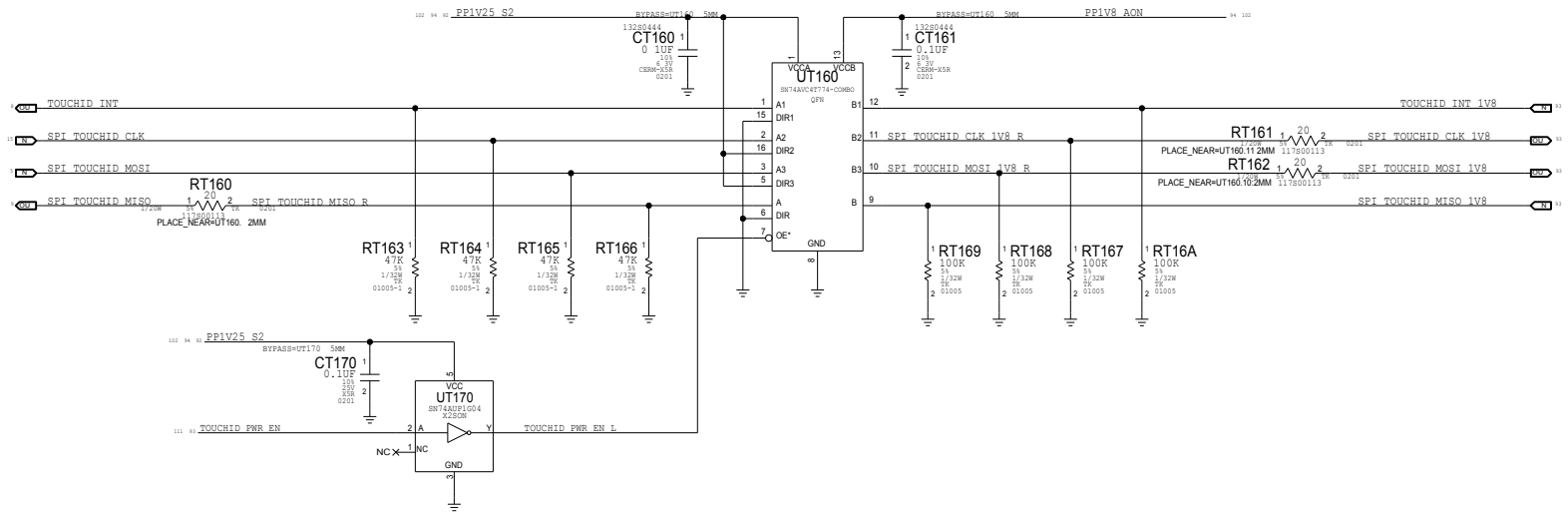
Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
RE ISION 5.0.0
BRANCH dvt-1
PAGE 250 OF 801
SHEE 91 OF 121

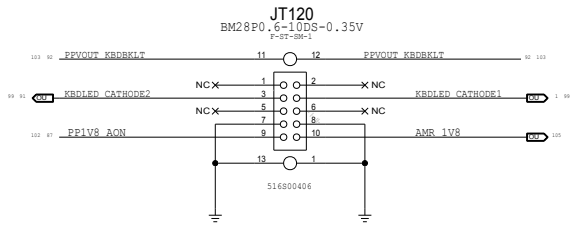
NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC HE P SE OR AGREES O HE FOLLOWING I O MA N A N IS DOCUMEN N CONF DENCE
III NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR
I ALL R GH S RESER ED

www.repairlap.com

A TouchID SPI Bus Level Shifter



B KBD BKLT Connector



Mates with J0200 on AMR KBBL COMBO FLEX
Mates with 516S00407

10/25/2022

PAGE TITLE: Keyboard Support

Apple Inc.

DRAWING NUMBER: 051-09343 | SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

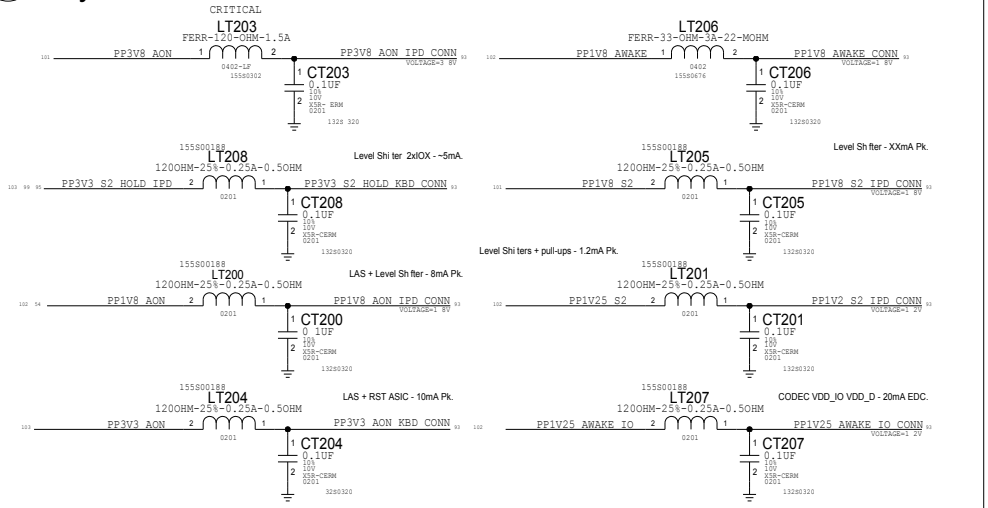
PAGE: 251 OF 801

SHEET: 92 OF 121

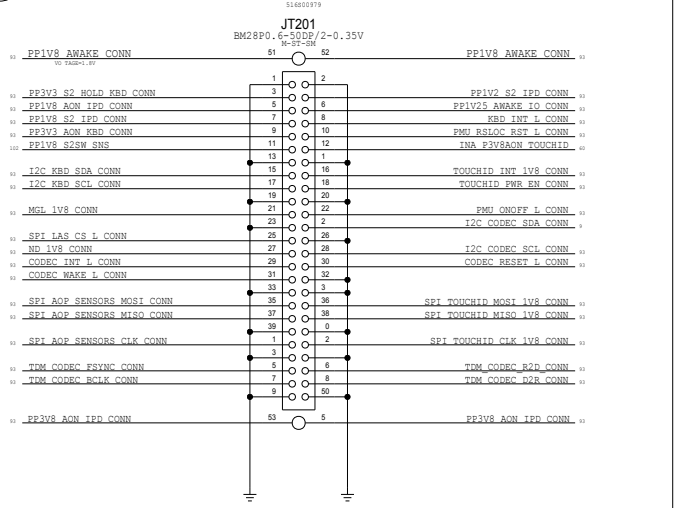
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING
THIS DOCUMENT CONFIDENCE
NOT TO REPRODUCE OR COPY
NOR TO REVEAL PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

A Keyboard Power Filters

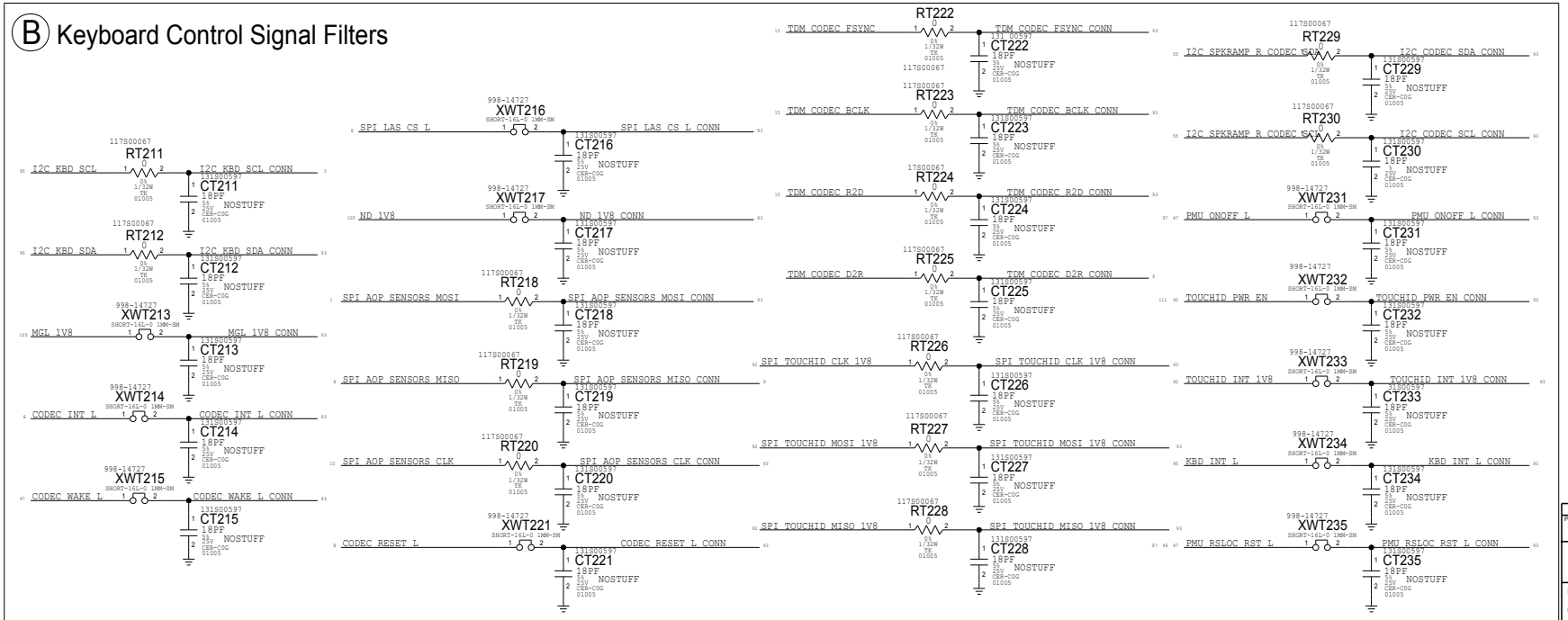


D KBD B2B CONNECTOR



Mates with J0200 516S00978 on MLB-KBDB flex

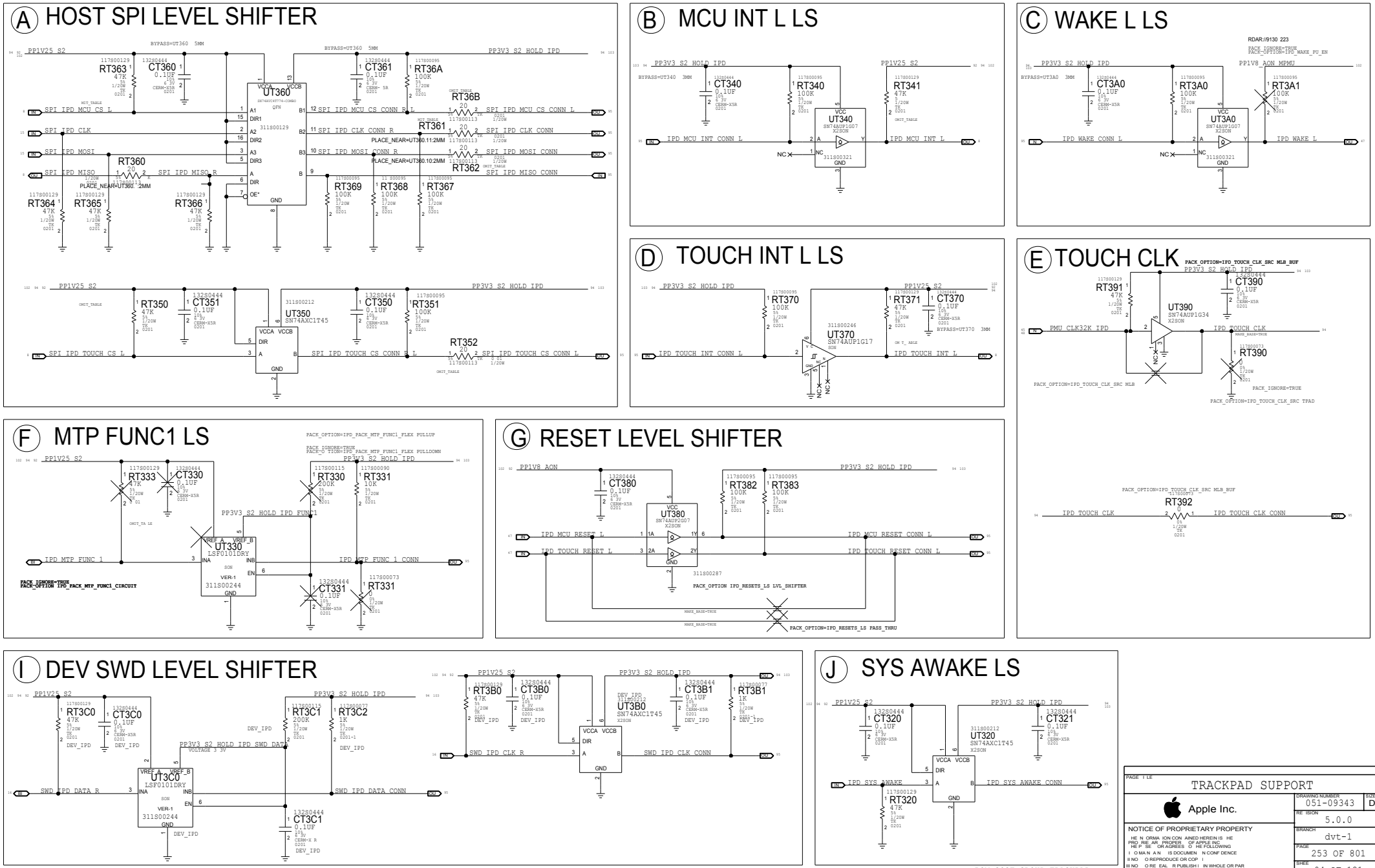
B Keyboard Control Signal Filters



BOM_COST_GROUP=KEYBOARD

10/26/2022	
PAGE TITLE	Keyboard Connector
Apple Inc.	DRAWING NUMBER 051-09343 / SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: 1. TO MAINTAIN CONFIDENTIALITY. 2. NO REPRODUCTION OR COPYING. 3. NO OTHER USE. 4. PUBLISHING IN WHOLE OR PART. ALL RIGHTS RESERVED.	BRANCH dvt-1
	PAGE 252 OF 801
	SHEET 93 OF 121

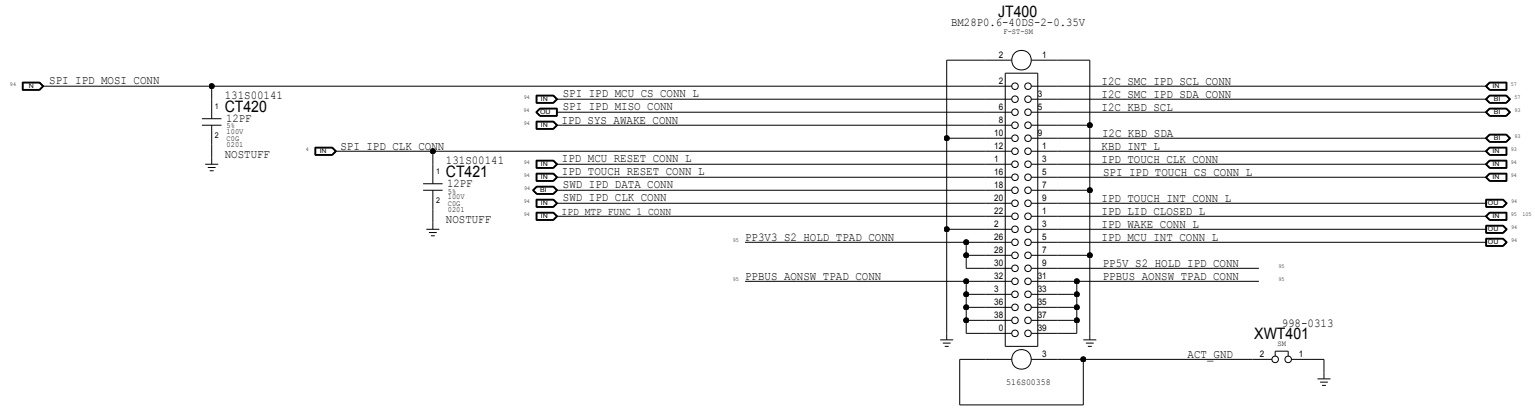
www.repairlap.com



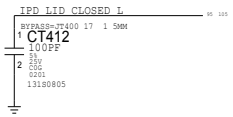
www.repairlap.com

A Trackpad Connector

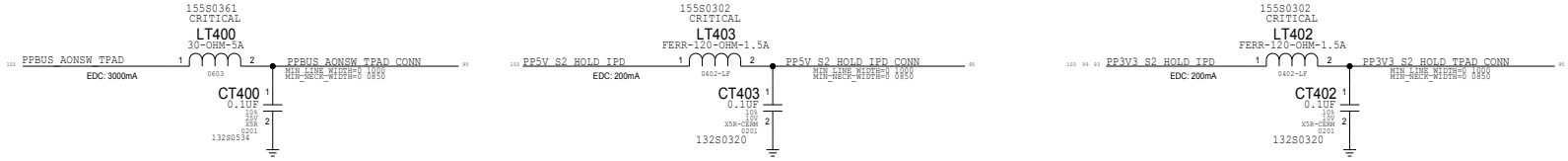
Bottom side contacts used
Pinout reversed from flex



D Trackpad Control



B Trackpad Power Supply Filters



C BOM CALLOUT TABLES

BOM_OPTION=IPD_SPI_CS_R:<0_OHM/20_OHM/33_OHM>
ADD BOMOPTION TO STUFF RT36B,RT352 WITH 0 OHM, 20 OHM, OR 33 OHM
SPI IPD CS L SERIES SOURCE TERMINATION RESISTOR

PAR #	Q	DESCRIP ION	REFERENCE DESIGNA OR(S)	BOM OP ON
117S00073	2	RES,TK,0 OHM,1A MAX,1 20W,020	RT36B,RT352	IPD_SPI_CS_R 0_OHM
117S00113	2	RES,TK,20 OHM,5%,1/20W,0201	RT36B RT352	IPD_SPI_CS_R 20_OHM
117S00122	2	RES,TK,33 OHM,5%,1/20W,0201	RT36B,RT352	IPD_SPI_CS_R 33_OHM

BOMOPTION=DEV_IPD
ADD BOMOPTION TO STUFF SWD LEVEL SH FTERS

YES: STUFF 1 8V->3.3V OPEN DRAIN LS FOR IPD_TOUCH_CLK_CONN
NO : UNSTUFF 1.8V->3.3V OPEN DRA N LS FOR PD_TOUCH_CLK_CONN
THE CIRCUIT IS SETUP TO OUTPUT HIGH WHEN NOT DRIVEN E.G. THROUGH A POWER STATE TRANSITION

USE BOM_OPTION TO SELECT BETWEEN 30K OR 47K PULL-UPS THAT T E TO SOC PINS

PAR #	Q	DESCRIP ION	REFERENC D SIGNA OR(S)	BOM OP ON
118S00521	5	RES,TK,30K OHM,1%, /20W,0201	RT350,R 363, T34 ,RT371	TPAD_SOC_PULLUP 30K
117S00129	5	RES,TK,47K OHM,5%,1/20W 0201	RT350,RT363,RT341 RT371	TPAD_SOC_PULLUP 47K

BOM_OPTION= PD_SPI_CLK_MOSI_R:<20_OHM/51_OHM>
ADD BOMOPTION TO STUFF RT361 and RT362 with 20 OHM or 51 OHM
SPI IPD CS L SERIES SOURCE TERMINATION RESISTOR

PAR #	Q	DESCR P ION	REFERENCE DESIGNA OR(S)	BOM OP ION
117S00113	2	RES,TK,20 OHM,5%,1/20W,0201	RT361,RT362	IPD_SPI_CLK_MOSI_R 20_OHM
118S0 418	2	RES,TK,51 OHM, %,1/20W 0201	RT361,RT362	IPD_SPI_CLK_M SI_R 51_OHM
117S00113	2	RES,TK,20 OHM,5%,1/20W,0201	RT361,RT362	IPD_SPI_CLK_MOSI_R 5_OHM

BOM_COST_GROUP=TRACKPAD

10/26/2022
PAGE I LE
Trackpad Connector
Apple Inc.
DRAWING NUMBER 051-09343
SIZE D
RE ISION 5.0.0
BRANCH dvt-1
PAGE 254 OF 801
SHEE 95 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC
HE P SE OR AGREES O HE FOLLOWING
I O MA N A N IS DOCUMEN N CONF DENCE
II NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR
I ALL R GH S RESER ED

www.repairlap.com

Intentionally Blank

PAGE TITLE

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

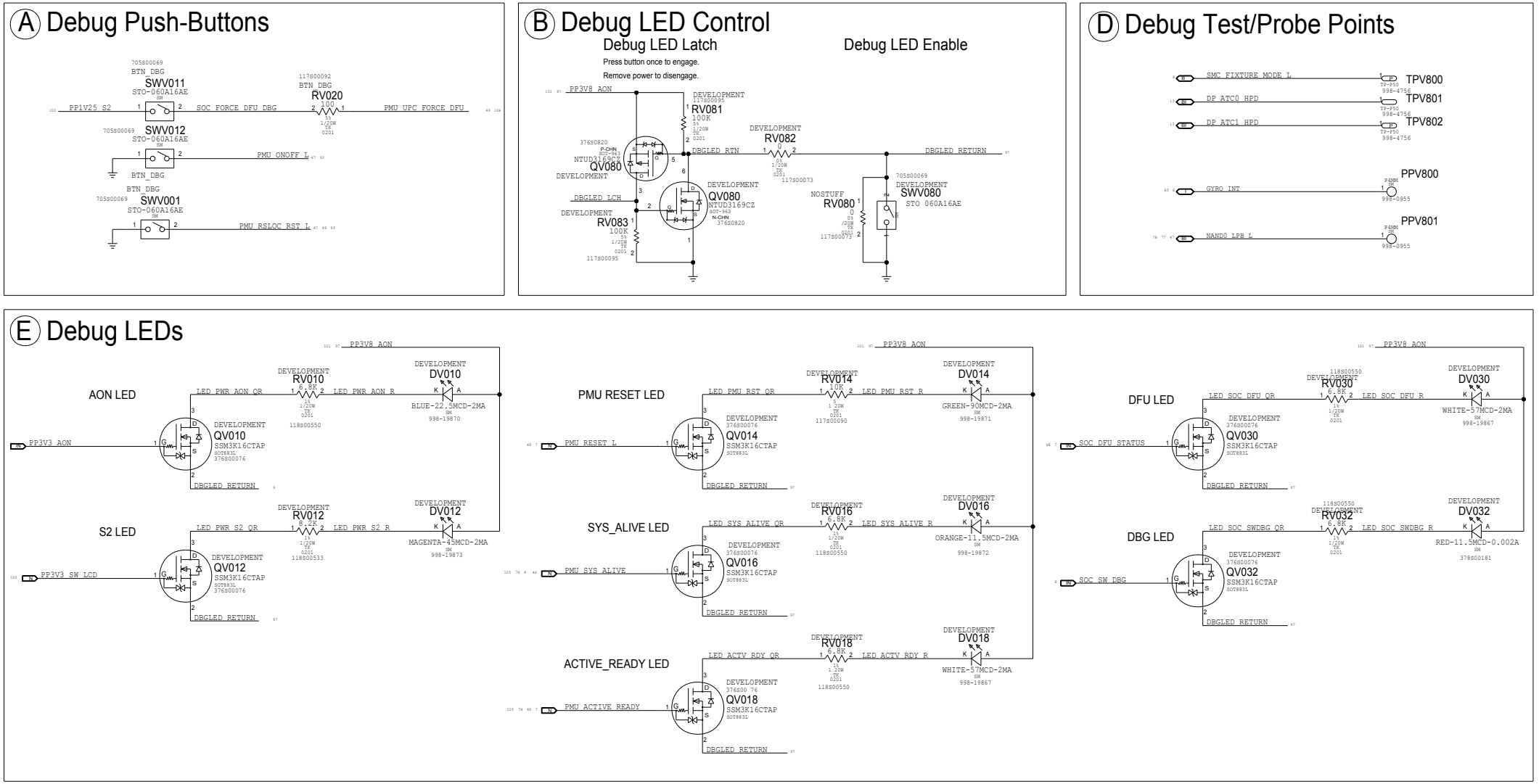
BRANCH dvt-1

PAGE 259 OF 801

SHEET 96 OF 121

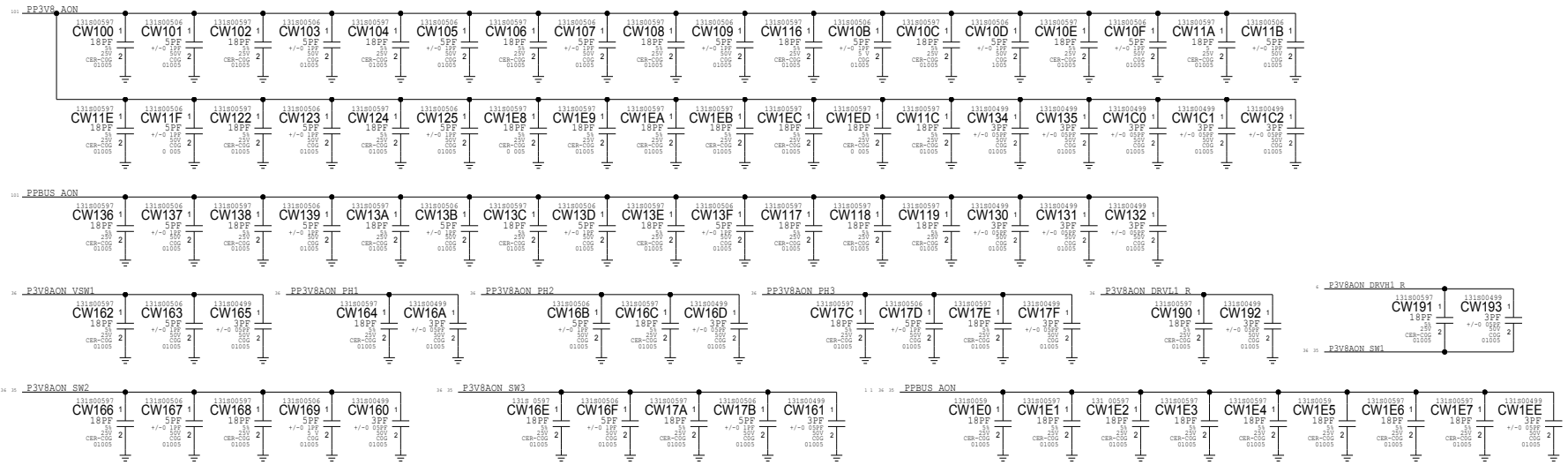
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
2. NOT TO REPRODUCE OR COPY IT
3. NOT TO REVEALPUBLISH IT IN WHOLE OR PART
4. ALL RIGHTS RESERVED

www.repairlap.com

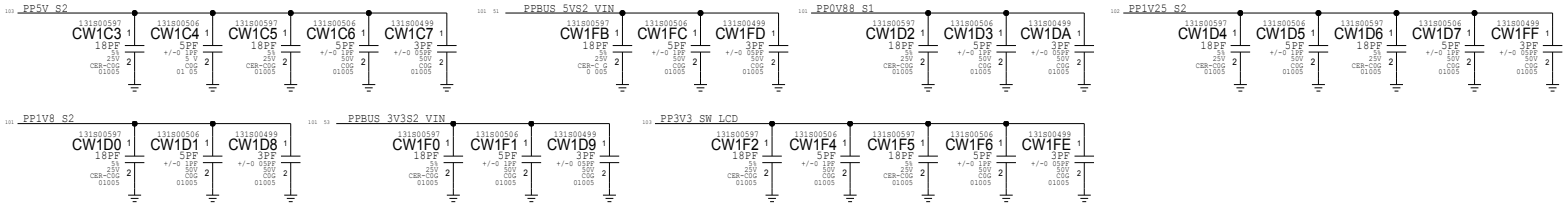


www.repairlap.com

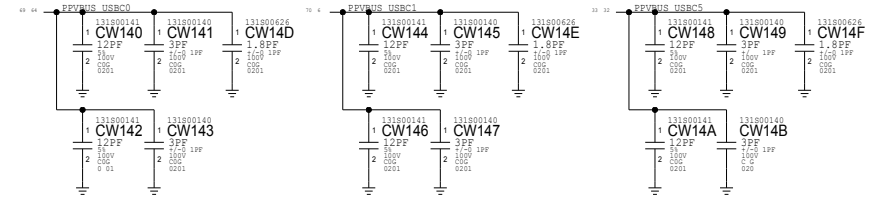
A ICEMAN Desense



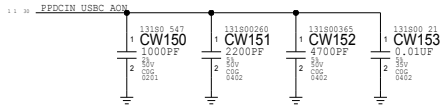
B BUCK POWER Desense



C USB-C Desense



D PDN Noise Mitigation (from PI Team Simulations)



BOM_COST_GROUP=DESENSE

PAGE TITLE	Desense 1
Apple Inc.	DRAWING NUMBER 051-09343 / SIZE D
NOTICE OF PROPRIETARY PROPERTY	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 281 OF 801
	SHEET 98 OF 121

www.repairlap.com

A Display PMIC Desense

PP3V3_SW_LCD
CW200 131800597 18PF 5% 25V CER-C0G 01005
CW201 131800506 5PF +/-0.1PF 50V C0G 01005
CW202 131800597 18PF 5% 25V CER-C0G 01005
CW203 131800506 5PF +/-0.1PF 50V C0G 01005
CW204 131800499 3PF +/-0.05PF 50V C0G 01005

PAVDDP_SDG_SW
CW218 131800597 18PF 5% 25V CER-C0G 01005 NOSTUFF
CW21E 131800499 3PF +/-0.05PF 50V C0G 01005 NOSTUFF

PAVDDN_SDG_SW
CW219 131800597 18PF 5% 25V CER-C0G 01005 NOSTUFF
CW21F 131800499 3PF +/-0.05PF 50V C0G 01005 NOSTUFF

PP1V8_DISP
CW206 131800597 18PF 5% 25V CER-C0G 01005
CW207 131800506 5PF +/-0.1PF 50V C0G 01005
CW20C 131800499 3PF +/-0.05PF 50V C0G 01005

PN_VGL2_MONTEREY
CW208 131800597 18PF 5% 25V CER-C0G 01005
CW209 131800506 5PF +/-0.1PF 50V C0G 01005
CW20D 131800499 3PF +/-0.05PF 50V C0G 01005

PN_VGL1_MONTEREY
CW210 131800597 18PF 5% 25V CER-C0G 01005
CW211 131800506 5PF +/-0.1PF 50V C0G 010 5
CW21C 131800499 3PF +/-0.05PF 50V C0G 01005

P1V8_SDG_SW
CW21B 131800597 18PF 5% 25V CER-C0G 01005 NOSTUFF
CW228 131800499 3PF +/-0.05PF 50V C0G 01005 NOSTUFF

PVGH_BOOST_SDG
CW212 131800597 18PF 5% 25V CER-C0G 01005
CW213 131800506 5PF +/-0.1PF 50V C0G 01005
CW20E 131800499 3PF +/-0.05PF 50V C0G 01005

PAVDDN_SDG_R
CW214 131800597 18PF 5% 25V CER-C0G 01005
CW215 131800506 5PF +/-0.1PF 50V C0G 01005
CW20F 131800499 3PF +/-0.05PF 50V C0G 01005

PAVDDP_SDG_R
CW216 131800597 18PF 5% 25V CER-C0G 01005
CW217 131800506 5PF +/-0.1PF 50V C0G 01005
CW21D 131800499 3PF +/-0.05PF 50V C0G 01005

PVGH_BOOST_SDG_SW
CW21A 131800597 18PF 5% 25V CER-C0G 01005 NOSTUFF
CW229 131800499 3PF +/-0.05PF 50V C0G 01005 NOSTUFF

B Speaker Amplifier Desense

PPBUS_AON_L_SPKRAMP
CW220 131800597 18PF 5% 25V CER-C0G 01005
CW221 131 00506 5PF +/ 0 1PF 50V C0G 01005
CW222 131800059 18PF 5% 25V CER-C0G 01005
CW223 131800506 5PF +/-0.1PF 50V C0G 01005
CW224 131800059 18PF 5% 25V CER-C0G 01005
CW225 131800506 5PF +/-0.1PF 50V C0G 01005
CW226 131800597 18PF 5% 25V CER-C0G 01005
CW227 131800506 5PF +/-0.1PF 50V C0G 01005
CW22A 131800499 3PF +/-0.05PF 50V C0G 01005

PPBUS_AON_R_SPKRAMP
CW230 131800597 18PF 5% 25V CER-C0G 01005
CW231 131800506 5PF +/-0.1PF 50V C0G 01005
CW232 1318005 7 18PF 5% 25V CER-C0G 01005
CW233 131800506 5PF +/-0.1PF 50V C0G 01005
CW234 13 800597 18PF 5% 25V CER-C0G 01005
CW235 131800506 5PF +/-0.1PF 50V C0G 01005
CW236 131800597 18PF 5% 25V CER-C0G 01005
CW237 131800 6 5PF +/-0.1PF 50V C0G 01005
CW23A 131800499 3PF +/-0.05PF 50V C0G 01005

C Display and Keyboard Backlight Desense

PPVOUT_LCDBKLT
CW240 131800141 12PF 5% 100V C0G 0201
CW241 131800140 3PF +/-0.1PF 100V C0G 0201
CW242 131800141 12PF 1 5% 100V C0G 0201
CW243 131800140 3PF +/-0.1PF 100V C0G 0201
CW256 131800499 3PF +/ 0 05PF 50V C0G 01005

PPVOUT_LCDBKLT_SW
CW244 131800141 12PF 5% 100V C0G 0201 NOSTUFF
CW245 131800140 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
CW257 131800499 3PF +/-0.05PF 50V C0G 01005 NOSTUFF

PPVIN_LCDBKLT_Q
CW246 131800141 12PF 5% 100V C0G 0201
CW247 131800140 3PF +/-0.1PF 100V C0G 0201
CW248 131800141 12PF 5% 100V C0G 0201
CW249 131800140 3PF +/-0.1PF 100V C0G 0201
CW24A 131800141 12PF 5% 100V C0G 0201
CW24B 131800140 3PF +/-0.1PF 100V C0G 0201
CW24C 131800141 12PF 5% 100V C0G 0201
CW24D 131800140 3PF +/-0.1PF 100V C0G 0201
CW258 131800499 3PF +/-0.05PF 50V C0G 01005

PPVOUT_LCDBKLT_D
CW24E 131800141 12PF 5% 100V C0G 0201
CW24F 131800140 3PF +/-0.1PF 100V C0G 0201
CW250 131800141 12PF 5% 100V C0G 0201
CW251 131800140 3PF +/-0.1PF 100V C0G 0201
CW252 131800141 12PF 5% 100V C0G 0201
CW253 131800140 3PF +/-0.1PF 100V C0G 0201
CW259 131800499 3PF +/-0.05PF 50V C0G 01005

KBDLED_CATHODE1
CW260 131800141 12PF 5% 100V C0G 0201

PP5V_S2_KBDLED
CW254 131800597 18PF 5% 25V CER-C0G 01005
CW255 131800506 5PF +/-0.1PF 50V C0G 01005
CW25A 131800499 3PF +/-0.05PF 50V C0G 01005

PPVOUT_KBDBKLT
CW25B 131800141 12PF 5% 100V C0G 0201

KBDLED_CATHODE2
CW263 131800141 12PF 5% 100V C0G 0201

D NAND Desense

PP2V5_AWAKE_NAND_VCC
CW270 131800597 18PF 5% 25V CER-C0G 01005
CW271 131800506 5PF +/-0.1PF 50V C0G 01005
CW272 131800597 18PF 5% 25V CER-C0G 01005
CW273 131800506 5PF +/-0.1PF 50V C0G 01005
CW274 131800597 18PF 5% 25V CER-C0G 01005
CW275 131800506 5PF +/-0.1PF 50V C0G 01005
CW276 131800597 18PF 5% 25V CER-C0G 01005
CW277 131800506 5PF +/-0.1PF 50V C0G 01005
CW278 131800597 18PF 5% 25V CER-C0G 01 05
CW279 131800506 5PF +/-0.1PF 50V C0G 01005
CW288 131800499 3PF +/-0.05PF 50V C0G 01005
CW27A 131800597 18PF 5% 25V CER-C0G 01005
CW27B 131800506 5PF +/-0.1PF 50V C0G 01005
CW27C 131800597 18PF 5% 25V CER-C0G 01005
CW27D 131800506 5PF +/-0.1PF 50V C0G 0 005
CW27E 131800597 18PF 5% 25V CER-C0G 01005
CW27F 131800506 5PF +/-0.1PF 50V C0G 01005
CW280 131800597 18PF 5% 25V CER-C0G 01005
CW281 131800506 5PF +/-0.1PF 50V C0G 01005
CW282 131800597 18PF 5% 25V CER-C0G 01005
CW283 131800506 5PF +/-0.1PF 50V C0G 01005
CW289 131800499 3PF +/-0.05PF 50V C0G 01005

PP1V25_AWAKE_NAND_VCCQ
CW284 131800597 18PF 5% 25V CER-C0G 01005
CW285 131800506 5PF +/-0.1PF 50V C0G 01005
CW286 131800597 18PF 5% 25V CER-C0G 01005
CW287 131800506 5PF +/-0.1PF 50V C0G 01005
CW292 131800499 3PF +/-0.05PF 50V C0G 01005
CW294 131800597 18PF 5% 25V CER-C0G 01005
CW295 131800506 5PF +/-0.1PF 50V C0G 01005

PP0V88_AWAKE_NAND_VDD
CW28A 131800597 18PF 5% 25V CER-C0G 01005
CW28B 131800506 5PF +/-0.1PF 50V C0G 01005
CW28C 131800597 18PF 5% 25V CER-C0G 01005
CW28D 131800506 5PF +/-0.1PF 50V C0G 01005
CW28E 131800597 18PF 5% 25V CER-C0G 01005
CW28F 131800506 5PF +/-0.1PF 50V C0G 01005
CW290 131800597 18PF 5% 25V CER-C0G 01005
CW291 131800506 5PF +/-0.1PF 50V C0G 01005
CW293 131800499 3PF +/-0.05PF 50V C0G 01005

E Camera Desense

PP5V_S2_CAMERA_FILT
CW2A0 131800597 18PF 5% 5V CER-C0G 01005
CW2A1 131800499 3PF +/-0.05PF 50V C0G 01005
CW2A2 131800506 5PF + -0.1PF 50V C0G 01005

F Trackpad Desense

PP3V3_S2_HOLD_IPD
PLACE_NEAR=LT 02.1:5MM
CW2B0 131800597 18PF 5% 25V CER-C0G 01005
CW2B1 131800506 5PF +/-0.1PF 50V C0G 01005
CW2B3 131800499 3PF +/-0.05PF 50V C0G 01005

G Display TCON Desense

SPI_TCON_CLK
CW2C0 131800597 18PF 5% 25V CER-C0G 01005
CW2C3 131800499 3PF +/-0.05PF 50V C0G 01005

SPI_TCON_MISO
CW2C1 131800597 18PF 5% 25V CER-C0G 01005
CW2C4 131800499 3PF +/-0.05PF 50V C0G 01005

SPI_TCON_MOSI
CW2C2 131800597 18PF 5% 25V CER-C0G 01005
CW2C5 131800499 3PF +/-0.05PF 50V C0G 01005

BOM_COST_GROUP=DESENSE

PAGE TITLE: Desense 2

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: THIS DOCUMENT CONTAINS NO REPRODUCTION OR COPYING. THIS DOCUMENT CONTAINS NO TRADE SECRETS. THIS DOCUMENT CONTAINS NO PUBLISHING IN WHOLE OR PART. ALL RIGHTS RESERVED.

DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	282 OF 801
SHEET	99 OF 121

www.repairlap.com

Ⓐ SOC Desense

PPVDD_AWAKE_PCPU

CW300 18PF	CW301 5PF	CW30A 3PF

PPVDD_AWAKE_PCPU

CW302 18PF	CW303 5PF	CW30B 3PF

PPVDD_AWAKE_CPU_SRAM

CW304 18PF	CW305 5PF	CW30C 3PF

PPVDD_AWAKE_CPU_SRAM

CW306 18PF	CW307 5PF	CW30D 3PF

PPVDD_S1_SOC

CW308 18PF	CW309 5PF	CW30E 3PF

PPVDD_S1_SOC

CW310 18PF	CW311 5PF	CW30F 3PF

PPVDD_S1_DCS

CW312 18PF	CW313 5PF	CW31A 3PF

PPVDD_S1_DCS

CW314 18PF	CW315 5PF	CW31B 3PF

PP0V779_S1_SRAM

CW316 18PF	CW317 5PF	CW31C 3PF

PP0V779_S1_SRAM

CW318 18PF	CW319 5PF	CW31D 3PF

PPVDD_S1_DISP

CW320 18PF	CW321 5PF	CW31E 3PF

PPVDD_S1_DISP

CW322 18PF	CW323 5PF	CW31F 3PF

PPVDD_AWAKE_GPU

CW324 18PF	CW325 5PF	CW32A 3PF

PPVDD_AWAKE_GPU

CW326 18PF	CW327 5PF	CW32B 3PF

PP1V05_S2SW_VDD2H

CW328 18PF	CW329 5PF	CW32C 3PF

PP1V05_S2SW_VDD2H

CW330 18PF	CW331 5PF	CW32D 3PF

PP1V12_S2SW_AMPH

CW332 18PF	CW333 5PF	CW32E 3PF

PP1V12_S2SW_AMPH

CW334 18PF	CW335 5PF	CW32F 3PF

PPVDD_AWAKE_ECPU

CW336 18PF	CW337 5PF	CW35B 3PF

PPVDD_AWAKE_ECPU

CW338 18PF	CW339 5PF	CW35C 3PF

PP1V2_AWAKE_PLL

CW33A 18PF	CW33B 5PF	CW35D 3PF

PP0V72_S2_VDD_LOW

CW33C 18PF	CW33D 5PF	CW35E 3PF

PP0V78_S1_VDD_FIXED

CW33E 18PF	CW33F 5PF	CW35F 3PF

PP1V2_S2_CIO

CW340 18PF	CW341 5PF	CW342 18PF	CW343 5PF	CW344 18PF	CW345 5PF	CW360 3PF	CW361 3PF	CW362 3PF

PP1V8_S2SW

CW346 18PF	CW347 5PF	CW348 18PF	CW349 18PF	CW34A 5PF	CW34B 18PF	CW34C 5PF	CW34D 18PF	CW34E 5PF	CW363 3PF	CW364 3PF	CW365 3PF	CW366 3PF

PP0V5_S1_VDDQL

CW34F 18PF	CW350 5PF	CW351 18PF	CW352 5PF	CW353 18PF	CW354 5PF	CW355 18PF	CW356 5PF	CW357 18PF	CW358 5PF	CW359 18PF	CW35A 5PF	CW367 3PF	CW368 3PF	CW369 3PF	CW36A 3PF	CW36B 3PF	CW36C 3PF

BOM_COST_GROUP=DESENSE

PAGE TITLE	Desense 3
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
NOTICE OF PROPRIETARY PROPERTY	BRANCH dvt-1
	PAGE 283 OF 801
	SHEET 100 OF 121

www.repairlap.com

USBC DCIN

PPDCIN_USBC_AON

PBUS

PPBUS_AON

PPBUS_5VS2_VIN

PPBUS_3V3S2_VIN

PPBUS_AON_L_SPKRAMP

PPBUS_AON_R_SPKRAMP

P3V8 VDD_MAIN

PP3V8_AON

P3V8 VDD_MAIN WLBT

PP3V8_AON_WLBT

MPMU BUCK 0

PPVDD_AWAKE_PCPU

MPMU BUCK 1

PPVDD_AWAKE_GPU

MPMU BUCK 2

PPVDD_S1_SOC

MPMU BUCK 3

PP1V8_S2

MPMU BUCK 4

PP1V05_S2SW_VDD2H

Powers Unuse MPMU LDO16

SPMU BUCK 5

PP0V779_S1_SRAM

SPMU BUCK 6

PP2V58_AWAKE_NAND_VCC

MPMU BUCK 7

PPVDD_AWAKE_CPU_SRAM

SPMU BUCK 8

PPVDD_S1_DISP

MPMU BUCK 9

PPVDD_S1_DCS

SPMU BUCK 10

PP0V5_S1_VDDQL

MPMU BUCK 11

PPVDD_AWAKE_ECPU

SPMU BUCK 12

PP0V88_S1

P5V LDO5

PP5V_AON

PAGE TITLE	POWER ALIASES 1
Apple Inc.	DRAWING NUMBER 051-09343 SIZE D
	REVISION 5.0.0
	BRANCH dvt-1
	PAGE 400 OF 801
	SHEET 101 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO BY THE FOLLOWING THIS DOCUMENT CONTAINS CONFIDENCE INFORMATION. NO REPRODUCE OR COPY IN WHOLE OR PART WITHOUT PRIOR WRITTEN PERMISSION. ALL RIGHTS RESERVED.

www.repairlap.com

MPMU BUCK 13

PP1V25_S2 → PP1V25_S2
MAKE_BASE=TRUE
MIN_TRUE_WIDTH=0.0750
MIN_LINE_WIDTH=0.1000

PP1V25_S2 (43)
PP1V25_S2 (98)
PP1V25_S2 (4)
PP1V25_S2 (43)
PP1V25_S2 (38)
PP1V25_S2 (39)
PP1V25_S2 (39)
PP1V25_S2 (47)
PP1V25_S2 (24)
PP1V25_S2 (25)
PP1V25_S2 (7)
PP1V25_S2 (56)
PP1V25_S2 (5)
PP1V25_S2 (57)
PP1V25_S2 (57)
PP1V25_S2 (56)
PP1V25_S2 (87)
PP1V25_S2 (63)
PP1V25_S2 (31)
PP1V25_S2 (33 34)
PP1V25_S2 (65 66 67 69 70 72)
PP1V25_S2 (80)
PP1V25_S2 (93)
PP1V25_S2 (92 94)
PP1V25_S2 (74)
PP1V25_S2 (82)
PP1V25_S2 (71)
PP1V25_S2 (71)
PP1V25_S2 (55)
PP1V25_S2
PP1V25_S2 (44)
PP1V25_S2 (91)
PP1V25_S2 (2)
PP1V25_S2 (75)
PP1V25_S2 (16)

SPMU BUCK 14

PP1V12_S2SW_AMPH → PP1V12_S2SW_AMPH
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8V

PP1V12_S2SW_AMPH (22)
PP1V12_S2SW_AMPH (38)
PP1V12_S2SW_AMPH (100)

MPMU BUCK 3 SW 1

PP1V8_AWAKE → PP1V8_AWAKE
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8V

PP1V8_AWAKE (14)
PP1V8_AWAKE (3)
PP1V8_AWAKE (8)

MPMU BUCK 3 SW 2

PP1V8_S2SW_SNS → PP1V8_S2SW_SNS
MAKE_BASE=TRUE

PP1V8_S2SW_SNS (93)
PP1V8_S2SW_SNS (58 59 60)

MPMU BUCK 13 SW 3

PP1V25_AWAKE_IO → PP1V25_AWAKE_IO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.25V

PP1V25_AWAKE_IO (5 24 25)
PP1V25_AWAKE_IO (16)
PP1V25_AWAKE_IO (14)
PP1V25_AWAKE_IO (14)
PP1V25_AWAKE_IO (7 12)
PP1V25_AWAKE_IO (55)
PP1V25_AWAKE_IO (47)
PP1V25_AWAKE_IO (68)
PP1V25_AWAKE_IO (93)
PP1V25_AWAKE_IO (88 89)
PP1V25_AWAKE_IO (81)

SPMU BUCK 3 SW 4

PP1V8_AWAKE_SPMU_GPIO → PP1V8_AWAKE_SPMU_GPIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8V

SPMU BUCK 13 SW 5

PP1V25_AWAKE_NAND_VCCQ → PP1V25_AWAKE_NAND_VCCQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.25V

PP1V25_AWAKE_NAND_VCCQ (77 78)
PP1V25_AWAKE_NAND_VCCQ (89)

SPMU BUCK 12 SW 6/7

PP0V88_AWAKE_NAND_VDD → PP0V88_AWAKE_NAND_VDD
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=0.88V

PP0V88_AWAKE_NAND_VDD (77)
PP0V88_AWAKE_NAND_VDD (78)
PP0V88_AWAKE_NAND_VDD (89)

SPMU BUCK 12 SW 7

TIED TO SW6

MPMU LDO 1

NC_MPMU_VLDO1 → NC_MPMU_VLDO1
MAKE_BASE=TRUE
NO_TEST=1

MPMU LDO 2

PP1V8_AON → PP1V8_AON
MAKE_BASE=TRUE
VOLTAGE=1.8V

PP1V8_AON (44)
PP1V8_AON (87 92)
PP1V8_AON (54 84)
PP1V8_AON (54 93)
PP1V8_AON (82 94)
PP1V8_AON (52)
PP1V8_AON (81)
PP1V8_AON
PP1V8_AON
PP1V8_AON

MPMU LDO 3

NC_MPMU_VLDO3 → NC_MPMU_VLDO3
MAKE_BASE=TRUE
NO_TEST=

SPMU LDO 4

PP0V72_S2_VDD_LOW → PP0V72_S2_VDD_LOW
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=0.72V

PP0V72_S2_VDD_LOW (39)
PP0V72_S2_VDD_LOW (25)
PP0V72_S2_VDD_LOW (1 0)

MPMU LDO 5

NC_MPMU_VLDO5 → NC_MPMU_VLDO5
MAKE_BASE=TRUE
NO_TEST=1

SPMU LDO 6

NC_SPMU_VLDO6 → NC_SPMU_VLDO6
MAKE_BASE=TRUE
NO_TEST=1

MPMU LDO 7

PP3V3_S2_LDO → PP3V3_S2_LDO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3V

PP3V3_S2_LDO (44)
PP3V3_S2_LDO (69 70)
PP3V3_S2_LDO (3)
PP3V3_S2_LDO (71)
PP3V3_S2_LDO (7)
PP3V3_S2_LDO (7)
PP3V3_S2_LDO (72)
PP3V3_S2_LDO (91)

MPMU LDO 8

PP1V2_AWAKE_PLL → PP1V2_AWAKE_PLL
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000
VOLTAGE=1.2V

PP1V2_AWAKE_PLL (44)
PP1V2_AWAKE_PLL (24)
PP1V2_AWAKE_PLL (100)
PP1V2_AWAKE_PLL (24)

MPMU LDO 9

PP1V8_AON_MPMU → PP1V8_AON_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8V

PP1V8_AON_MPMU (44 46)
PP1V8_AON_MPMU (45 47 48)
PP1V8_AON_MPMU (31)
PP1V8_AON_MPMU (9)

MPMU LDO 9B

PP1V2_AON_MPMU → PP1V2_AON_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.1000
VOLTAGE=1.2V

PP1V2_AON_MPMU (4)
PP1V2_AON_MPMU (4)
PP1V2_AON_MPMU (87)

SYNC DATE=

PAGE TITLE
POWER ALIASES 2

Apple Inc.

DRAWING NUMBER 051-09343 | SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 401 OF 801
SHEET 102 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO BY THE FOLLOWING
1. THIS DOCUMENT CONFIDENTIAL
2. NO REPRODUCTION OR COPY
3. NO OTHER USE, PUBLISHING IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

SPMU LDO 9

PP1V8_AON_SPMU — PP1V8_AON_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8V
PP1V8_AON_SPMU

SPMU LDO 9B

PP1V2_AON_SPMU — PP1V2_AON_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.2V
PP1V2_AON_SPMU
PP1V2_AON_SPMU

MPMU LDO 10

PP3V3_AON — PP3V3_AON
MAKE_BASE=TRUE
VOLTAGE=3.3V
PP3V3_AON
PP3V3_AON
PP3V3_AON

MPMU LDO 11

PP0V855_S2SW_CIO — PP0V855_S2SW_CIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000
VOLTAGE=0.855V
PP0V855_S2SW_CIO
PP0V855_S2SW_CIO

SPMU LDO12

PP0V78_S1_VDD_FIXED — PP0V78_S1_VDD_FIXED
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=0.805V
PP0V78_S1_VDD_FIXED
PP0V78_S1_VDD_FIXED
PP0V78_S1_VDD_FIXED
PP0V78_S1_VDD_FIXED
PP0V78_S1_VDD_FIXED

UP701 Input

NC_PPPANEL_LCD_SW_VIN — NC_PPPANEL_LCD_SW_VIN
MAKE_BASE=TRUE
O_FUSE=1

UC710 - 3V3_SW_LCD

PP3V3_SW_LCD — PP3V3_SW_LCD
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

Sourced from PBus
Enabled by EDP_PANEL_PWR_EN

PP3V3_SW_LCD
PP3V3_SW_LCD
PP3V3_SW_LCD
PP3V3_SW_LCD
PP3V3_SW_LCD
PP3V3_SW_LCD
PP3V3_SW_LCD

UC300 - 5V S2

PP5V_S2 — PP5V_S2
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=5V
MAKE_BASE=TRUE

Sourced from PBus
Enabled by P5VS2_PWR_EN

PP5V_S2
PP5V_S2
PP5V_S2
PP5V_S2
PP5V_S2
PP5V_S2
PP5V_S2
PP5V_S2
PP5V_S2
PP5V_S2
PP5V_S2

Trackpad - 5V S2

PP5V_S2_HOLD_IPD — PP5V_S2_HOLD_IPD
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S2_HOLD_IPD

MPMU LDO13

NC_PPVOUT_MPMU_VLDO13_REG — NC_PPVOUT_MPMU_VLDO13_REG
MAKE_BASE=TRUE
NC_PPVOUT_MPMU_VLDO13_REG

MPMU LDO14

NC_MPMU_VLDO14 — NC_MPMU_VLDO14
MAKE_BASE=TRUE
NO_TEST=1

SPMU LDO15

NC_SPMU_VLDO15 — NC_SPMU_VLDO15
MAKE_BASE=TRUE
NO_TEST=1

MPMU LDO16

NC_MPMU_VLDO16 — NC_MPMU_VLDO16
MAKE_BASE=TRUE
NO_TEST=1

SPMU LDO17

NC_SPMU_VLDO17 — NC_SPMU_VLDO17
MAKE_BASE=TRUE
NO_TEST=1

SPMU LDO18

NC_SPMU_VLDO18 — NC_SPMU_VLDO18
MAKE_BASE=TRUE
NO_TEST=1

PP3V3_S2_HOLD_IPD — PP3V3_S2_HOLD_IPD
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0800
VOLTAGE=3.3V
PP3V3_S2_HOLD_IPD
PP3V3_S2_HOLD_IPD
PP3V3_S2_HOLD_IPD

PP5V_S2_CAMERA_FILT — PP5V_S2_CAMERA_FILT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
VOLTAGE=5V
PP5V_S2_CAMERA_FILT

PP5V_SW_MINNIE — PP5V_SW_MINNIE
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=5V
PP5V_SW_MINNIE

PP1V25_SW_MINNIE — PP1V25_SW_MINNIE
MAKE_BASE=TRUE
VOLTAGE=1.25V
PP1V25_SW_MINNIE
PP1V25_SW_MINNIE

PP1V8_S2SW — PP1V8_S2SW
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
PP1V8_S2SW
PP1V8_S2SW

Keyboard Backlight - 5V S2

PP5V_S2_KBDLED — PP5V_S2_KBDLED
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S2_KBDLED
PP5V_S2_KBDLED
PP5V_S2_KBDLED

PPBUS_AONSW_TPAD — PPBUS_AONSW_TPAD
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.35V
PPBUS_AONSW_TPAD

Digital Ground

GND
VOLTAGE=0V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

MPMU LDO19

(NOT USED)

MPMU LDO20

PP1V2_S2_CIO — PP1V2_S2_CIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000
VOLTAGE=1.2V
PP1V2_S2_CIO
PP1V2_S2_CIO
PP1V2_S2_CIO

MPMU LDOINT

PP1V5_LDOINT_MPMU — PP1V5_LDOINT_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.5V
PP1V5_LDOINT_MPMU
PP1V5_LDOINT_MPMU
PP1V5_LDOINT_MPMU
PP1V5_LDOINT_MPMU
PP1V5_LDOINT_MPMU

SPMU LDOINT

PP1V5_LDOINT_SPMU — PP1V5_LDOINT_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.5V
PP1V5_LDOINT_SPMU
PP1V5_LDOINT_SPMU
PP1V5_LDOINT_SPMU

MPMU VDD BOOST

PP5V_MPMU_BSTLQ — PP5V_MPMU_BSTLQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=5V
PP5V_MPMU_BSTLQ

SPMU VDD BOOST

PP5V_SPMU_BSTLQ — PP5V_SPMU_BSTLQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=5V
PP5V_SPMU_BSTLQ

MPMU LDO RTC

SHORTED TO MPMU LDOINT FOR PORTABLES

Display Backlight Rails

PPVOUT_LCDBKLT — PPVOUT_LCDBKLT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000
VOLTAGE=48V
PPVOUT_LCDBKLT
PPVOUT_LCDBKLT

PPVIN_LCDBKLT — PPVIN_LCDBKLT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13V
PPVIN_LCDBKLT

PPVOUT_LCDBKLT_D — PPVOUT_LCDBKLT_D
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000
VOLTAGE=48V

KBD Backlight Rails

PPVOUT_KBDBKLT — PPVOUT_KBDBKLT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=48V
PPVOUT_KBDBKLT

SYNC DATE=

PAGE TITLE

POWER ALIASES 3

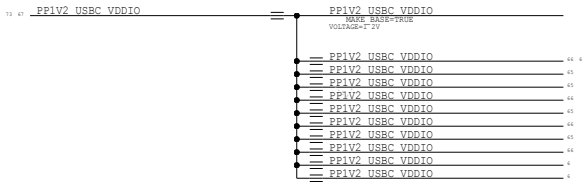
Apple Inc.

DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	402 OF 801
SHEET	103 OF 121

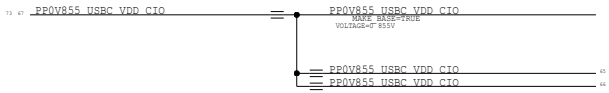
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO THE FOLLOWING
1. OMAN ANY THIS DOCUMENT CONFIDENCE
2. NO REPRODUCE OR COPY
3. NO REVEAL PUBLISH IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

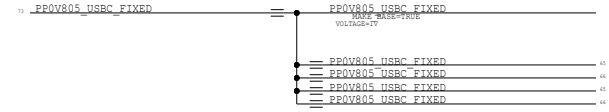
USB 1V2 VDDIO



USB 0V855 CIO



USB 0V805 Fixed



PAGE TITLE

POWER ALIASES 4

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 403 OF 801

SHEET 104 OF 121

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING: (I) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE, (II) NOT TO REPRODUCE OR COPY, (III) NOT TO RELEASE, PUBLISH, IN WHOLE OR PART, (IV) ALL RIGHTS RESERVED.

www.repairlap.com

A Secure Disable Aliases

ND_1V8		ND_1V8
		ND_1V8
MGL_1V8		MGL_1V8
		MGL_1V8
AMR_1V8		AMR_1V8
		AMR_1V8
		AMR_1V8
NC_IPD_LID_OPEN_1V8		NC_IPD_LID_OPEN_1V8
DMIC_DISABLE_L		DMIC_DISABLE_L
LID_CLOSED_DMIC_WARN_L		LID_CLOSED_DMIC_WARN_L
LID_CLOSED_DMIC_WARN_L		
IPD_LID_CLOSED_L		IPD_LID_CLOSED_L
IPD_LID_CLOSED_L		
DMIC_WARN_L		DMIC_WARN_L
DMIC_WARN_L		

B Speaker Amplifier Aliases

TDM_SPKRAMP_L_D2R		TDM_SPKRAMP_L_D2R
		TDM_SPKRAMP_L_D2R
		TDM_SPKRAMP_L_D2R
TDM_SPKRAMP_R_D2R		TDM_SPKRAMP_R_D2R
		TDM_SPKRAMP_R_D2R
		TDM_SPKRAMP_R_D2R

C PMU Aliases

SWD_NUB_SWCLK_SPMU		SWD_NUB_SWCLK_SPMU
SWD_NUB_SWDIO_SPMU		SWD_NUB_SWDIO_SPMU
SWD_NUB_SWCLK_MPMU		SWD_NUB_SWCLK_MPMU
SWD_NUB_SWDIO_MPMU		SWD_NUB_SWDIO_MPMU
PMU_SYS_ALIVE		PMU_SYS_ALIVE

D Charger Aliases

P5VS2_PGOOD		P5VS2_PGOOD
NC_CHGR_CBC_ON		NC_CHGR_CBC_ON
NC_CHGR_EN_VR1		NC_CHGR_EN_VR1
NC_CHGR_SMC_RST_L		NC_CHGR_SMC_RST_L

E PP5V_S2 Aliases

P5VS2_PWR_EN		P5VS2_PWR_EN
P5VS2_PWR_EN		
P5VS2_EN		P5VS2_EN

F Display and Backlight Aliases

EDP_PANEL_DISCHARGE		EDP_PANEL_DISCHARGE
PMU_ACTIVE_READY		PMU_ACTIVE_READY
NC_BKLT_ISET_KEYB		NC_BKLT_ISET_KEYB
NC_BKLT_KEYB1		NC_BKLT_KEYB1
NC_BKLT_KEYB2		NC_BKLT_KEYB2
NC_KEYBDBKLT_SW2		NC_KEYBDBKLT_SW2
NC_VOUT_KEYBDLED_FB2		NC_VOUT_KEYBDLED_FB2
UNUSED_LP8548_PWM		UNUSED_LP8548_PWM
EDP_PANEL_PWR_EN		EDP_PANEL_PWR_EN
NC_LCDBKLT_FET_DRV		NC_LCDBKLT_FET_DRV

G Secure Element Aliases

NC_SE_GPIO0		NC_SE_GPIO0
TP_SE_GPIO1		TP_SE_GPIO1
NC_I2C_SE_A_SCL		NC_I2C_SE_A_SCL
NC_I2C_SE_A_SDA		NC_I2C_SE_A_SDA
NC_I2C_SE_B_SCL		NC_I2C_SE_B_SCL
NC_I2C_SE_B_SDA		NC_I2C_SE_B_SDA
TP_SYS_GPIO0		TP_SYS_GPIO0
NC_SYS_GPIO1		NC_SYS_GPIO1
NC_SYS_GPIO2		NC_SYS_GPIO2
NC_I2C_SYS_SCL		NC_I2C_SYS_SCL
NC_I2C_SYS_SDA		NC_I2C_SYS_SDA
NC_SYS_GPIO3		NC_SYS_GPIO3

H NAND Aliases

NC_NAND0_S5E0_VPP		NC_NAND0_S5E0_VPP
NC_NAND0_S5E1_VPP		NC_NAND0_S5E1_VPP
SWD_NAND0_SWCLK_R		SWD_NAND0_SWCLK_R

I Wireless Module Aliases

NC_RF_BT_DED		NC_RF_BT_DED

J Audio Aliases

NC_SPKRAMP_C_VSENSEN		NC_SPKRAMP_C_VSENSEN
NC_SPKRAMP_C_VSENSEP		NC_SPKRAMP_C_VSENSEP
NC_SPKRAMP_F_VSENSEN		NC_SPKRAMP_F_VSENSEN
NC_SPKRAMP_F_VSENSEP		NC_SPKRAMP_F_VSENSEP

10/25/2022

PAGE TITLE: Signal Aliases 1

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: THIS DOCUMENT CONFIDENTIAL. NO REPRODUCE OR COPY. NO TRANSFER ALL RIGHTS RESERVED

DRAWING NUMBER	051-09343
SIZE	D
REVISION	5.0.0
BRANCH	dvt-1
PAGE	405 OF 801
SHEET	105 OF 121

www.repairlap.com

A USB-C Aliases: USB 2.0 I/F

USB2_ATC0_LS_P — MAKE_BASE=TRUE — USB2_ATC0_LS_P
USB2_ATC0_LS_N — AKE_BASE=TRUE — USB2_ATC0_LS_N
USB2_ATC1_LS_P — M KE_B SE= RUE — USB2_ATC1_LS_P
USB2_ATC1_LS_N — MAKE_B SE=T UE — USB2_ATC1_LS_N
USB2_ATC0_DBG_LS_P — MAKE_BASE TRUE — USB2_ATC0_DBG_LS_P — USB2_ATC0_DBG_LS_P
USB2_ATC0_DBG_LS_N — MAKE_BASE=TRUE — USB2_ATC0_DBG_LS_N — USB2_ATC0_DBG_LS_N
USB2_ATC1_DBG_LS_P — MAKE_BASE=TRUE — USB2_ATC1_DBG_LS_P — USB2_ATC1_DBG_LS_P
USB2_ATC1_DBG_LS_N — MAKE_BASE=TRUE — USB2_ATC1_DBG_LS_N — USB2_ATC1_DBG_LS_N

B USB-C Aliases: CIO Debug I/F

CIO_ATC0_LSRX — MAKE_BASE=TRUE — CIO_ATC0_LSRX
CIO_ATC0_LSTX — MAKE_BASE=TRUE — CIO_ATC0_LSTX
CIO_ATC1_LSRX — MAKE_BASE=TRUE — CIO_ATC1_LSRX
CIO_ATC1_LSTX — MA E_BASE=TRUE — CIO_ATC1_LSTX

C USB-C Aliases: EUSB I/F

EUSB_ATC0_P — MA E_BASE=TRUE — EUSB_ATC0_P
EUSB_ATC0_N — MAKE_BASE=TRUE — EUSB_ATC0_N
EUSB_ATC1_P — MAKE_B SE= RUE — EUSB_ATC1_P
EUSB_ATC1_N — MAKE_BASE= UE — EUSB_ATC1_N
EUSB_DBG_P — MAKE_BASE=TRUE — EUSB_DBG_P
EUSB_DBG_P
EUSB_DBG_N — MAKE_BASE=TRUE — EUSB_DBG_N
EUSB_DBG_N
ATCRTMR0_RESET_L — MAKE_ ASE TR — ATCRTMR0_RESET_L

D USB-C Aliases: I2C I/F

I2C_UPC0_ATCRTMR0_SDA — AKE_BASE=TRUE — I2C_UPC0_ATCRTMR0_SDA — BI
I2C_UPC0_ATCRTMR0_SDA
I2C_UPC0_ATCRTMR0_SCL — MAKE_BASE=TRUE — I2C_UPC0_ATCRTMR0_SCL — BI
I2C_UPC0_ATCRTMR0_SCL
I2C_UPC1_ATCRTMR1_SDA — MAKE_BASE=TRUE — I2C_UPC1_ATCRTMR1_SDA — BI
I2C_UPC1_ATCRTMR1_SDA
I2C_UPC1_ATCRTMR1_SCL — MAKE_BASE=TRUE — I2C_UPC1_ATCRTMR1_SCL — BI
I2C_UPC1_ATCRTMR1_SCL

E USB-C Aliases: SWD I/F

SWD_NUB_ATCRTMR_SWCLK — MAKE_BASE=TRUE — SWD_NUB_ATCRTMR_SWCLK
SWD_NUB_ATCRTMR_SWCLK
SWD_NUB_ATCRTMR_SWDIO — MAKE_BASE=TRUE — SWD_NUB_ATCRTMR_SWDIO
SWD_NUB_ATCRTMR_SWDIO

F USB-C Aliases: VDD I/O Fuse I/F

GND — MA E_BASE=TRUE — GND
GND — MAK _BAS =TRUE — GND

G USB-C Aliases: SOC Dock Connect

SOC_DOCK_CONNECT — MAK _BAS =TRUE — SOC_DOCK_CONNECT

H USB-C Aliases: UPC I2C

I2C_UPC01_3V3_SDA — MAK _BA E=TRUE — I2C_UPC01_3V3_SDA
I2C_UPC01_3V3_SDA
I2C_UPC01_3V3_SCL — MAKE_BASE=T UE — I2C_UPC01_3V3_SCL
I2C_UPC01_3V3_SCL

I USB-C Aliases: UPC SPMI

SPMI_NUB_UPC0_CLK — AKE_BASE=TRUE — SPMI_NUB_UPC0_CLK
SPMI_NUB_UPC0_DATA — MA E_BASE=TRUE — SPMI_NUB_UPC0_DATA
SPMI_NUB_UPC1_CLK — MAK _BASE=TRUE — SPMI_NUB_UPC1_CLK
SPMI_NUB_UPC1_DATA — MAKE_BASE=TRUE — SPMI_NUB_UPC1_DATA
SPMI_NUB_UPC5_CLK — MAKE_BASE=TRUE — SPMI_NUB_UPC5_CLK
SPMI_NUB_UPC5_DATA — MAKE_BASE=TRUE — SPMI_NUB_UPC5_DATA
SPMI_NUB_UPC015_CLK_R — MAKE_BASE=TRUE — SPMI_NUB_UPC015_CLK_R
SPMI_NUB_UPC015_DATA_R — N E_BASE=TRUE — SPMI_NUB_UPC015_DATA_R
NC_UPC_SMC_I2C_INT_L — NO_TEST=1 M ST_BASE=TRUE — NC_UPC_SMC_I2C_INT_L

J USB-C Aliases: PMU UPC FORCE DFU

PMU_UPC_FORCE_DFU — MAKE_BAS =TR — PMU_UPC_FORCE_DFU
UPC0_SOC_DFU_BOOTED_L — MAKE_BASE=TRUE — UPC0_SOC_DFU_BOOTED_L
UPC0_SOC_DFU_BOOTED_L
SOC_FORCE_DFU — MA E_BASE=TRUE — SOC_FORCE_DFU

K USB-C Aliases: UPC SWD

SWD_UPC0_CLK — M KE_B SE= RUE — SWD_UPC0_CLK
SWD_UPC0_DATA — MAKE_B SE=TRUE — SWD_UPC0_DATA
SWD_UPC1_CLK — MAKE_BASE=TRUE — SWD_UPC1_CLK
SWD_UPC1_DATA — MAKE_BASE=TRUE — SWD_UPC1_DATA
SWD_UPC5_CLK — MAKE_BASE=TRUE — SWD_UPC5_CLK
SWD_UPC5_DATA — MAKE_BASE=TRUE — SWD_UPC5_DATA

L USB-C Aliases: UPC PWR Too Low

INPUT_PWR_2LOW_L — AKE_BASE=TRUE — INPUT_PWR_2LOW_L
INPUT_PWR_2LOW_L
INPUT_PWR_2LOW_L

M USB-C Aliases: Unused Mogul

NC_UPC0_AID0 — MAKE_BASE=TRUE NO_TEST=1 — NC_UPC0_AID0

N USB-C Aliases: Unused I2C0 to UPCs

NC_I2C_UPC_SCL — MAKE_BASE=TRUE — NC_I2C_UPC_SCL
NC_I2C_UPC_SDA — MAKE_BASE=TRUE — NC_I2C_UPC_SDA
NC_UPC_I2C_INT_L — MAKE_BASE=TRUE — NC_UPC_I2C_INT_L

10/27/2022

PAGE TITLE: Signal Aliases 2

Apple Inc.

DRAWING NUMBER: 051-09343 SIZE: D

REVISION: 5.0.0

BRANCH: dvt-1

PAGE: 406 OF 801

SHEET: 106 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: THIS DOCUMENT CONFIDENCE. NO REPRODUCE OR COPY IN WHOLE OR PART. ALL RIGHTS RESERVED

www.repairlap.com

A GPIO AOP ALIAS

NC_SOC_AOP_I2CM1_SCL	=	NC_SOC_AOP_I2CM1_SCL (MAKE_BASE=TRUE)
NC_SOC_AOP_I2CM1_SDA	=	NC_SOC_AOP_I2CM1_SDA (MAKE_BASE=TRUE)
NC_SOC_AOP_I2CM2_SCL	=	NC_SOC_AOP_I2CM2_SCL (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AOP_I2CM2_SDA	=	NC_SOC_AOP_I2CM2_SDA (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_NUB_SPMI2_SCLK	=	NC_SOC_NUB_SPMI2_SCLK (MAKE_BASE=TRUE)
NC_SOC_NUB_SPMI2_SDATA	=	NC_SOC_NUB_SPMI2_SDATA (MAKE_BASE=TRUE)
NC_SOC_AOP_UART0_RXD	=	NC_SOC_AOP_UART0_RXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AOP_UART0_TXD	=	NC_SOC_AOP_UART0_TXD (MAKE_BASE=TRUE)
NC_SOC_AOP_UART1_RXD	=	NC_SOC_AOP_UART1_RXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AOP_UART1_TXD	=	NC_SOC_AOP_UART1_TXD (MAKE_BASE=TRUE)
NC_SOC_AOP_UART2_RXD	=	NC_SOC_AOP_UART2_RXD (MAKE_BASE=TRUE)
NC_SOC_AOP_UART2_TXD	=	NC_SOC_AOP_UART2_TXD (MAKE_BASE=TRUE)
NC_PDM_DMIC_DATA2	=	NC_PDM_DMIC_DATA2 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_SGPIO1	=	NC_SOC_SGPIO1 (MAKE_BASE=TRUE, NO_TEST=1)
P3V8AON_ILIMIT_DIV_PULL_PWM	=	P3V8AON_ILIMIT_DIV_PULL_PWM (MAKE_BASE=TRUE)
NC_SOC_AOP_GPIO_15	=	NC_SOC_AOP_GPIO_15 (MAKE_BASE=TRUE, NO_TEST=1)
NC_HDMI_CEC_AOP_TX	=	NC_HDMI_CEC_AOP_TX (MAKE_BASE=TRUE)
NC_HDMI_CEC_AOP_RX	=	NC_HDMI_CEC_AOP_RX (MAKE_BASE=TRUE, NO_TEST=1)
NC_HDMI_HDP_AOP	=	NC_HDMI_HDP_AOP (MAKE_BASE=TRUE)
TP_SOC_DOCK_ATTENTION	NC =	TP_SOC_DOCK_ATTENTION (MAKE_BASE=TRUE)

B GPIO AP ALIAS

NC_SOC_AP_GPIO_2	=	NC_SOC_AP_GPIO_2 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_3	=	NC_SOC_AP_GPIO_3 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_22	=	NC_SOC_AP_GPIO_22 (MAKE_BASE=TRUE)
NC_BKLT_PWR_ON	=	NC_BKLT_PWR_ON (MAKE_BASE=TRUE)
NC_SOC_AP_GPIO_1	=	NC_SOC_AP_GPIO_1 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SWD_UPC_SWDIO1_R	=	NC_SWD_UPC_SWDIO1_R (MAKE_BASE=TRUE, NO_TEST=1)
NC_CCG_I2C_INT	=	NC_CCG_I2C_INT (MAKE_BASE=TRUE)
NC_SD_PRSNT_L_DMIC_ID	=	NC_SD_PRSNT_L_DMIC_ID (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_17	=	NC_SOC_AP_GPIO_17 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_18	=	NC_SOC_AP_GPIO_18 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_19	=	NC_SOC_AP_GPIO_19 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_20	=	NC_SOC_AP_GPIO_20 (MAKE_BASE=TRUE)
NC_SOC_AP_GPIO_23	=	NC_SOC_AP_GPIO_23 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_24	=	NC_SOC_AP_GPIO_24 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_25	=	NC_SOC_AP_GPIO_25 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_GPIO_26	=	NC_SOC_AP_GPIO_26 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART1_CTS_L	=	NC_SOC_AP_UART1_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART1_RTS_L	=	NC_SOC_AP_UART1_RTS_L (MAKE_BASE=TRUE)
NC_SOC_AP_UART1_RXD	=	NC_SOC_AP_UART1_RXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART1_TXD	=	NC_SOC_AP_UART1_TXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART2_CTS_L	=	NC_SOC_AP_UART2_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART2_RTS_L	=	NC_SOC_AP_UART2_RTS_L (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART2_RXD	=	NC_SOC_AP_UART2_RXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART2_TXD	=	NC_SOC_AP_UART2_TXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART3_CTS_L	=	NC_SOC_AP_UART3_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART3_RTS_L	=	NC_SOC_AP_UART3_RTS_L (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART3_RXD	=	NC_SOC_AP_UART3_RXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART3_TXD	=	NC_SOC_AP_UART3_TXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_SOC_AP_UART4_RXD	=	NC_SOC_AP_UART4_RXD (MAKE_BASE=TRUE)
NC_SOC_AP_UART4_TXD	=	NC_SOC_AP_UART4_TXD (MAKE_BASE=TRUE, NO_TEST=1)
NC_UART_TCON_R2D	=	NC_UART_TCON_R2D (MAKE_BASE=TRUE, NO_TEST=1)
NC_UART_HDMI_D2R	=	NC_UART_HDMI_D2R (MAKE_BASE=TRUE, NO_TEST=1)
NC_UART_HDMI_R2D	=	NC_UART_HDMI_R2D (MAKE_BASE=TRUE, NO_TEST=1)

C DEBUG ALIAS

NC_SOC_SWD_TMS5	=	NC_SOC_SWD_TMS5 (MAKE_BASE=TRUE, NO_TEST=1)

D GND ALIAS

The DUT_GND_DETECT signal is for dev only,
and should be tied to GND.

GND (MAKE_BASE=TRUE) = GND — IN

SYNC MASTER= SYNC DATE=

PAGE TITLE

SOC: ALIASES GPIO

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 420 OF 801

SHEET 107 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. EXCEPT WHERE OTHERWISE AGREED BY APPLE IN WRITING THE FOLLOWING INFORMATION IS DOCUMENT CONFIDENTIAL. NO REPRODUCTION OR COPY IN WHOLE OR PART ALL RIGHTS RESERVED

www.repairlap.com

A SPI & I2S ALIAS

NC_TDM_SPKRAMP_TOP_BCLK_R	NC_TDM_SPKRAMP_TOP_BCLK_R	MAKE_BASE=TRUE NO_TEST=1
NC_TDM_SPKRAMP_TOP_D2R	NC_TDM_SPKRAMP_TOP_D2R	MAKE_BASE=TRUE
NC_TDM_SPKRAMP_TOP_R2D_R	NC_TDM_SPKRAMP_TOP_R2D_R	MAKE_BASE=TRUE NO_TEST=1
NC_TDM_SPKRAMP_TOP_FSYNC_R	NC_TDM_SPKRAMP_TOP_FSYNC_R	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_AP_SPI5_MISO	NC_SOC_AP_SPI5_MISO	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_AP_SPI5_MOSI	NC_SOC_AP_SPI5_MOSI	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_AP_SPI5_SCLK	NC_SOC_AP_SPI5_SCLK	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_AP_SPI5_CS_L	NC_SOC_AP_SPI5_CS_L	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_SSPI0_MISO	NC_SOC_SSPI0_MISO	MAKE_BASE=TRUE
NC_SOC_SSPI0_MOSI	NC_SOC_SSPI0_MOSI	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_SSPI0_SCLK	NC_SOC_SSPI0_SCLK	MAKE_BASE=TRUE
NC_SOC_AP_SPI2_CS_L	NC_SOC_AP_SPI2_CS_L	MAKE_BASE=TRUE
NC_SPI_DP2HDMI_HOLD_L	NC_SPI_DP2HDMI_HOLD_L	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_AP_I2S0_MCK	NC_SOC_AP_I2S0_MCK	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_AP_I2S1_MCK	NC_SOC_AP_I2S1_MCK	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_AP_I2S2_MCK	NC_SOC_AP_I2S2_MCK	MAKE_BASE=TRUE
NC_AOP_I2S0_MCK	NC_AOP_I2S0_MCK	MAKE_BASE=TRUE NO_TEST=1
NC_AOP_I2S0_LRCLK	NC_AOP_I2S0_LRCLK	MAKE_BASE=TRUE
NC_AOP_I2S0_BCLK	NC_AOP_I2S0_BCLK	MAKE_BASE=TRUE
NC_AOP_I2S0_DIN	NC_AOP_I2S0_DIN	MAKE_BASE=TRUE NO_TEST=1
NC_AOP_I2S0_DOUT	NC_AOP_I2S0_DOUT	MAKE_BASE=TRUE NO_TEST=1
NC_PDM_DMIC_CLK7_R	NC_PDM_DMIC_CLK7_R	MAKE_BASE=TRUE
NC_SOC_SPI3_MOSI	NC_SOC_SPI3_MOSI	MAKE_BASE=TRUE
NC_SOC_SPI3_MISO	NC_SOC_SPI3_MISO	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_SPI3_SCLK	NC_SOC_SPI3_SCLK	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_SPI3_SSIN	NC_SOC_SPI3_SSIN	MAKE_BASE=TRUE NO_TEST=1

B GPIO MTP ALIAS

NC_SOC_MTP_I2C0_SCL	NC_SOC_MTP_I2C0_SCL	MAKE_BASE=TRUE
NC_SOC_MTP_I2C0_SDA	NC_SOC_MTP_I2C0_SDA	MAKE_BASE=TRUE
NC_SOC_MTP_FUNC_6	NC_SOC_MTP_FUNC_6	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MTP_FUNC_7	NC_SOC_MTP_FUNC_7	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MTP_FUNC_1	NC_SOC_MTP_FUNC_1	MAKE_BASE=TRUE
NC_SOC_MTP_FUNC_2	NC_SOC_MTP_FUNC_2	MAKE_BASE=TRUE

SYNC MASTER= SYNC DATE=

PAGE TITLE

SOC: ALIASES SPI, I2S

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 421 OF 801

SHEET 108 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: (I) TO MAINTAIN IN CONFIDENCE THIS DOCUMENT, (II) NOT TO REPRODUCE OR COPY IT, (III) NOT TO RELEASE OR PUBLISH IT IN WHOLE OR PART. (IV) ALL RIGHTS RESERVED.

www.repairlap.com

Ⓐ LPDP ALIAS

NC_SOC_LPDP_RX_AUX_D0	NC_SOC_LPDP_RX_AUX_D0	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D1	NC_SOC_LPDP_RX_AUX_D1	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_AUX_D2	NC_SOC_LPDP_RX_AUX_D2	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_AUX_D3	NC_SOC_LPDP_RX_AUX_D3	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_AUX_D4	NC_SOC_LPDP_RX_AUX_D4	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_AUX_D5	NC_SOC_LPDP_RX_AUX_D5	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_AUX_D6	NC_SOC_LPDP_RX_AUX_D6	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_AUX_D7	NC_SOC_LPDP_RX_AUX_D7	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_D1P	NC_SOC_LPDP_RX_D1P	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_D1N	NC_SOC_LPDP_RX_D1N	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_D2P	NC_SOC_LPDP_RX_D2P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D2N	NC_SOC_LPDP_RX_D2N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D3P	NC_SOC_LPDP_RX_D3P	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_D3N	NC_SOC_LPDP_RX_D3N	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_D4P	NC_SOC_LPDP_RX_D4P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D4N	NC_SOC_LPDP_RX_D4N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D5P	NC_SOC_LPDP_RX_D5P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D5N	NC_SOC_LPDP_RX_D5N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D6P	NC_SOC_LPDP_RX_D6P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D6N	NC_SOC_LPDP_RX_D6N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D7P	NC_SOC_LPDP_RX_D7P	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX_D7N	NC_SOC_LPDP_RX_D7N	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX1_RCAL_POS	NC_SOC_LPDP_RX1_RCAL_POS	MAKE_BASE=TRUE, NO_TEST=1
NC_SOC_LPDP_RX1_RCAL_NEG	NC_SOC_LPDP_RX1_RCAL_NEG	MAKE_BASE=TRUE, NO_TEST=1
NC_LPDP_EXT_DATA_CP<0>	NC_LPDP_EXT_DATA_CP<0>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<0>	NC_LPDP_EXT_DATA_CN<0>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<1>	NC_LPDP_EXT_DATA_CP<1>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<1>	NC_LPDP_EXT_DATA_CN<1>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<2>	NC_LPDP_EXT_DATA_CP<2>	MAKE_BASE=TRUE, NO_TEST=1
NC_LPDP_EXT_DATA_CN<2>	NC_LPDP_EXT_DATA_CN<2>	MAKE_BASE=TRUE, NO_TEST=1
NC_LPDP_EXT_DATA_CP<3>	NC_LPDP_EXT_DATA_CP<3>	MAKE_BASE=TRUE, NO_TEST=1
NC_LPDP_EXT_DATA_CN<3>	NC_LPDP_EXT_DATA_CN<3>	MAKE_BASE=TRUE, NO_TEST=1
NC_LPDP_EXT_AUX_CP	NC_LPDP_EXT_AUX_CP	MAKE_BASE=TRUE
NC_LPDP_EXT_AUX_CN	NC_LPDP_EXT_AUX_CN	MAKE_BASE=TRUE
NC_LPDP_EXT_HPD	NC_LPDP_EXT_HPD	MAKE_BASE=TRUE, NO_TEST=1

SYNC MASTER= SYNC DATE=

PAGE TITLE

SOC: ALIASES LPDP RX

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 423 OF 801

SHEET 109 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. EXCEPT WHERE OTHERWISE AGREED BY THE PARTIES THE FOLLOWING INFORMATION IS DOCUMENTED CONFIDENCE
NOT TO BE REPRODUCED OR COPIED
NOR TO BE REVEALED OR PUBLISHED IN WHOLE OR PART
ALL RIGHTS RESERVED

www.repairlap.com

A PCIe ALIAS

13	NC_SOC_GP_PCIE_RX1P	NC_SOC_GP_PCIE_RX1P	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_RX1N	NC_SOC_GP_PCIE_RX1N	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_TX1P	NC_SOC_GP_PCIE_TX1P	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_TX1N	NC_SOC_GP_PCIE_TX1N	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_CLK1_100MP	NC_SOC_GP_PCIE_CLK1_100MP	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_CLK1_100MN	NC_SOC_GP_PCIE_CLK1_100MN	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_CLKREQ_1_L	NC_SOC_GP_PCIE_CLKREQ_1_L	MAKE_BASE=TRUE
13	NC_SOC_GP_PCIE_PERST_1_L	NC_SOC_GP_PCIE_PERST_1_L	MAKE_BASE=TRUE
3	NC_SOC_GP_PCIE_RX2P	NC_SOC_GP_PCIE_RX2P	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_RX2N	NC_SOC_GP_PCIE_RX2N	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_TX2P	NC_SOC_GP_PCIE_TX2P	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_TX2N	NC_SOC_GP_PCIE_TX2N	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_CLK2_100MP	NC_SOC_GP_PCIE_CLK2_100MP	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_CLK2_100MN	NC_SOC_GP_PCIE_CLK2_100MN	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_CLKREQ_2_L	NC_SOC_GP_PCIE_CLKREQ_2_L	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_PERST_2_L	NC_SOC_GP_PCIE_PERST_2_L	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_RX3P	NC_SOC_GP_PCIE_RX3P	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_RX3N	NC_SOC_GP_PCIE_RX3N	MAKE_BASE=TRUE NO_TEST=1
1	NC_SOC_GP_PCIE_TX3P	NC_SOC_GP_PCIE_TX3P	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_TX3N	NC_SOC_GP_PCIE_TX3N	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_CLK3_100MP	NC_SOC_GP_PCIE_CLK3_100MP	MAKE_BASE=TRUE NO_TEST=1
13	NC_SOC_GP_PCIE_CLK3_100MN	NC_SOC_GP_PCIE_CLK3_100MN	MAKE_BASE=TRUE NO_TEST=1
9	NC_SOC_GP_PCIE_CLKREQ_3_L	NC_SOC_GP_PCIE_CLKREQ_3_L	MAKE_BASE=TRUE NO_TEST=1
1	NC_SOC_GP_PCIE_PERST_3_L	NC_SOC_GP_PCIE_PERST_3_L	MAKE_BASE=TRUE NO_TEST=1

B DISP ALIAS

9	NC_I2C_SD_DISP_BKLT_SCL	NC_I2C_SD_DISP_BKLT_SCL	MAKE_BASE=TRUE
9	NC_I2C_SD_DISP_BKLT_SDA	NC_I2C_SD_DISP_BKLT_SDA	MAKE_BASE=TRUE NO_TEST=1
11	I2C_DISP_BKLT_SCL	I2C_DISP_BKLT_SCL	MAKE_BASE=TRUE 55
11	I2C_DISP_BKLT_SDA	I2C_DISP_BKLT_SDA	MAKE_BASE=TRUE 55
11	NC_SPI_DISP_BKLT_CLK_R	NC_SPI_DISP_BKLT_CLK_R	MAKE_BASE=TRUE NO_TEST=1
11	NC_SPI_DISP_BKLT_CS_L	NC_SPI_DISP_BKLT_CS_L	MAKE_BASE=TRUE NO_TEST=1
11	NC_SPMI_DISP_BKLT_CLK	NC_SPMI_DISP_BKLT_CLK	MAKE_BASE=TRUE NO_TEST=1
11	NC_SPMI_DISP_BKLT_DATA	NC_SPMI_DISP_BKLT_DATA	MAKE_BASE=TRUE
11	NC_SOC_DISP_POL	NC_SOC_DISP_POL	MAKE_BASE=TRUE NO_TEST=1
11	NC_DISP_BKLT_FSYNC	NC_DISP_BKLT_FSYNC	MAKE_BASE=TRUE
81	DISP_BKLT_LSYNC	DISP_BKLT_LSYNC 11	MAKE_BASE=TRUE
11	NC_SOC_DISP_TOUCH_BSYNC0	NC_SOC_DISP_TOUCH_BSYNC0	MAKE_BASE=TRUE
11	NC_SOC_DISP_TOUCH_BSYNC1	NC_SOC_DISP_TOUCH_BSYNC1	MAKE_BASE=TRUE
11	NC_SOC_DISP_TOUCH_EB	NC_SOC_DISP_TOUCH_EB	MAKE_BASE=TRUE
11	NC_BKLT_BOOST_THROTTLE_L	NC_BKLT_BOOST_THROTTLE_L	MAKE_BASE=TRUE NO_TEST=1

D LPDP Aliases

11	NC_SOC_LPDP_DP2HDMI_RCAL_POS	NC_SOC_LPDP_DP2HDMI_RCAL_POS	MAKE_BASE=TRUE NO_TEST=1
11	NC_SOC_LPDP_DP2HDMI_RCAL_NEG	NC_SOC_LPDP_DP2HDMI_RCAL_NEG	MAKE_BASE=TRUE

SYNC MASTER= SYNC DATE=

PAGE TITLE

SOC: ALIASES PCIE, LPDP TX

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT AS OTHERWISE AGREED TO IN THE FOLLOWING WRITING, THIS DOCUMENT IS CONFIDENTIAL. NO REPRODUCTION OR COPY IN WHOLE OR PART IS ALLOWED. ALL RIGHTS RESERVED.

DRAWING NUMBER 051-09343 SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 424 OF 801
SHEET 110 OF 121

www.repairlap.com

A SMC & NUB ALIAS

TOUCHID_PWR_EN	TOUCHID_PWR_EN	MAKE_BASE=TRUE
NC_SOC_NUB_GPIO_2	NC_SOC_NUB_GPIO_2	MAKE_BASE=TRUE
NC_SOC_NUB_GPIO_3	NC_SOC_NUB_GPIO_3	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_NUB_GPIO_4	NC_SOC_NUB_GPIO_4	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_NUB_GPIO_5	NC_SOC_NUB_GPIO_5	MAKE_BASE=TRUE NO_TEST=1
NC_ENET_LOW_PWR	NC_ENET_LOW_PWR	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_NUB_GPIO_10	NC_SOC_NUB_GPIO_10	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_NUB_GPIO_12	NC_SOC_NUB_GPIO_12	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_NUB_GPIO_14	NC_SOC_NUB_GPIO_14	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_NUB_GPIO_15	NC_SOC_NUB_GPIO_15	MAKE_BASE=TRUE NO_TEST=1

D MTR_TD Aliases

NC_SOC_MTR_TD_B	NC_SOC_MTR_TD_B	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MTR_TD_BS	NC_SOC_MTR_TD_BS	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MTR_TD_E	NC_SOC_MTR_TD_E	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MTR_TD_ES	NC_SOC_MTR_TD_ES	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MTR_TD_ESD	NC_SOC_MTR_TD_ESD	MAKE_BASE=TRUE NO_TEST=1

B ISP ALIAS

NC_SOC_ISP_GPIO_1	NC_SOC_ISP_GPIO_1	MAKE_BASE=TRUE
NC_SOC_ISP_GPIO_2	NC_SOC_ISP_GPIO_2	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_ISP_GPIO_3	NC_SOC_ISP_GPIO_3	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_ISP_SPMI0_SCLK	NC_SOC_ISP_SPMI0_SCLK	MAKE_BASE=TRUE
NC_SOC_ISP_SPMI0_SDATA	NC_SOC_ISP_SPMI0_SDATA	MAKE_BASE=TRUE
NC_SOC_ISP_SPMI1_SCLK	NC_SOC_ISP_SPMI1_SCLK	MAKE_BASE=TRUE
NC_SOC_ISP_SPMI1_SDATA	NC_SOC_ISP_SPMI1_SDATA	MAKE_BASE=TRUE
NC_SOC_SENSOR0_CLK	NC_SOC_SENSOR0_CLK	MAKE_BASE=TRUE
NC_SOC_SENSOR1_CLK	NC_SOC_SENSOR1_CLK	MAKE_BASE=TRUE

E MISC. ALIAS

NC_SOC_SMC_GPIO_1	NC_SOC_SMC_GPIO_1	MAKE_BASE=TRUE NO_TEST=1
NC_SMC_FAN_0_PWM	NC_SMC_FAN_0_PWM	MAKE_BASE=TRUE NO_TEST=1
NC_SMC_FAN_0_TACH	NC_SMC_FAN_0_TACH	MAKE_BASE=TRUE NO_TEST=1
NC_SMC_FAN_1_PWM	NC_SMC_FAN_1_PWM	MAKE_BASE=TRUE NO_TEST=1
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_NUB_CLK_OUT_0	NC_SOC_NUB_CLK_OUT_0	MAKE_BASE=TRUE NO_TEST=1
TP_SOC_NUB_CLK_OUT_1	TP_SOC_NUB_CLK_OUT_1	MAKE_BASE=TRUE

C MIPI Aliases

NC_SOC_MIPI0C_DPCLK	NC_SOC_MIPI0C_DPCLK	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MIPI0C_DNCLK	NC_SOC_MIPI0C_DNCLK	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MIPI0C_DPDATA<0>	NC_SOC_MIPI0C_DPDATA<0>	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MIPI0C_DNDATA<0>	NC_SOC_MIPI0C_DNDATA<0>	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MIPI0C_DPDATA<1>	NC_SOC_MIPI0C_DPDATA<1>	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MIPI0C_DNDATA<1>	NC_SOC_MIPI0C_DNDATA<1>	MAKE_BASE=TRUE NO_TEST=1
NC_SOC_MIPI0C_REXT	NC_SOC_MIPI0C_REXT	MAKE_BASE=TRUE NO_TEST=1 CKPLUS_WAIVE=MULTI_PIN_NC_NETS

F UWB Aliases

NC_UWB_HOST_WAKE	NC_UWB_HOST_WAKE	MAKE_BASE=TRUE NO_TEST=1
NC_UWB_DUMP_TRIG	NC_UWB_DUMP_TRIG	MAKE_BASE=TRUE
NC_UWB_CS_L	NC_UWB_CS_L	MAKE_BASE=TRUE
NC_SWD_UWB_SWDIO_R	NC_SWD_UWB_SWDIO_R	MAKE_BASE=TRUE

SYNC MASTER= SYNC DATE=

PAGE TITLE

SOC: ALIASES CAMERA, USB, MISC

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 425 OF 801

SHEET 111 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES AGREES TO THE FOLLOWING: (1) MAINTAIN IS DOCUMENT IN CONFIDENCE (2) NOT REPRODUCE OR COPY (3) NOT RELEASE PUBLISH IN WHOLE OR PART. ALL RIGHTS RESERVED

www.repairlap.com

PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	
CLASS NAME		CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	N
I2C	P	DEFAULT	SMB*SCL*,SMB*SDA*,I2C*SCL*,I2C*SDA*,I2C*INT*	Y
SPI	P	DEFAULT	SPI*MISO*,SPI*MOSI*,SPI*CLK*	Y
SPMI	P	DEFAULT	SPMI*	Y
SWD	P	DEFAULT	SWD_NAND* SWD_NUB*	Y
JTAG	P	DEFAULT	*JTAG*SEL,*JTAG*TCK,*JTAG*TDI,*JTAG*TDO,*JTAG*TMS	Y
CL CK_24M	P	A_45_OHM_SE	SOC_XTAL24M*,SOC_24M_O R,NAND0_CLK24M*	Y
CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
TDM_SPKRAMP	P	DEFAULT	TDM_SPKRAMP_*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
DMIC_PDM	P	A_45_OHM_SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
USBC_SBU	P	A_45_OHM_SE	USBC0_SBU*,USBC1_SBU*	Y
CIO D2R	P	A_85_OHM_DIFF	DP DP USBC* D2R*	Y
CIO R2D	P	A_85_OHM_DIFF	DP DP USBC* R2D*	Y
PCIE_NAND D2R	P	A_85_OHM_DIFF	DP DP_PC E_NAND* D2R*	Y
PCIE_NAND R2D	P	A_85_OHM_DIFF	DP DP_PCIE_NAND* R2D*	Y
PCIE_WLBT D2R	P	A_85_OHM_DIFF	DP DP_PCIE_WLBT* R2D*	Y
PCIE_WLBT R2D	P	A_85_OHM_DIFF	DP DP_PCIE_WLBT* D2R*	Y
LPDP	P	A_85_OHM_DIFF	DP DP_LPDP_INT_DATA*	Y
LPDP_FTCAM	P	A_85_OHM_DIFF	DP DP_LPDP_FTCAM_DATA*	Y
PCIE_CLK	P	A_85_OHM_DIFF	DP DP_PCIE_CLK100M*	Y
EUSB	P	A_85_OHM_DIFF	DP DP_EUSB*	Y
USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC*_LS,DP_USB_ATC*_LS,DP_USBC*_USB_BOT,DP_USBC*_USB_TOP	Y
USBC_ATC_AUX	P	A_85_OHM_DIFF	DP:DP_USBC*_AUX*	Y
ISNS TSNS	P	SNS DP	DP:DP_ISNSP,DP_CMOR_CS*,DP_RYVRAON_ISNSP,DP_RYVRAON_ISNSP,DP_RYVRAON_USNSP,DP_TSN NS*	Y
GROUND	P	DEFAULT	GND	Y
OWER	P	POWER	PP*,PN*	Y

PHYSICAL CONSTRAINT SET, NET ASSIGNMENT

	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)

PAGE TITLE

17.4 PHYSICAL CSETS

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 501 OF 801

SHEET 112 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING
I. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II. NOT TO REPRODUCE OR COPY IT
III. NOT TO RELEASE, PUBLISH IT IN WHOLE OR PART
IV. ALL RIGHTS RESERVED

www.repairlap.com

SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	
CLASS NAME		CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	N
CLOCK_24M	S	A_DIELECTRIC_3X	=	Y
CLOCK_32K	S	A_DIELECTRIC_3X	=	Y
CIO_D2R	S	A_DIELECTRIC_5X	=	Y
CIO_R2D	S	A_DIELECTRIC_5X	=	Y
USBC_ATC_AUX	S	A_DIELECTRIC_4X	=	Y
PCIE_NAND_D2R	S	A_DIELECTRIC_4X	=	Y
PCIE_NAND_R2D	S	A_DIELECTRIC_4X	=	Y
PCIE_WLST_D2R	S	A_DIELECTRIC_4X	=	Y
PCIE_WLST_R2D	S	A_DIELECTRIC_4X	=	Y
PCIE_CLK	S	A_DIELECTRIC_5X	=	Y
LPDP	S	A_DIELECTRIC_5X	=	Y
LPDP_FTCAM	S	A_DIELECTRIC_4X	=	Y
EUSB	S	A_DIELECTRIC_4X	=	Y
USB2	S	A_DIELECTR_C_4X	=	Y
GROUND	S	DEFAULT	=	Y
OWER	S	DEFAULT	=	Y
RF	S	RF	RF_ANT*	Y

PAGE TITLE

17.4 SPACING CSETS, ISO

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 502 OF 801

SHEET 113 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OR AGREES TO THE FOLLOWING
I. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II. NOT TO REPRODUCE OR COPY IT
III. NOT TO RELEASE PUBLISH IT IN WHOLE OR PART
IV. ALL RIGHTS RESERVED

www.repairlap.com

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
CIO_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP_FTCAM	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
USBC_ATC_AUX	GROUND	DEFAULT_WITH_4X_TO_SHAPE
EUSB	GROUND	DEFAULT_WITH_4X_TO_SHAPE
USB2	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP	POWER	DEFAULT_WITH_4X_TO_ HAPE
LPDP_FTCAM	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
CIO_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
CIO_D2R	CIO_R2D	A_DIELECTRIC_5X
PCIE_NAND_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_NAND_R2D	A_DIELECTRIC_5X
PCIE_WLBT_D2R	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_WLBT_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
CIO_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_CLK	A_DIELECTRIC_4X
CIO_R2D	LPDP	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_NAND_R2D	LPDP	A_DIELECTRIC_4X
PCIE_WLBT_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_WLBT_R2D	LPDP	A_DIELECTRIC_4X
PCIE_CLK	PCIE_CLK	A_DIELECTRIC_4X
PCIE_CLK	LPDP	A_DIELECTRIC_4X
LPDP	LPDP	A_DIELECTRIC_3X
LPDP_FTCAM	LPDP_FTCAM	A_DIELECTRIC_3X

SYNC MASTER = SYNC DATE

PAGE TITLE

17.4 SPACING CSETS, CLASS-CLASS

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 503 OF 801

SHEET 114 OF 121

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:

(I) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE,

(II) NOT TO REPRODUCE OR COPY IT,

(III) NOT TO RELEASE, PUBLISH IT IN WHOLE OR PART.

(IV) ALL RIGHTS RESERVED.

www.repairlap.com

SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-13035	1	PCBA,MUDUMALAI,X2483	U0600	CRITICAL	SOC:INTERPOSER

C0 GOOD HY

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-30913	1	SOC,IRE C0+8 ,1Y,4C,BIN3,CX,H,M2565	U0600	CRITICAL	SOC GOOD_C0_HY_8GB
998-30914	1	SOC,IRE C0+16G,1Y,4C,BIN3,CX,H,M2565	U0600	CRITICAL	SOC GOOD_C0_HY_16GB
998-30915	1	SOC,IRE C0+24G,1Z,4C,BIN3,CX,H,M2565	U0600	CRITICAL	SOC GOOD_C0_HY_24GB

AR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DE	COMMEN S
998-30907	998-30913	ALT_CMN	ALL	Hynix Bin1
998-30908	998-30914	ALT_CMN	ALL	Hynix Bin1
998-30909	998-30915	ALT_CMN	ALL	Hynix Bin1

PAR NUMBER	AL ER A E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S
998-32805	998-30913	ALT_CMN	ALL	Hynix Bin4
998-32806	998-30914	ALT_CMN	ALL	Hynix Bin4
998-32807	998-30915	ALT_CMN	ALL	Hynix Bin4

C0 GOOD SA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-32030	1	SOC,IRE C0+8G,1A,4C,BIN3,CX,S,M2565	U0600	CRITICAL	SOC GOOD_C0_SS_8GB

NO SAMSUNG 16,24 GB DRAM CONFIGS

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DES	COMMEN S
998-32028	998-32030	ALT_CMN	ALL	Samsung Bin1

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	R F ES	COMMEN S
998-32808	998-32030	ALT_CMN	ALL	Samsung Bin4

C0 GOOD MI

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
NO MICRON 8GB DRAM CONFIG					
998-32534	1	SO ,IR C0+ 8G,1B,4C,BIN3,CX,H,M2565	U0600	CRITICAL	SOC GOOD_C0_MI_16GB
998-30918	1	SOC,IRE C0+2 G,1A,4C,BIN3,CX,H,M2565	U0600	CRITICAL	SOC GOOD_C0_MI_24GB

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DES	COMMEN S
NO MICRON 8GB DRAM CONFIG				
998-30911	998-32534	ALT_CMN	ALL	Micron Bin1
998-30912	998-30918	ALT_CMN	ALL	Micron Bin1

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S
NO MICRON 8GB DRAM CONFIG				
998-32809	998-32534	ALT_CMN	ALL	Micron Bin4
998-32810	998-309 8	ALT_CMN	ALL	Micron Bin4

C0 BEST HY

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-30907	1	SOC,IRE C0+8 ,1Y,4C,BIN1,CX,H,M2565	U0600	CRITICAL	SOC BEST_C0_HY_8GB
998-30908	1	SOC,IRE C0+16G,1Y,4C,BIN1,CX,H,M2565	U0600	CRITICAL	SOC BEST_C0_HY_16GB
998-30909	1	SOC,IRE C0+24G,1Z,4C,BIN1,CX,H,M2565	U0600	CRITICAL	SOC BEST_C0_HY_24GB

C0 BEST SA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-32028	1	SOC,IRE C0+8G,1A,4C,BIN1,CX,S,M2565	U0600	CRITICAL	SOC BEST_C0_SS_8GB

NO SAMSUNG 16,24 GB DRAM CONFIGS

C0 BEST MI

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
NO MICRON 8GB DRAM CONFIG					
998-32531	1	S ,IR C + 8G,1B,4C,BIN1,CX,H,M2565	U0600	CRITICAL	SOC BEST_C0_MI_16GB
998-30912	1	SOC,IRE 0+2 G,1A,4C,BIN1,CX,H,M2565	U0600	CRITICAL	SOC BEST_C0_MI_24GB

SYNC MASTER= SYNC DATE=
PAGE I LE

BOM: SOC

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
RE ISION 5.0.0
BRANCH dvt-1
PAGE 601 OF 801
SHEE 115 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC HE P SE OR AGREES O HE FOLLOWING I O MA N A N IS DOCUMEN N CONF DENCE
III NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR I ALL R GH S RESER ED

www.repairlap.com

NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
NANDCFG KX_256G	NAND_L0_L1 ITLC_256G_KX
NANDCFG WD_256G	NAND_L0_L1 ITLC_256G_WD
NANDCFG KX_512G	NAND_L0_L1 ITLC_512G_KX
NANDCFG WD_512G	NAND_L0_L1 ITLC_512G_WD
NANDCFG KX_1P0T	NAND_L0_L1 ITLC_1P0T_KX
NANDCFG WD_1P0T	NAND_L0_L1 ITLC_1P0T_WD
NANDCFG KX_2P0T	NAND_L0_L1 ITLC_2P0T_KX
NANDCFG WD_2P0T	NAND_L0_L1 ITLC_2P0T_WD
NANDCFG INTERPOSER	NAND_L0_L1 INTERPOSER
NANDCFG NONE	NAND_L0_L1 OFF
NANDCFG S5E_MK2	NAND_L0_L1 S5E_MK2

NAND Landing 0 and Landing 1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-24627	2	IC,NAND,S5E-MK2,13.3x11.0MM,H=1.3,LGA315	UN000,UN100	CRITICAL	NAND_L0_L1 S5E_MK2
939-11766	2	PCBA,MANAS,X2371	UN000,UN100	CRITICAL	NAND_L0_L1 INTERPOSER
335S00551	2	NAND,BC5T,128GB,S5E,11.0,512G,K,ULGA315	UN000,UN100	CRITICAL	NAND_L0_L1 ITLC_256G_KX
335S00619	2	NAND,BC5T,128GB,S5E,11.0,512G,W,ULGA315	UN000,UN100	CRITICAL	NAND_L0_L1 ITLC_256G_WD
335S00552	2	NAND,BC5T,256GB,S5E,XX.X,512G,K, LGA315	UN000,UN100	CRITICAL	NAND_L0_L1 ITLC_512G_KX
335S00620	2	NAN BC5T,256GB,S5E,XX.X,512G,W,ULGA3 5	UN000,UN100	CRITICAL	NAND_L0_L1 ITLC_512G_WD
335S00553	2	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100	CRITICAL	NAND_L0_L1 ITLC_1P0T_KX
335S00550	2	NAND,BC5T,512GB,S5E,XX.X,512G,W,ULGA315	UN000,UN100	CRITICAL	NAND_L0_L1 ITLC_1P0T_WD
335S00643	2	NAND,BC5T,1TB,S5E,XX.X,512G,K,MLGA315	UN000,UN100	CRITICAL	NAND_L0_L1 ITLC_2P0T_KX
335S00567	2	NAND BC5ST,1024GB,S5E,XX.X,512G,W,LGA315	UN000,UN100	CRITICAL	NAND_L0_L1 ITLC_2P0T_WD

SYNC MASTER= SYNC DATE=
PAGE I LE

BOM: NAND

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
RE ISION 5.0.0
BRANCH dvt-1
PAGE 602 OF 801
SHEE 116 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC HE P SE OR AGREES O HE FOLLOWING I O MA N A N IS DOCUMEN N CONF DENCE
II NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR
I ALL R GH S RESER ED

www.repairlap.com

A Module Parts

RT13 Retimer

PAR #	Q	DESCR P ION	REFERENC DESIGNA OR(S)	CRI ICAL	BOM OP ION
998-25504	2	C,LIFUKA,B0,USB-C R TIME ,DEV CSP154	UF000,UF100	CRITICAL	ATCRTMR B0
998-27476	2	C,LIFUKA,B1,USB-C RETIMER EV,CSP154	UF000,UF100	CRITICAL	ATCRTMR B1_DEV
338S00888	2	C,LIFUKA,B1,USB-C RETIMER,ATX,C P154	UF000,UF 00	CRITICAL	ATCRTMR B1_ATX_PROD
338S00889	2	C,LIFUKA,B1,USB-C RETIMER,SCN,CSP154	UF000,UF100	CRITICAL	ATCRTMR B1_SCX_PROD
338S00890	2	C,LIFUKA,B1,USB-C RETIMER,ASE,CSP154	UF000,UF100	CRITICAL	ATCRTMR B1_ASE_PROD
998-30147	2	C,LIFUKA,B2,USBC RETIMER,AXX,CSP154	UF000,UF100	CRITICAL	ATCRTMR B2_DEV
998-33058	2	C,LIFUKA,B2,USBC RE MER A06,CSP154	UF000,UF100	CRITICAL	ATCRTMR B2_A06_DEV
998 33083	2	C,LIFUKA,B2,USBC RETI ER,A 9,CSP154	UF000,UF100	CRITICAL	ATCRTMR B2_A09_DEV

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DES	COMMEN S
998-33083	998-33058	ALT_CMN	UF000,UF100	rdar //113696992

Ace3

PAR #	Q	DESCR P ION	REFERENCE DESIGNA OR(S)	CRI ICAL	BOM OP ION
353S03133	3	IC,SE0101S04,ACX3,A0,USB PD W/WV,WSA149	UF400,UF500	CRITICAL	USBCPC PORTABLE_A0
353S03508	3	IC,SE0101S05,ACX3,A1,USB PD W/WV,WSA149	UF400,UF500	CRITICAL	USBCPC PORTABLE_A1

eUSB Level Shifter

PAR #	Q	DESCR P ION	REFERENCE DESIGNA OR(S)	CRI ICAL	BOM OP ION
338S00908	2	IC,RTMR,CYUSB2402,A3,CSP24	UF600,UF650	CRITICAL	OTP_CORRECTED_V2_PORTABLE

Secure Element Prod and Dev

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DES	COMMEN S
338S00941	338S00956	ALT_CMN	U5000	

B Programmable Parts

USBC Ace3 SPI Flash

AR #	Q	DESCRIP ON	REFERENCE DES GNA OR(S)	CRI ICAL	BOM OP ION
335S00644	1	IC,SPI SERIAL FL SH,8M ITE, .0V,USON8	UF260	CRITICAL	UPC01_ROM BLANK

Winbond

PAR NUMBER	AL ERNA E FOR PAR NUM ER	BOM OP ION	REF D S	COMMEN S	
335S00537	335S00644	UPC01_ROM:BLANK	UF260	rdar //100123287	Macronix
335S00571	335S00644	UPC01_ROM:BLANK	UF260	rdar //100123287	Gigadevice

MagSafe Ace3 SPI Flash

PAR #	Q	DESCRIP ON	REFERENCE DE GNA OR(S)	CRI ICAL	BOM OP ION
335S00644	1	IC,SPI SERIAL FLASH,8MBITS,1.0V,USON8	U5660	CRITICAL	UPC5_ROM BLANK

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S	
335S00537	335S00644	UPC5_ROM:BLANK	U5660	rdar //100123287	Macronix
335S00571	335S00644	UPC5_ROM:BLANK	U5660	rdar //100123287	Gigadevice

SOC QSPI Flash

PAR #	Q	DESCRIP ON	REFERENCE DES GNA OR(S)	CRI ICAL	BOM OP ION
335S00575	1	IC,FLASH,8MBIT,1.2 ,QE=1 W,6X8MM,USON	U1900	CRITICAL	SOC_ROM BLANK

Macronix

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF D S	COMMEN S
335S00574	335S00575	SOC_ROM BLANK	U1900	Winbond rdar://108580217
335S00596	335S00575	SOC_ROM BLANK	U1900	Gigadevice rdar://108580217

Re-timer ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00638	2	IC FLASH,64MBIT,1 2V,QE=1,W CSP12	UF090,UF190	CRITICAL	ATCRTMR_ROM:CSP_BLANK

Gigadevice

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DES	COMMEN S
335S00573	335S00638	ATCRTMR_ROM:CSP_BLANK	UF090,UF190	Winbond rdar://108012086
335S00594	335S00638	ATCRTMR_ROM:CSP_BLANK	UF090,UF190	Macronix rdar://108012086

C USB-C Approved Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
376S00588	376S00078	QF910,QF940,QF960	TOSHIBA	VISHAY
353S4037	353S03251	UF690	TI	ON-SEMI
353S00636	353S03251	UF690	TI	PERICOM
353S03294	353S03251	UF690	TI	PERICOM

PAGE I LE
BOM: Prog and Module Parts

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
RE ISION 5.0.0
BRANCH dvt-1
PAGE 603 OF 801
SHEE 117 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC HE P SE OR AGREES O HE FOLLOWING I O MA N A N IS DOCUMEN N CONF DENCE III NO O REPRODUCE OR COP I III NO O RE EAL R PUBLISH I IN WHOLE OR PAR I ALL R GH S RESER ED

www.repairlap.com

MPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-30983	1	IC,PMU,STOWE,A1,OTP-CPC,WLCSP420	U8100	CRITICAL	MPMU_IC:A1_CPC
998-31475	1	IC,PMU,STOWE,A1,OTP-CPD,WLCSP420	U8100	CRITICAL	MPMU_IC:A1_CPD
998-31669	1	IC,PMU,STOWE,A1,OTP-CPE,WLCSP420	U8100	CRITICAL	MPMU_IC:A1_CPE
998-32325	1	IC,PMU,STOWE,A1,OTP-CPF,WLCSP420	U8100	CRITICAL	MPMU_IC:A1_CPF
998-32439	1	IC,PMU,STOWE,A1,OTP-CPG,WLCSP420	U8100	CRITICAL	MPMU_IC:A1_CPG

SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-30984	1	IC,PMU,VALE,A1,OTP-CPC,WLCSP196	U7700	CRITICAL	SPMU_IC:A1_CPC
998-32326	1	IC,PMU,VALE,A1,OTP-CPD,WLCSP196	U7700	CRITICAL	SPMU_IC:A1_CPD

PAGE TITLE
BOM: PMU

Apple Inc.

DRAWING NUMBER 051-09343
SIZE D
REVISION 5.0.0
BRANCH dvt-1
PAGE 604 OF 801
SHEET 118 OF 121

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE PARTIES OF AGREES TO THE FOLLOWING
I. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II. NOT TO REPRODUCE OR COPY IT
III. NOT TO REVEAL, PUBLISH IT IN WHOLE OR PART
IV. ALL RIGHTS RESERVED

www.repairlap.com

Resistors

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S		
107800033	107800034	ALT_CNN	ALL	rdar://problem/59471007	TFT	Cyntec
107800055	107800090	ALT_CNN	ALL	dar://problem/73982769	Cyntec	TFT
107800101	107800005	ALT_CNN	ALL	TB	Yageo	Cyntec
107800443	107800005	ALT_CNN	ALL	TBD	FT	Cyntec
107800102	107800017	ALT_CNN	ALL	TBD	Yageo	Cyntec
10780276	107800020	ALT_CNN	ALL	TBD	Cyntec	TFT
107800298	107800460	ALT_CNN	ALL	TBD	TDK	Murata
107800076	107800044	ALT_CNN	ALL	rdar://problem/71831138	Yageo	Cyntec
107800365	107800373	ALT_CNN	ALL	rd r://problem/71831414	Cyntec	TFT
1078 0475	107800044	ALT_CNN	ALL	Peter R Req 1/27	TF	Cyntec
107800325	107800232	ALT_CNN	ALL	Peter Re 1/27	FT	Cyntec
107800479	107800478	ALT_CNN	ALL	Peter R Req 1/27	Yageo	Cyntec
116800014	116800044	ALT_CNN	ALL	Peter R Req 1/27	Cyntec	TFT
104800138	104800135	ALT_CNN	ALL	rdar://97447887	Cyntec	TFT

Ceramic Capacitors

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM O ION	REF DES	COMMEN	A te nate Vendor	Primary Vendor
13880846	13880811	ALT_CNN	ALL	rdar://prob1 m/59474499	Sam ung	Murata
138800332	138800328	ALT_CNN	ALL	rdar://problem/74145755	Kyocera	Murata
138800229	138800107	ALT_CNN	ALL	rdar://108573025	Kyocera	Murata
138800078	138800107	ALT_CNN	ALL	rdar://108573025	Taiyo	Murata
138800022	13880801	ALT_CNN	ALL	rdar://problem/74146716	Taiyo	Murata/Samsung
138800181	13880835	ALT_CNN	ALL	ar / pr lem/74150148	Samsung	Murata
138800291	13880835	ALT_CNN	ALL	rdar:// rob1 m/ 4150148	Kyocera	Murata
138800197	138800409	ALT_CNN	ALL	rdar://proble /75264457	Mura a	Taiyo
138800413	138800410	ALT_CNN	ALL	rdar://problem/75264476	Mura a	Taiyo
138800164	138800138	ALT_CNN	ALL	rdar://problem/71831667	Taiyo	Kyocera
138800280	138800138	ALT_CNN	ALL	dar://problem/71831667	Samsung	Kyocera
138800139	138800138	ALT_CNN	ALL	rd r:/ problem/71831667	Mura a	Kyocera
138800047	138800073	ALT_CNN	ALL	rdar //p obl m/71831776	aiyo	Murata
138800097	13880750	ALT_CNN	ALL	rdar://p o lem 74149037	Taiyo Y den	Murata
138800151	138800149	ALT_CNN	ALL	rdar://problem/71832189	Taiyo	Murata
138800150	138800149	ALT_CNN	ALL	rdar://problem/71832189	SEMCO	Murata
138800148	138800149	ALT_CNN	ALL	rdar://problem/71832189	Kyocera	Murata
138800330	138800081	ALT_CNN	ALL	rd r:/problem/74146122	SEMCO	Murata
1388 771	138800336	ALT_CNN	ALL	rdar //p oblem/71832350	Taiyo	Murata
138800343	138800329	ALT_CNN	ALL	rdar:/ pro lem/71832255	Kyocera	Murata
138800284	138800136	ALT_CNN	ALL	rdar://problem/74149755	Kyoc ra	Murata
13880852	13880818	ALT_CNN	ALL	TBD	Samsung	Murata
138800031	13880861	ALT_CNN	ALL	rdar://73954319	Mura a/Taiyo	Murata
138800385	138800377	ALT_CNN	ALL	rdar://problem/73954114	Kyocera	Murata
138800416	138800328	ALT_CNN	ALL	rdar://problem/74145755	Taiyo Yuden	Murata
13880 087	138800482	ALT_CNN	ALL	T	aiyo Yuden	Murata
132800176	13280640	ALT_CNN	ALL	rdar:// rob1 m/ 1831575	Yageo	Murata
13881065	13881058	ALT_CNN	ALL	Peter R Req 27	Taiyo	Murata
131800633	131800506	ALT_CNN	ALL	Eric L Req 2/25	Kyocera/Taiyo	Murata
131800691	131800365	ALT_CNN	ALL	rdar://108571469	SEMCO	Murata
138800124	138800123	ALT_CNN	ALL	dar://96478420	Taiyo	Murata
138800345	138800134	ALT_CNN	ALL	rd r://108531210	aiyo	Murata
138800489	138800488	ALT_CNN	ALL	rdar://1085 0532	Kyocera	Murata
138800457	138800377	ALT_CNN	ALL	rdar://1 7 2 5 4	SEMCO	Murata
138800188	138800043	ALT_CNN	ALL	rdar://110740505	Taiyo	Murata
131800535	131800365	ALT_CNN	ALL	rdar://108571469	Taiyo	Murata

Poly-Tantalum Capacitors

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DES	COMMEN S		
128800031	128800011	ALT_CNN	ALL	rdar://problem/73938832	ROHM CORP	Kemet
128800026	128800011	ALT_CNN	ALL	rdar://problem/73938832	NEC	Kemet
128800131	128800094	ALT_CNN	ALL	rdar://91966007	Semco	Tokin/Kemet
128500069	128800094	ALT_CNN	ALL	rdar //91966007	Rohm	Tokin/Kemet
12880 106	128800107	ALT_CNN	ALL	r r:/ pro lem/73938270	Toki	Kemet
128800110	128800107	ALT_CNN	ALL	rdar:// rob1m/ 3938270	Samsung	Kemet

Inductors

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S		
152800398	152800204	ALT_CNN	ALL	rdar://problem/73959393	Taiyo	Cyntec
152800997	152800476	ALT_CNN	ALL	rdar://problem/73957780	Chil sin	Murata
152800991	152800984	ALT_CNN	ALL	rdar://problem/73958066	Taiyo	Cyntec
152801494	152801263	ALT_CNN	ALL	rdar://problem/73957626	Murata	Taiyo
152800343	152801325	ALT_CNN	ALL	rdar://problem/78474169	Cyntec	Mu ata
152800979	152800874	ALT_CNN	ALL	rdar://problem/73960389	Taiyo	Cyntec
152801548	152800289	ALT_CNN	ALL	rdar://problem/76165749	Murata	Cyntec
152800809	152800332	ALT_CNN	ALL	TBD	Taiyo Yuden	Cyntec
152801782	152801458	ALT_CNN	ALL	rdar://98672879	Sunlord	Cyntec
152801781	152801457	ALT_CNN	ALL	rdar://98673070	Sunlord	Cyntec
152801461	152801283	ALT_CNN	ALL	Peter R Req 1/27	Sunlord	Cyntec
152801836	152801268	ALT_CNN	ALL	rdar://problem/73958701	Taiyo	Cyntec
152801804	152800114	ALT_CNN	ALL	TBD	Chil sin	Cyntec
152801805	152800136	ALT_CNN	ALL	Per Louisa Zhang	Chil sin	Cyntec

Ferrites and Filters

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S		
155800034	1558 0302	ALT_CNN	ALL	rdar://108576666	Murata	Murata
1558 0741	1558 0361	ALT_CNN	ALL	TBD	Murata	TDK
155800867	1558 0644	ALT_CNN	ALL	rdar://108577302	TDK	Murata
155800374	1558 0676	ALT_CNN	ALL	TBD	TDK	M rata
155800885	155800188	ALT_CNN	ALL	rdar://108573925	TDK	Mu ata

Fuses

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S		
740800081	740800053	ALT_CNN	ALL	rdar://problem/73218321	Bourns	AEM

Diodes and TVSs

PAR NUMBER	AL E NA E FOR PAR UM ER	BOM OP ION	REF D S	COMMEN S		
377800166	377800160	ALT_CNN	ALL	rdar://problem/59407974	Semtech	O Semi
377800123	377800031	ALT_CNN	ALL	rdar://problem/59407768	Semtech	On Semi
377800186	377800060	ALT_CNN	ALL	rdar://problem/59407847	Semtech	ST Micro
377800210	377800172	ALT_CNN	ALL	rdar://problem/73218476	Semtech	TI
371800325	371800065	ALT_CNN	ALL	rdar://problem/59 045 1	Diodes Inc	On Semi
371800284	371800187	ALT_CNN	ALL	rdar:/ problem/761 1510	NXP	On Semi
371800240	371800364	ALT_CNN	ALL	rdar://problem/76171942	NXP	Diodes
371800205	371800077	ALT_CNN	ALL	LOUISA REQ.	Vishay	NXP
371800220	371800307	ALT_CNN	ALL	rdar://problem/73940785	On Semi	Diodes Inc
371800370	371800062	ALT_CNN	ALL		Diodes Inc	On Semi
371800217	371800079	ALT_CNN	ALL	rdar://109469452		
371800435	371800079	ALT_CNN	ALL	rdar://107029515		

Crystals and XOs

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DE	COMMEN S		
197800318	197800323	ALT_CNN	ALL	rdar://problem/75588335	NDK	TXC
197800335	197800323	ALT_CNN	ALL	rdar://problem/75588335	Kyocera	TXC
197800391	197800323	ALT_CNN	ALL	rdar://98214743	Kyocera	TXC
19780590	19780591	ALT_CNN	ALL	rdar://problem/739533 5	EPSON	NDK
19780588	19780591	ALT_CNN	ALL	rdar://problem/73953315	TXC	NDK

Analog ICs

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ION	REF DES	COMMEN S		
353801655	353803149	ALT_CNN	ALL		On Semi	TI
353802434	35383332	ALT_CNN	ALL	rdar://108579720	On Semi	TI

Discrete FETs

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DES	COMMEN S		
376800253	376800076	ALT_CNN	ALL		On Semi	Toshiba
376800228	37681179	ALT_CNN	ALL	rd r:/ problem/73939839	Fairch ld	Vishay
376800007	37681179	ALT_CNN	ALL	rda :/problem/73939839	Alt for 72W Charger AOS	Vishay
37681147	376800281	ALT_CNN	ALL	rdar://pr blo /73 40267	On Semi	AOS
376800632	37680820	ALT_CNN	ALL	rdar://10078591	Diodes I c	On Semi
37680725	37680604	ALT_CNN	ALL	LOUISA REQ.	Vishay	On Semi

376800516	376800544	ALT_CNN	ALL	rdar //100786186	On Semi	Toshiba
376800618	376800544	ALT_CNN	ALL	rdar:/ 10 786 86	Dio es c	Toshiba
376800292	376800294	ALT_CNN	ALL	rdar://100 0 454	Nex eria	Diodes Inc
376800633	376800294	ALT_CNN	ALL	rdar://100804454	Diodes Inc	Diodes Inc
376800303	376800012	ALT_CNN	ALL	rdar://problem/73219339	Diodes Inc	TI
376800519	376800521	ALT_CNN	ALL	rdar:/ 91767233	Vishay	On Semi
376800332	376800074	ALT_CNN	ALL	rdar://100804973	Nexperia	Toshiba
376800588	376800074	ALT_CNN	ALL	rdar:/ 100804973	Vishay	Toshiba
376800078	376800074	ALT_CNN	ALL	rdar://1 08 4973	Toshiba	Toshiba
376800634	376800074	ALT_CNN	ALL	rdar://100804973	Diodes In	Toshiba
376800647	376800074	ALT_CNN	ALL	rdar://100804973	Diodes Inc	Toshiba
376800588	376800078	ALT_CNN	ALL	rdar://100803216	Vishay	Toshiba
376800634	376800078	ALT_CNN	ALL	rdar://100803216	Diodes Inc	Toshiba
376800647	376800078	ALT_CNN	ALL	rd r:/ 100803216	Diodes Inc	Toshiba
3763005 8	376800078	ALT_CNN	ALL	rda :/91590 33	Vishay	Toshiba
376800634	376800078	ALT_CNN	ALL	rdar://91 908 3	Diodes Inc	Toshiba
376800647	376800078	ALT_CNN	ALL	rdar://91590833	Diodes I c	Toshiba
376800224	376800557	ALT_CNN	ALL	rdar://105746357	Nexperia	Diodes Inc

Logic ICs

PAR NUMBER	AL ERNA E FOR PAR NUMBER	BOM OP ON	REF DES	COMMEN S		
311800392	311800129	ALT_CNN	ALL	rdar:/ pr blo /59489090	Nexperia	TI
311800269	311800234	ALT_CNN	ALL	rdar://pro 1 m/59489341	Nex eria	TI
311800267	311800244	ALT_CNN	ALL	TBD	Nexperia	TI
311800268	311800246	ALT_CNN	ALL	TBD	Nexperia	TI
311800317	311800316	ALT_CNN	ALL	TBD	Nexperia	TI
311800272	311800287	ALT_CNN	ALL	TBD	Nexperia	TI
311800386	311800336	ALT_CNN	ALL	rdar:/ 87560278	TI	NXP/Diodes
31180612	311800263	ALT_CNN	ALL	rdar://p ob em/76165274	NXP	TI
311800322	311800321	ALT_CNN	ALL	rdar://problem/7 34560	Nexpe ia	TI
311800230	311800212	ALT_CNN	ALL	rdar://problem/71866365	Nexperia	TI
311800078	311800275	ALT_CNN	ALL		Nexperia	TI
311800385	311800323	ALT_CNN	ALL		Nexperia	TI
311800360	311800362	ALT_CNN	ALL		Nexperia	TI

PAGE I LE
BOM: Alternates

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D
RE ISION 5.0.0
BRANCH dvt-1
PAGE 610 OF 801
SHEE 119 OF 121

NOTICE OF PROPRIETARY PROPERTY
HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC
HE P SE OR AGREES O HE FOLLOWING
I O MA N A N IS DOCUMEN N CONF DENCE
II NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR
I ALL R GH S RESER ED

www.repairlap.com

Hynix	HY	H
Micron	MI	M
Samsung	SS	S

APN	EEEEEEE	DESC	BOMOPTIONs
639-20091	0000FAM	PCBA,MLB,SOC,BEST,HY-8G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:BEST_C0_HY_8GB
639-20061	0000F71	PCBA,MLB,SOC,BEST,HY-8G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:BEST_C0_HY_8GB
639-20081	0000F7M	PCBA,MLB,SOC,BEST,HY-8G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:BEST_C0_HY_8GB
639-20057	0000F6X	PCBA,MLB,SOC,BEST,HY-8G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:BEST_C0_HY_8GB
639-20049	0000FJV	PCBA,MLB,SOC,GOOD,HY-8G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:GOOD_C0_HY_8GB
639-20069	0000F79	PCBA,MLB,SOC,GOOD,HY-8G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:GOOD_C0_HY_8GB
639-20087	0000FA7	PCBA,MLB,SOC,GOOD,HY-8G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:GOOD_C0_HY_8GB
639-20053	0000F6T	PCBA,MLB,SOC,GOOD,HY-8G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:GOOD_C0_HY_8GB
639-20055	0000F6V	PCBA,MLB,SOC,BEST,HY-8G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:BEST_C0_HY_8GB
639-20074	0000F7E	PCBA,MLB,SOC,BEST,HY-8G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:BEST_C0_HY_8GB
639-20078	0000F7J	PCBA,MLB,SOC,BEST,HY-8G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:BEST_C0_HY_8GB
639-20073	0000F7D	PCBA,MLB,SOC,BEST,HY-8G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:BEST_C0_HY_8GB
639-20064	0000F74	PCBA,MLB,SOC,GOOD,HY-8G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:GOOD_C0_HY_8GB
639-20102	0000FAZ	PCBA,MLB,SOC,GOOD,HY-8G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:GOOD_C0_HY_8GB
639-20094	0000FAR	PCBA,MLB,SOC,GOOD,HY-8G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:GOOD_C0_HY_8GB
639-20065	0000F75	PCBA,MLB,SOC,GOOD,HY-8G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:GOOD_C0_HY_8GB
639-20089	0000FAK	PCBA,MLB,SOC,BEST,HY-16G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:BEST_C0_HY_16GB
639-20056	0000F6W	PCBA,MLB,SOC,BEST,HY-16G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:BEST_C0_HY_16GB
639-20077	0000F7H	PCBA,MLB,SOC,BEST,HY-16G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:BEST_C0_HY_16GB
639-20051	0000F6R	PCBA,MLB,SOC,BEST,HY-16G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:BEST_C0_HY_16GB
639-20093	0000FAQ	PCBA,MLB,SOC,GOOD,HY-16G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:GOOD_C0_HY_16GB
639-20063	0000F73	PCBA,MLB,SOC,GOOD,HY-16G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:GOOD_C0_HY_16GB
639-20083	0000F7P	PCBA,MLB,SOC,GOOD,HY-16G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:GOOD_C0_HY_16GB
639-20048	0000FJU	PCBA,MLB,SOC,GOOD,HY-16G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:GOOD_C0_HY_16GB
639-20046	0000F6L	PCBA,MLB,SOC,BEST,HY-16G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:BEST_C0_HY_16GB
639-20068	0000F78	PCBA,MLB,SOC,BEST,HY-16G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:BEST_C0_HY_16GB
639-20072	0000F7C	PCBA,MLB,SOC,BEST,HY-16G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:BEST_C0_HY_16GB
639-20067	0000F77	PCBA,MLB,SOC,BEST,HY-16G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:BEST_C0_HY_16GB
639-20058	0000F6Y	PCBA,MLB,SOC,GOOD,HY-16G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:GOOD_C0_HY_16GB
639-20098	0000FAV	PCBA,MLB,SOC,GOOD,HY-16G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:GOOD_C0_HY_16GB
639-20097	0000FAU	PCBA,MLB,SOC,GOOD,HY-16G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:GOOD_C0_HY_16GB
639-20075	0000F7F	PCBA,MLB,SOC,GOOD,HY-16G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:GOOD_C0_HY_16GB
639-20090	0000FAL	PCBA,MLB,SOC,BEST,HY-24G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:BEST_C0_HY_24GB
639-20059	0000F6Z	PCBA,MLB,SOC,BEST,HY-24G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:BEST_C0_HY_24GB
639-20079	0000F7K	PCBA,MLB,SOC,BEST,HY-24G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:BEST_C0_HY_24GB
639-20054	0000F6U	PCBA,MLB,SOC,BEST,HY-24G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:BEST_C0_HY_24GB
639-20047	0000FT	PCBA,MLB,SOC,GOOD,HY-24G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:GOOD_C0_HY_24GB
639-20066	0000F76	PCBA,MLB,SOC,GOOD,HY-24G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:GOOD_C0_HY_24GB
639-20085	0000F7R	PCBA,MLB,SOC,GOOD,HY-24G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:GOOD_C0_HY_24GB
639-20050	0000F6Q	PCBA,MLB,SOC,GOOD,HY-24G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:GOOD_C0_HY_24GB
639-20052	0000F6S	PCBA,MLB,SOC,BEST,HY-24G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:BEST_C0_HY_24GB
639-20071	0000F7B	PCBA,MLB,SOC,BEST,HY-24G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:BEST_C0_HY_24GB
639-20076	0000F7G	PCBA,MLB,SOC,BEST,HY-24G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:BEST_C0_HY_24GB
639-20070	0000F7A	PCBA,MLB,SOC,BEST,HY-24G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:BEST_C0_HY_24GB
639-20060	0000F70	PCBA,MLB,SOC,GOOD,HY-24G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:GOOD_C0_HY_24GB
639-20100	0000FAX	PCBA,MLB,SOC,GOOD,HY-24G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:GOOD_C0_HY_24GB
639-20082	0000F7N	PCBA,MLB,SOC,GOOD,HY-24G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:GOOD_C0_HY_24GB
639-20062	0000F72	PCBA,MLB,SOC,GOOD,HY-24G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:GOOD_C0_HY_24GB

APN	EEEEEEE	DESC	BOMOPTIONs
639-18692	000058Z	PCBA,MLB,SOC,BEST,MI-16G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:BEST_C0_MI_16GB
639-18713	000059L	PCBA,MLB,SOC,BEST,MI-16G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:BEST_C0_MI_16GB
639-18690	000058X	PCBA,MLB,SOC,BEST,MI-16G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:BEST_C0_MI_16GB
639-18700	0000597	PCBA,MLB,SOC,BEST,MI-16G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:BEST_C0_MI_16GB
639-18701	0000598	PCBA,MLB,SOC,GOOD,MI-16G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:GOOD_C0_MI_16GB
639-18708	000059F	PCBA,MLB,SOC,GOOD,MI-16G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:GOOD_C0_MI_16GB
639-18699	0000596	PCBA,MLB,SOC,GOOD,MI-16G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:GOOD_C0_MI_16GB
639-18705	000059C	PCBA,MLB,SOC,GOOD,MI-16G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:GOOD_C0_MI_16GB
639-18720	000059T	PCBA,MLB,SOC,BEST,MI-16G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:BEST_C0_MI_16GB
639-18730	00005A3	PCBA,MLB,SOC,BEST,MI-16G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:BEST_C0_MI_16GB
639-18717	0000590	PCBA,MLB,SOC,BEST,MI-16G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:BEST_C0_MI_16GB
639-18723	000059W	PCBA,MLB,SOC,BEST,MI-16G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:BEST_C0_MI_16GB
639-18728	00005A1	PCBA,MLB,SOC,GOOD,MI-16G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:GOOD_C0_MI_16GB
639-18735	00005A8	PCBA,MLB,SOC,GOOD,MI-16G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:GOOD_C0_MI_16GB
639-18715	000059N	PCBA,MLB,SOC,GOOD,MI-16G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:GOOD_C0_MI_16GB
639-18732	00005A5	PCBA,MLB,SOC,GOOD,MI-16G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:GOOD_C0_MI_16GB
639-18695	0000592	PCBA,MLB,SOC,BEST,MI-24G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:BEST_C0_MI_24GB
639-18716	000059P	PCBA,MLB,SOC,BEST,MI-24G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:BEST_C0_MI_24GB
639-18693	0000590	PCBA,MLB,SOC,BEST,MI-24G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:BEST_C0_MI_24GB
639-18703	0000594	PCBA,MLB,SOC,BEST,MI-24G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:BEST_C0_MI_24GB
639-18694	0000591	PCBA,MLB,SOC,GOOD,MI-24G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:GOOD_C0_MI_24GB
639-18711	000059J	PCBA,MLB,SOC,GOOD,MI-24G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:GOOD_C0_MI_24GB
639-18702	0000599	PCBA,MLB,SOC,GOOD,MI-24G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:GOOD_C0_MI_24GB
639-18707	000059F	PCBA,MLB,SOC,GOOD,MI-24G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:GOOD_C0_MI_24GB
639-18722	000059V	PCBA,MLB,SOC,BEST,MI-24G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:BEST_C0_MI_24GB
639-18733	00005A6	PCBA,MLB,SOC,BEST,MI-24G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:BEST_C0_MI_24GB
639-18709	000059G	PCBA,MLB,SOC,BEST,MI-24G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:BEST_C0_MI_24GB
639-18726	000059Z	PCBA,MLB,SOC,BEST,MI-24G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:BEST_C0_MI_24GB
639-18731	00005A4	PCBA,MLB,SOC,GOOD,MI-24G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:GOOD_C0_MI_24GB
639-18736	00005A9	PCBA,MLB,SOC,GOOD,MI-24G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:GOOD_C0_MI_24GB
639-18718	000059R	PCBA,MLB,SOC,GOOD,MI-24G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:GOOD_C0_MI_24GB
639-18724	000059X	PCBA,MLB,SOC,GOOD,MI-24G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:GOOD_C0_MI_24GB
639-18698	0000595	PCBA,MLB,SOC,BEST,SS-8G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:BEST_C0_SA_8GB
639-18706	000059D	PCBA,MLB,SOC,BEST,SS-8G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:BEST_C0_SA_8GB
639-18696	0000593	PCBA,MLB,SOC,BEST,SS-8G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:BEST_C0_SA_8GB
639-18704	000059B	PCBA,MLB,SOC,BEST,SS-8G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:BEST_C0_SA_8GB
639-18697	0000594	PCBA,MLB,SOC,GOOD,SS-8G,KX-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_256G,SOC:GOOD_C0_SA_8GB
639-18714	000059M	PCBA,MLB,SOC,GOOD,SS-8G,KX-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_512G,SOC:GOOD_C0_SA_8GB
639-18691	000063J	PCBA,MLB,SOC,GOOD,SS-8G,KX-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_1P0T,SOC:GOOD_C0_SA_8GB
639-18710	000059H	PCBA,MLB,SOC,GOOD,SS-8G,KX-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:KX_2P0T,SOC:GOOD_C0_SA_8GB
639-18725	000059Y	PCBA,MLB,SOC,BEST,SS-8G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:BEST_C0_SA_8GB
639-18734	00005A7	PCBA,MLB,SOC,BEST,SS-8G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:BEST_C0_SA_8GB
639-18712	000059K	PCBA,MLB,SOC,BEST,SS-8G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:BEST_C0_SA_8GB
639-18729	00005A2	PCBA,MLB,SOC,BEST,SS-8G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:BEST_C0_SA_8GB
639-18721	000059U	PCBA,MLB,SOC,GOOD,SS-8G,WD-256G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_256G,SOC:GOOD_C0_SA_8GB
639-18737	00005AA	PCBA,MLB,SOC,GOOD,SS-8G,WD-512G,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_512G,SOC:GOOD_C0_SA_8GB
639-18719	000059S	PCBA,MLB,SOC,GOOD,SS-8G,WD-1P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_1P0T,SOC:GOOD_C0_SA_8GB
639-18727	00005A0	PCBA,MLB,SOC,GOOD,SS-8G,WD-2P0T,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:WD_2P0T,SOC:GOOD_C0_SA_8GB
685-00547		COMMON PARTS,MLB,X2818	MLB_COMMON,SSD_2L,SYS_BOOT_PWR:DEFAULT_500MA
939-15447	000063K	PCBA,MLB,DCDC,X2818	ALTERNATE:PART,ALT_CMN,CMN_PARTS_BOM,DEV_PARTS_BOM,NANDCFG:INTERPOSER,SOC:INTERPOSER
[illegible]	[illegible]	PCBA,MLB,RF-CHAR,X2818	RF_COMMON
[illegible]		DEV PARTS,MLB,X2818	ALTERNATE:PART,ALT_CMN,MLB_DEV

Common BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00547	COMMON PARTS,MLB,X2818	MLB_COMMON,ALT_CMN,ALTERNATE:PART,SSD_2L
985-02073	DEV PARTS,MLB,X2818	MLB_DEV,ALT_CMN,ALTERNATE:PART

SYNC DATE=

PAGE TITLE

BOM: Variants

Apple Inc.

DRAWING NUMBER 051-09343 SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 611 OF 801

SHEET 120 OF 121

NOTICE OF PROPRIETARY PROPERTY

HE N ORMA ION CON AINED HEREIN IS HE PRO RIE AR PROPER OF APPLE INC
HE P SE OR AGREES O HE FOLLOWING
I O MA N A N IS DOCUMEN N CONF DENCE
II NO O REPRODUCE OR COP I
III NO O RE EAL R PUBLISH I IN WHOLE OR PAR
I ALL R GH S RESER ED

www.repairlap.com

End of Schematic

PAGE TITLE

Apple Inc.

DRAWING NUMBER 051-09343

SIZE D

REVISION 5.0.0

BRANCH dvt-1

PAGE 801 OF 801

SHEET 121 OF 121

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. EXCEPT WHERE THE PRIOR WRITTEN CONSENT OF APPLE INC. HAS BEEN OBTAINED, THE RECEIPT OF THIS DOCUMENT CONSTITUTES AGREEMENT BY THE RECIPIENT THE FOLLOWING: (1) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE, (2) NOT TO REPRODUCE OR COPY IT, (3) NOT TO REVEAL, PUBLISH OR PUBLICIZE IT IN WHOLE OR PART, (4) TO RETURN IT ON REQUEST. ALL RIGHTS RESERVED.

www.repairlap.com