

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ECN

DESCRIPTION OF REVISION

CK APPD  
DATE

2010-10-12

SCHEM, FLYING DUTCHMAN, MLB, K91F

REV B RELEASE, 01/31/11

Page

(.csa)

Contents

Sync

Date

1

1

Table of Contents

MASTER

MASTER

2

2

System Block Diagram

K17\_REF

06/30/2009

3

3

Power Block Diagram

K17\_REF

06/30/2009

4

4

Revision History

MASTER

MASTER

5

5

BOM Configuration

K17\_REF

05/28/2009

6

7

Functional / ICT Test

K18\_MLB

04/27/2010

7

8

Power Aliases

K18\_MLB

04/27/2010

8

9

Signal Aliases

K18\_MLB

04/27/2010

9

10

CPU DMI/PEG/FDI/RSVD

K92\_SUMA

06/21/2010

10

11

CPU CLOCK/MISC/JTAG

K92\_MLB

08/03/2010

11

12

CPU DDR3 INTERFACES

K92\_SUMA

06/15/2010

12

13

CPU POWER

K92\_MLB

08/03/2010

13

14

CPU POWER AND GND

K92\_SUMA

06/15/2010

14

16

CPU DECOUPLING-I

K92\_MLB

08/19/2010

15

17

CPU DECOUPLING-II

K92\_MLB

08/19/2010

16

18

PCH SATA/PCIE/CLK/LPC/SPI

K91\_MLB

10/19/2010

17

19

PCH DMI/FDI/GRAPHICS

K92\_MLB

07/06/2010

18

20

PCH PCI/FLASHCACHE/USB

K92\_MLB

07/06/2010

19

21

PCH MISC

K91\_MLB

10/20/2010

20

22

PCH POWER

K92\_MLB

07/06/2010

21

23

PCH GROUNDS

K92\_MLB

04/30/2010

22

24

PCH DECOUPLING

K92\_MLB

07/06/2010

23

25

CPU & PCH XDP

K91\_MLB

10/17/2010

24

26

USB HUBS

K91\_ERIC

10/08/2010

25

28

Chipset Support

K92\_MLB

07/06/2010

26

29

DDR3 SO-DIMM Connector A

K92\_SUMA

06/23/2010

27

30

DDR3 Byte/Bit Swaps

K92\_SUMA

05/10/2010

28

31

DDR3 SO-DIMM Connector B

K92\_SUMA

06/23/2010

29

32

CPU Memory S3 Support

K18\_MLB

04/27/2010

30

33

FSB/DDR3/FRAMEBUF Vref Margining

K18\_MLB

04/27/2010

31

34

X19/ALS/CAMERA CONNECTOR

K91\_MARY

10/08/2010

32

35

SD READER CONNECTOR

K91\_ERIC

10/08/2010

33

36

T29 Host (1 of 2)

T29\_REF

10/12/2010

34

37

T29 Host (2 of 2)

T29\_REF

10/12/2010

35

38

T29 Power Support

T29\_REF

10/12/2010

36

39

ETHERNET PHY (CAESAR IV)

K91\_ERIC

10/11/2010

37

40

Ethernet Connector

K91\_TRINHNI

05/26/2010

38

41

FireWire LLC/PHY (FW643)

K18\_MLB

04/27/2010

39

42

FireWire Port & PHY Power

T27\_REF

06/10/2010

40

43

FireWire Connector

T27\_REF

06/10/2010

41

45

SATA/IR/SIL Connectors

K91\_ERIC

11/08/2010

42

46

External USB Connectors

K91\_ERIC

10/08/2010

43

48

Front Flex Support

K18\_MLB

04/27/2010

44

49

SMC

K91\_BEN

07/12/2010

45

50

SMC Support

K91\_BEN

07/12/2010

Page

(.csa)

Contents

Sync

Date

46

51

LPC+SPI Debug Connector

K18\_MLB

04/27/2010

47

52

SMBus Connections

K18\_MLB

04/27/2010

48

53

Voltage & Load Side Current Sensing

K91\_DINESH

08/16/2010

49

54

High Side and CPU/AXG Current Sensing

K91\_DINESH

10/29/2010

50

55

Thermal Sensors

K91\_DINESH

09/22/2010

51

56

Fan Connectors

K18\_MLB

04/27/2010

52

57

WELLSPRING 1

K91\_ERIC

10/08/2010

53

58

WELLSPRING 2

K91\_ERIC

07/14/2010

54

59

Digital Accelerometer

K91\_DINESH

08/06/2010

55

61

SPI ROM

K91\_BEN

06/08/2010

56

62

AUDIO: CODEC/REGULATOR

K91\_AUDIO

09/30/2010

57

63

AUDIO: LINE INPUT FILTER

K91\_AUDIO

07/12/2010

58

65

AUDIO: HEADPHONE FILTER

K91\_AUDIO

07/12/2010

59

66

AUDIO: SPEAKER AMP

K91\_AUDIO

07/12/2010

60

67

AUDIO: JACKS

K91\_AUDIO

09/30/2010

61

68

AUDIO: JACK TRANSLATORS

K91\_AUDIO

09/21/2010

62

69

DC-In & Battery Connectors

K91\_ERIC

10/08/2010

63

70

PBus Supply & Battery Charger

K91\_CHANG

07/20/2010

64

71

System Agent Supply

K91\_ERIC

10/08/2010

65

72

5V / 3.3V Power Supply

K91\_ERIC

10/08/2010

66

73

1.5V DDR3 Supply

K91\_ERIC

10/08/2010

67

74

CPU IMVP7 & AXG VCore Regulator

K91\_ERIC

10/08/2010

68

75

CPU IMVP7 & AXG VCore Output

K91\_ERIC

09/22/2010

69

76

CPU VCCIO (1.05V) Power Supply

K91\_ERIC

10/08/2010

70

77

Misc Power Supplies

K91\_ERIC

11/01/2010

71

78

Power FETs

K91\_MARY

10/14/2010

72

79

Power Control 1/ENABLE

K91\_MARY

07/22/2010

73

80

Whistler PCI-E

K92\_SUMA

06/15/2010

74

81

Whistler CORE/FB POWER

K92\_SUMA

06/15/2010

75

82

Whistler FRAME BUFFER I/F

K92\_MLB

08/03/2010

76

84

GDDR5 Frame Buffer A

K92\_MLB

08/19/2010

77

85

GDDR5 Frame Buffer B

K92\_MLB

08/19/2010

78

86

Whistler LVDS/DP/GPIO

K92\_MLB

12/01/2010

79

87

Whistler GPIOs & STRAPs

K92\_MLB

11/23/2010

80

88

Whistler DP PWR/GNDs

K92\_SUMA

06/15/2010

81

89

GPU (Whistler) CORE SUPPLY

K91\_ERIC

12/21/2010

82

90

LVDS Display Connector

K18\_MLB

04/27/2010

83

92

Muxed Graphics Support

K92\_MLB

11/21/2010

84

93

DisplayPort/T29 A MUXing

T29\_REF

10/16/2010

85

94

DisplayPort/T29 A Connector

T29\_REF

10/16/2010

86

95

1V0 GPU / 1V5 FB Power Supply

K91\_ERIC

10/08/2010

87

96

Graphics MUX (GMUX)

K91\_MARY

08/03/2010

88

97

LCD Backlight Driver

K90I\_KIRAN

06/25/2010

89

99

Power Sequencing EG/PCH S0

K91\_MARY

08/03/2010

90

100

CPU Constraints

K92\_MLB

08/09/2010

Page

(.csa)

Contents

Sync

Date

91

101

Memory Constraints

K18\_MLB

04/27/2010

92

102

PCH Constraints 1

K92\_MLB

08/09/2010

93

103

PCH Constraints 2

K92\_MLB

08/09/2010

94

104

Ethernet/FW Constraints

K91\_ERIC

08/03/2010

95

105

T29 Constraints

T29\_REF

10/16/2010

96

106

SMC Constraints

K18\_MLB

04/27/2010

97

107

GPU (Whistler) CONSTRAINTS

K92\_MLB

08/09/2010

98

108

Project Specific Constraints

K18\_MLB

04/27/2010

99

109

PCB Rule Definitions

K18\_MLB

04/27/2010

100

130

DEBUG SENSORS AND ADC

K91\_DINESH

08/06/2010

101

132

Power Supplies BIST

K91\_DINESH

08/18/2010

ALIASES

RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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820-2915	1	PCBF, MLB, K91	PCB	CRITICAL	

DRAWING  
TITLE=MLB  
ABBREV=DRAWING  
LAST\_MODIFIED=Mon Jan 31 12:49:37 2011

DRAWING TITLE

SCHEM, MLB, K91

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PAGE

SHEET

SIZE

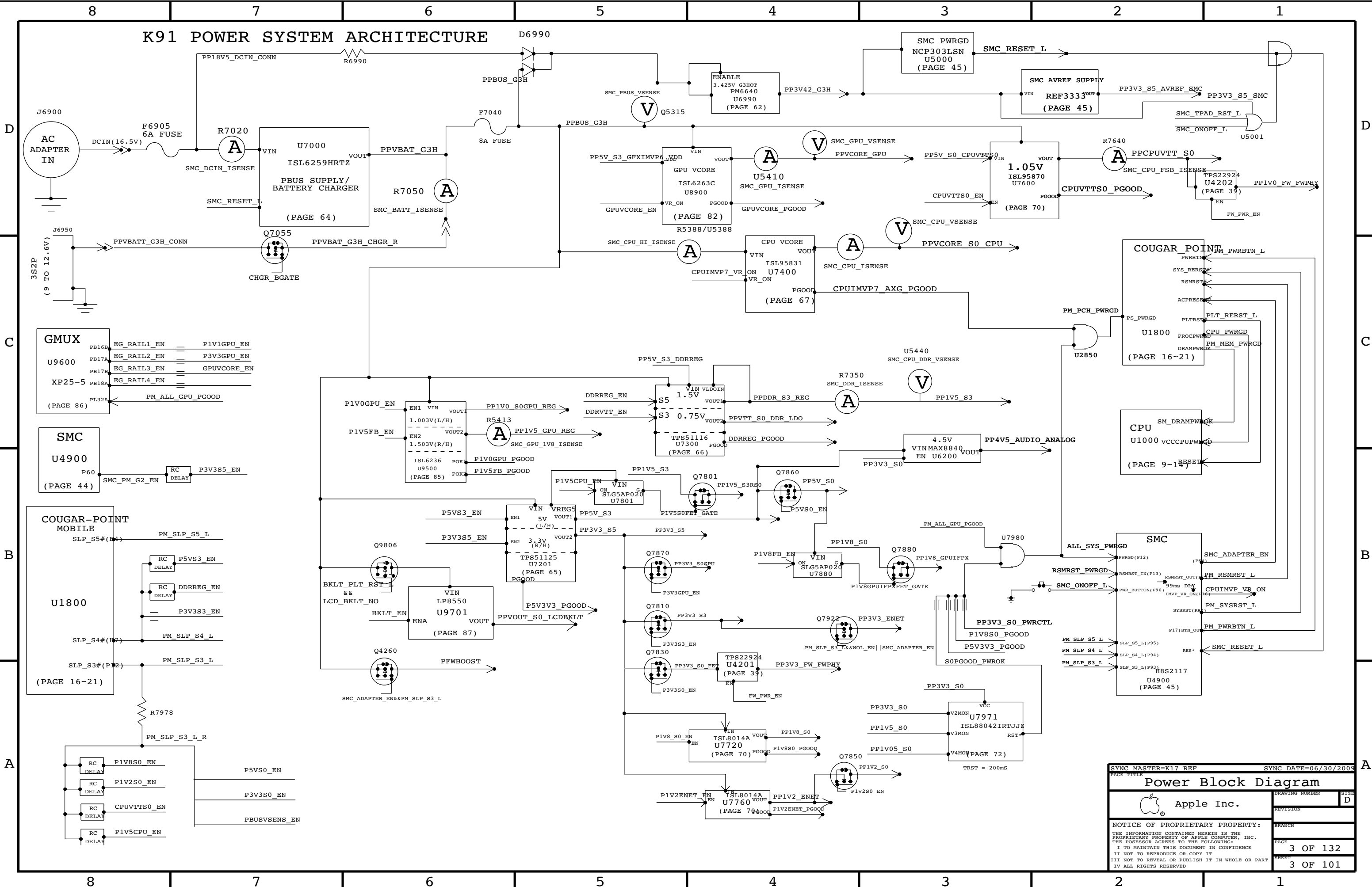
D

1 OF 132

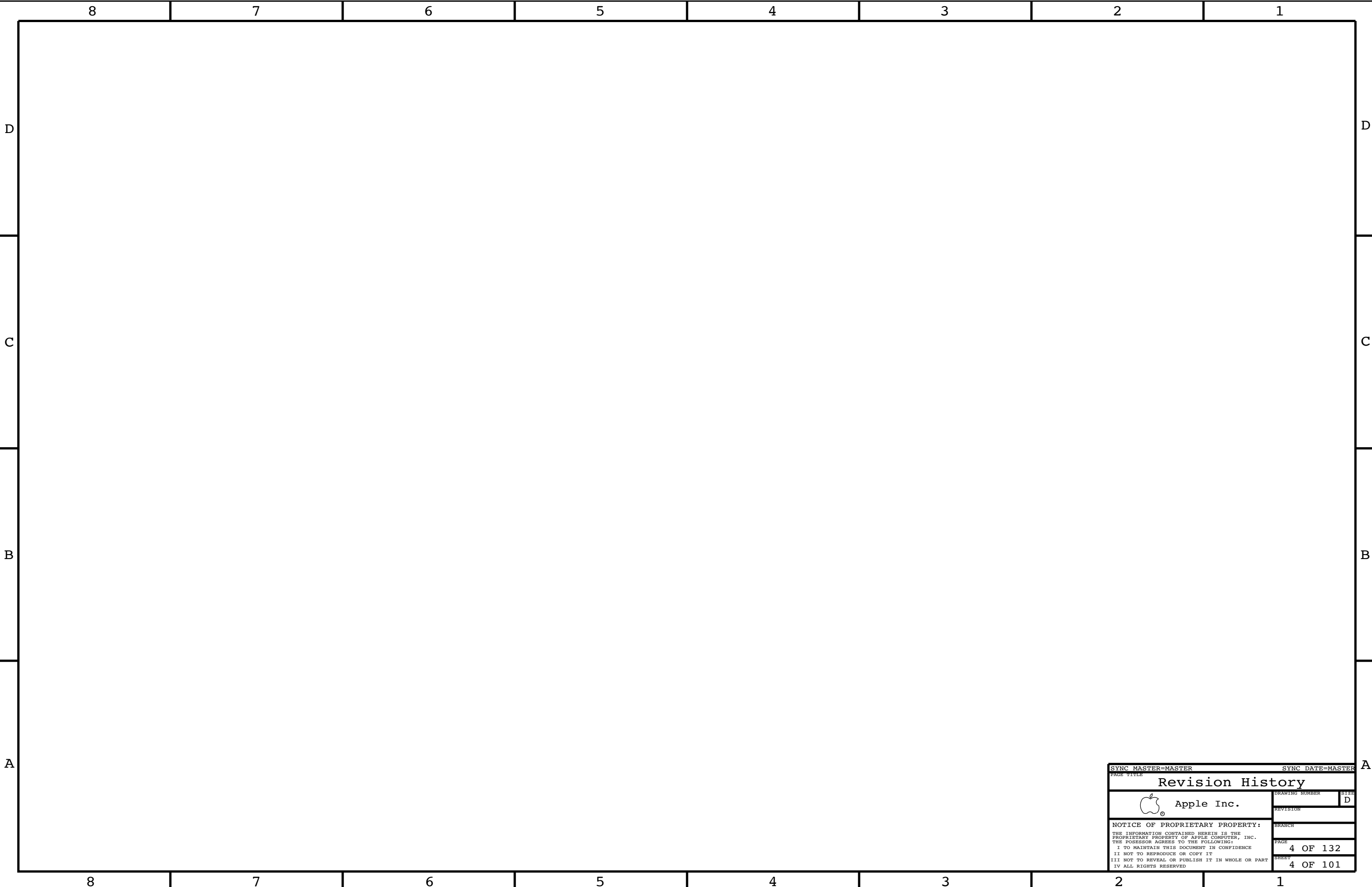
1 OF 101




K91 POWER SYSTEM ARCHITECTURE



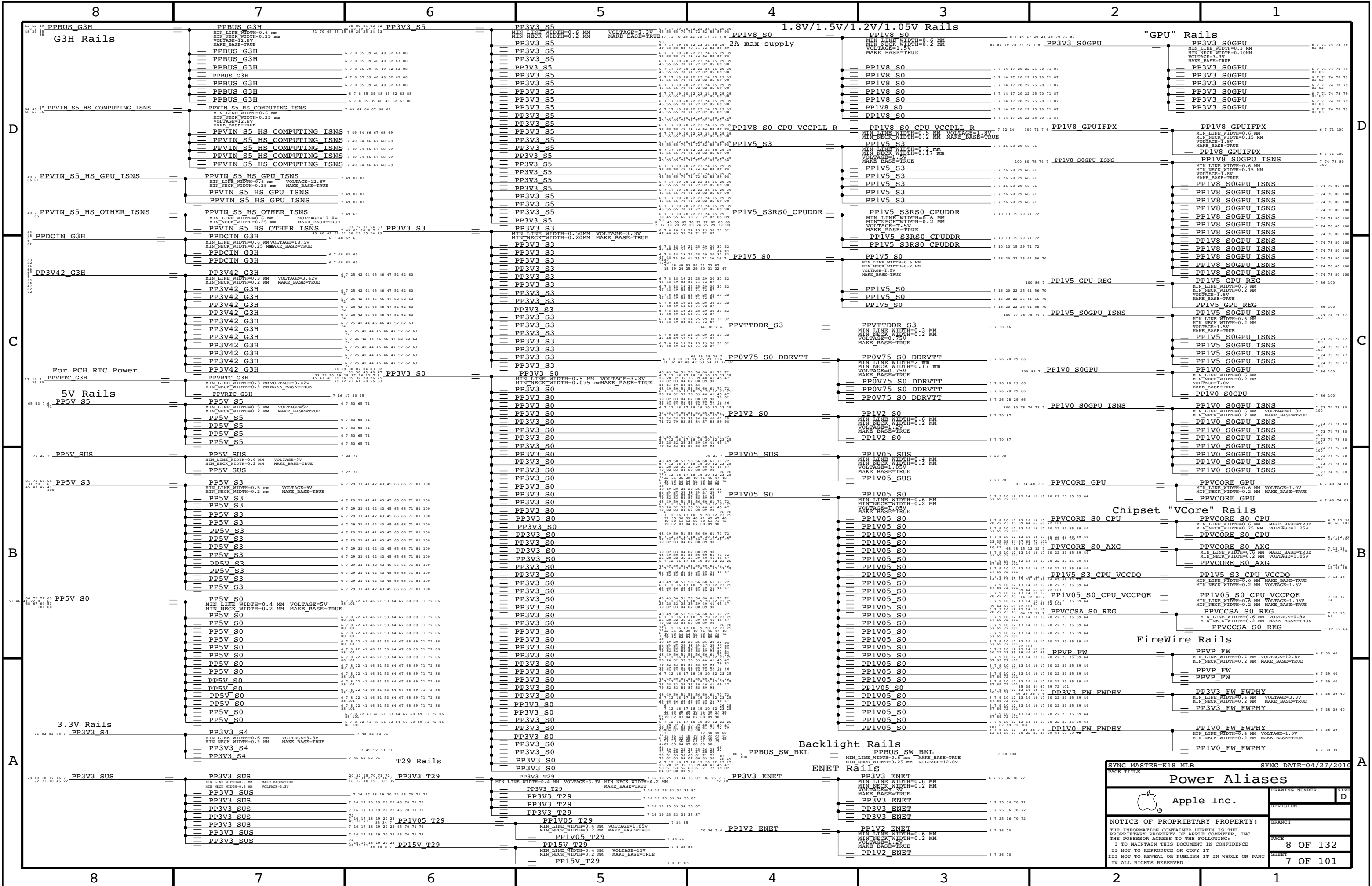
PAGE TITLE		PAGE	
Power Block Diagram		3 OF 132	
Apple Inc.		3 OF 101	
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SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
Revision History			
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	4 OF 132
		SHEET	4 OF 101

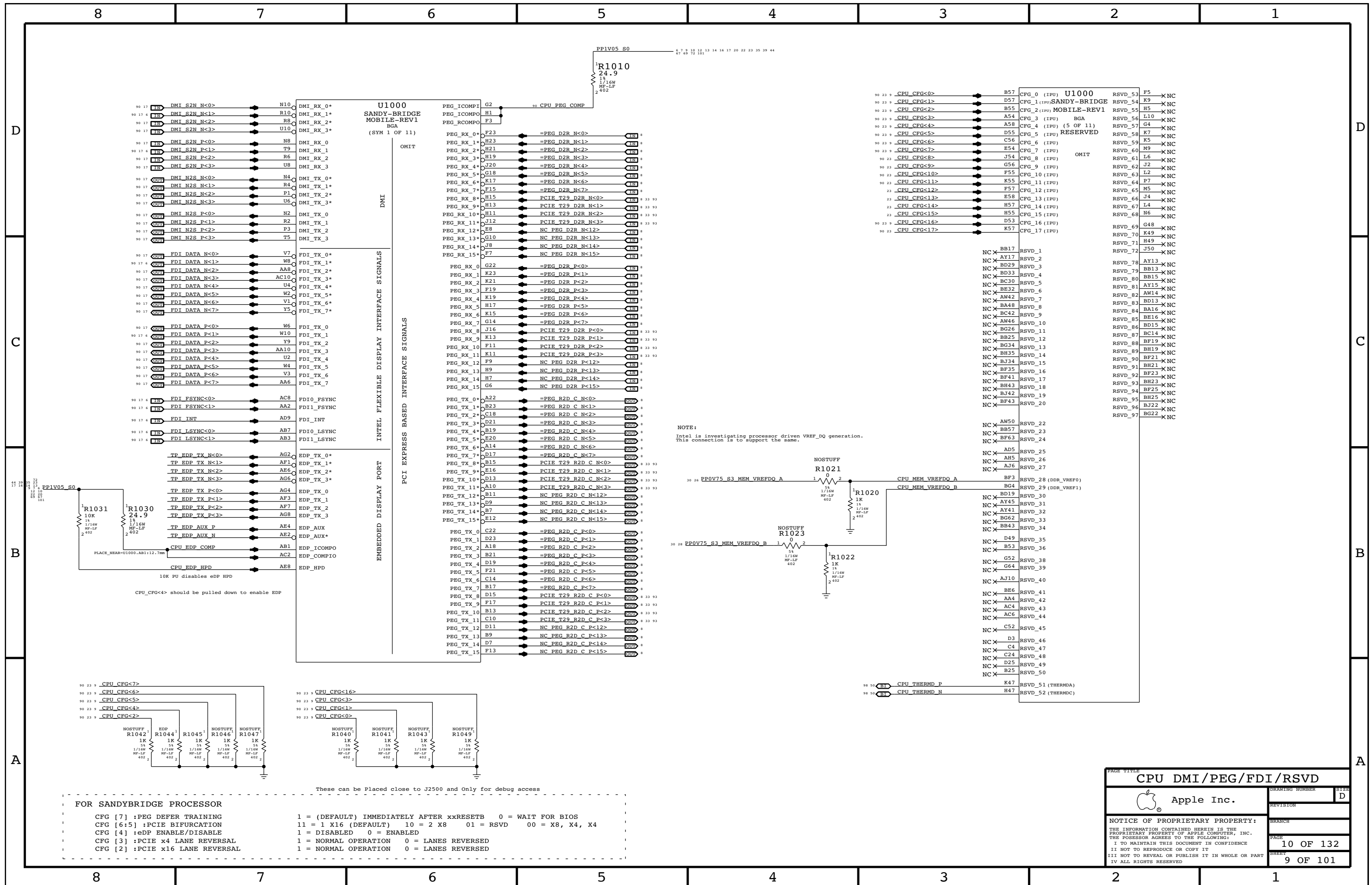


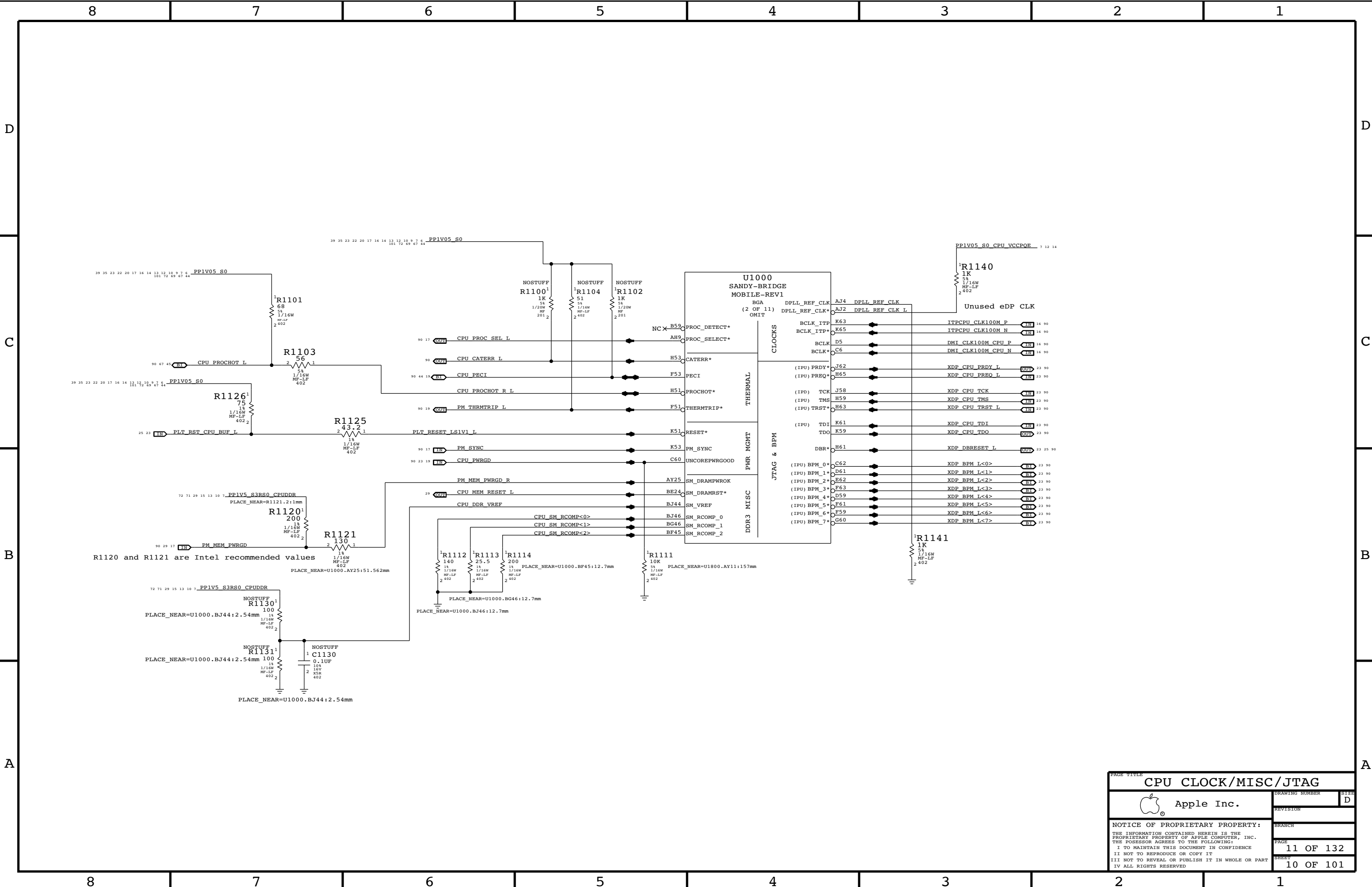




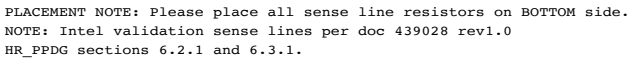


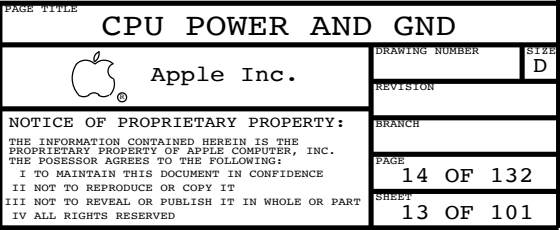






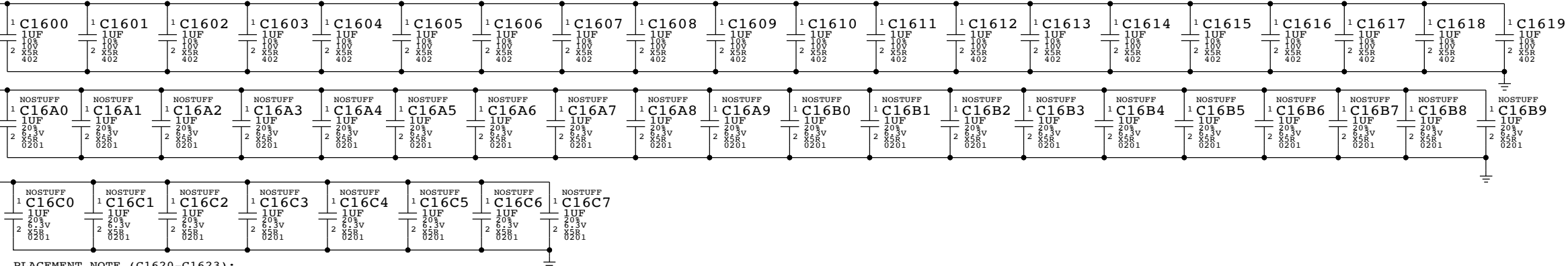




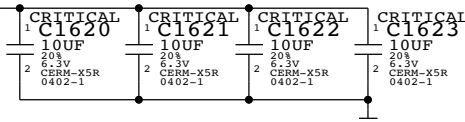


Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

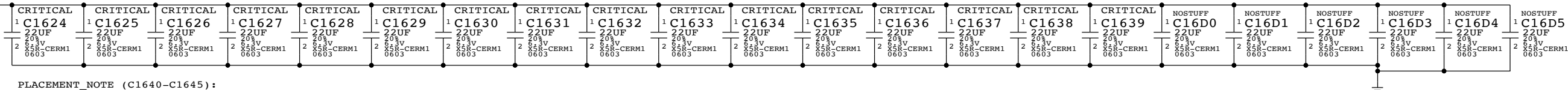
Place on bottom side of U1000



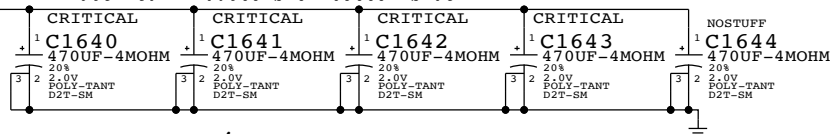
**Place near U1000 on bottom side**



**Place near P inductors on carb bottom inside bottom side.**

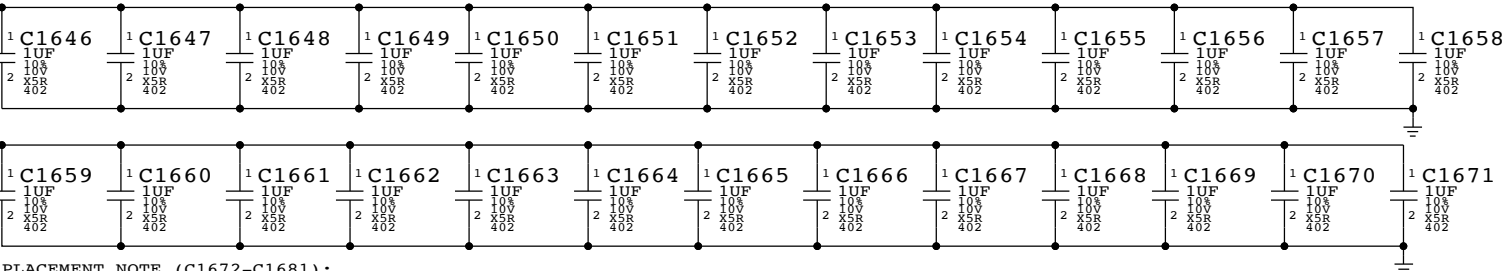


Place near inductors on bottom side.

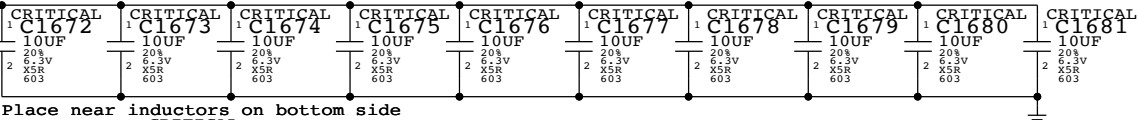


Intel recommendation:	2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation:	2x 330uF, 10x 10uF 0603, 26x 1uF 0402

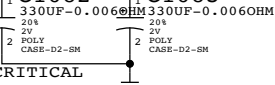
Place on bottom side of U1000



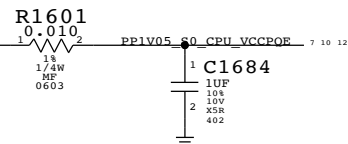
Place near U1000 on bottom side



C1682	CRITICAL C1683
-------	-------------------



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402




**CPU VCCPLL Low pass filter**

Diagram illustrating the CPU VCCPLL Low pass filter circuit. The circuit includes a resistor R1600 (0 Ohms) and two capacitors C1685 (1uF) and C1686 (1uF) in series. A third capacitor C1687 (330uF) is connected in parallel with the output, and a diode D1687 (20V) is connected in parallel with C1687. The output is connected to PE1VR\_S0\_CPU\_VCCPLL\_R. The circuit is labeled as CRITICAL with a tolerance of 330UF-0.0060HM. Placement instructions are provided for the input and output pins.

Input: PLACE\_NEAR=U1000.AK63;2.54 mm:NO\_VIA

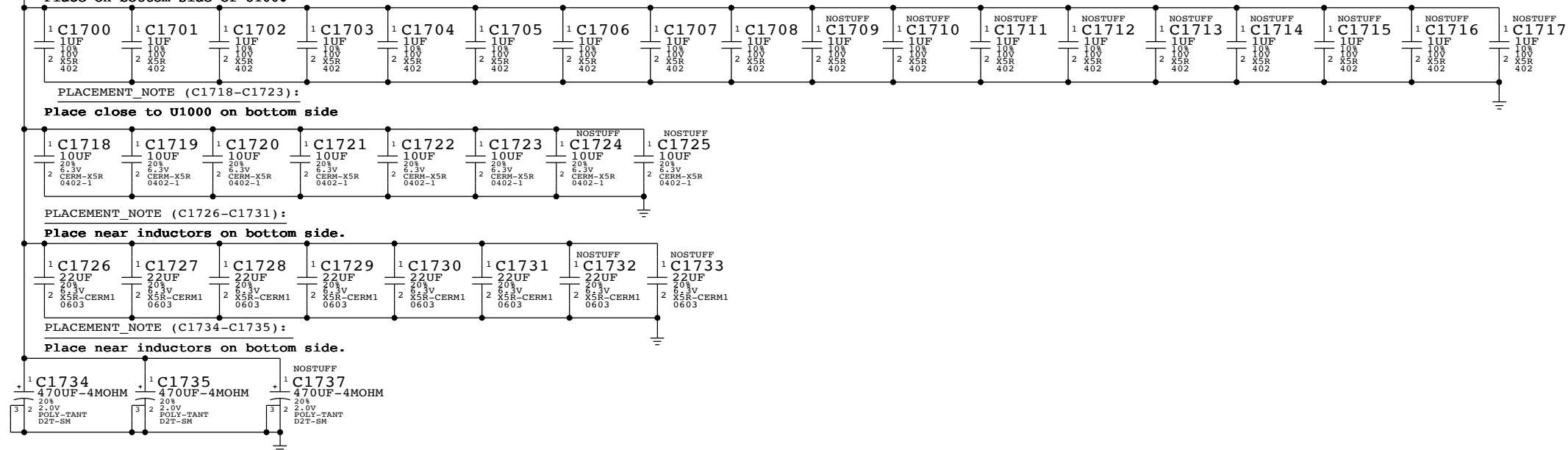
Output: PLACE\_NEAR=U1000.AK65;2.54 mm:NO\_VIA

SYNC MASTER=K92 MLB		SYNC DATE=08/19/201	
PAGE TITLE			
CPU DECOUPLING-I			
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		PAGE	
		16 OF 132	
		SHEET	
		14 OF 101	

Intel recommendation:	2x 470uF	4mOhm,	2x 470uF	4mOhm (NOSTUFF),	6x 22uF	0805,	2x 22uF	0805 (NOSTUFF),	6x 10uF	0603,	2x 10uF	0603 (NOSTUFF),	9x 1uF	0402,	9x 1uF	0402 (NOSTUFF)
Apple Implementation:	2x 470uF	4mOhm,	1x 470uF	4mOhm (NOSTUFF),	6x 22uF	0603,	2x 22uF	0603 (NOSTUFF),	6x 10uF	0402,	2x 10uF	0402 (NOSTUFF),	9x 1uF	0402,	9x 1uF	0402 (NOSTUFF)

Place on bottom side of U1000

Place on bottom side of U1000

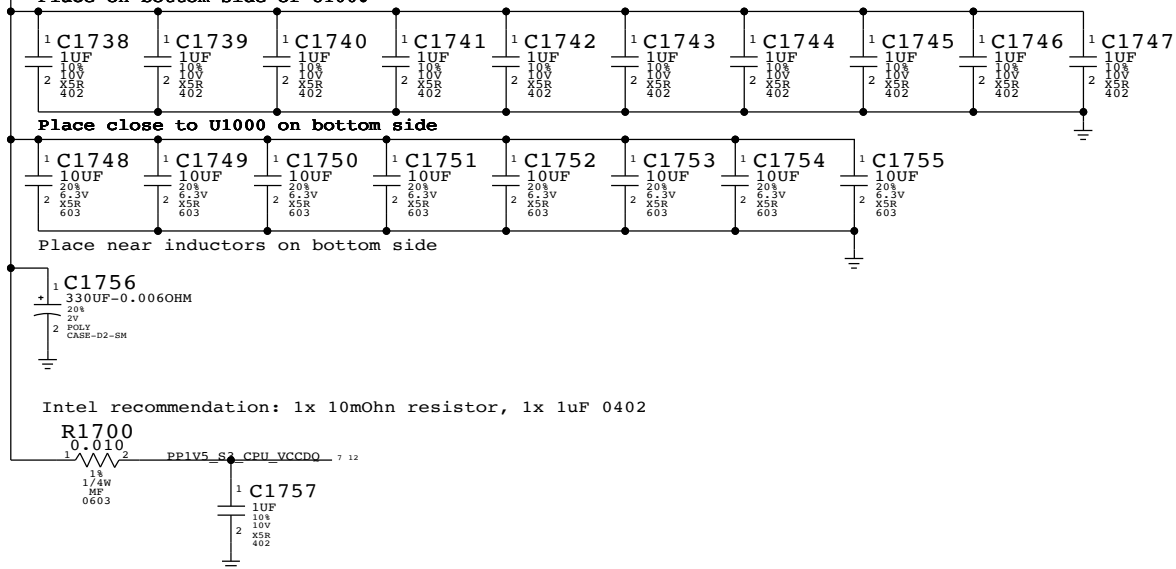


Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402  
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

Place on bottom side of U1000

Place on bottom side of U1000

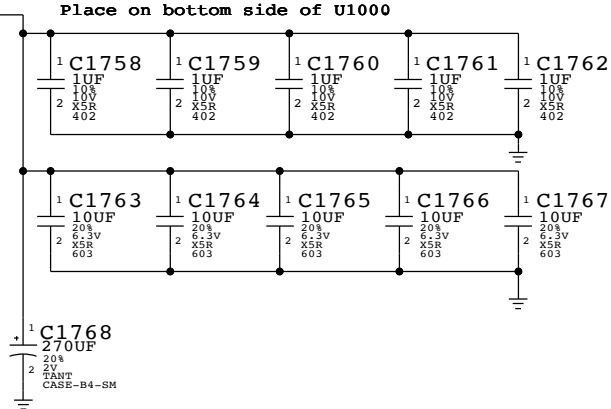
Place on bottom side of U1000

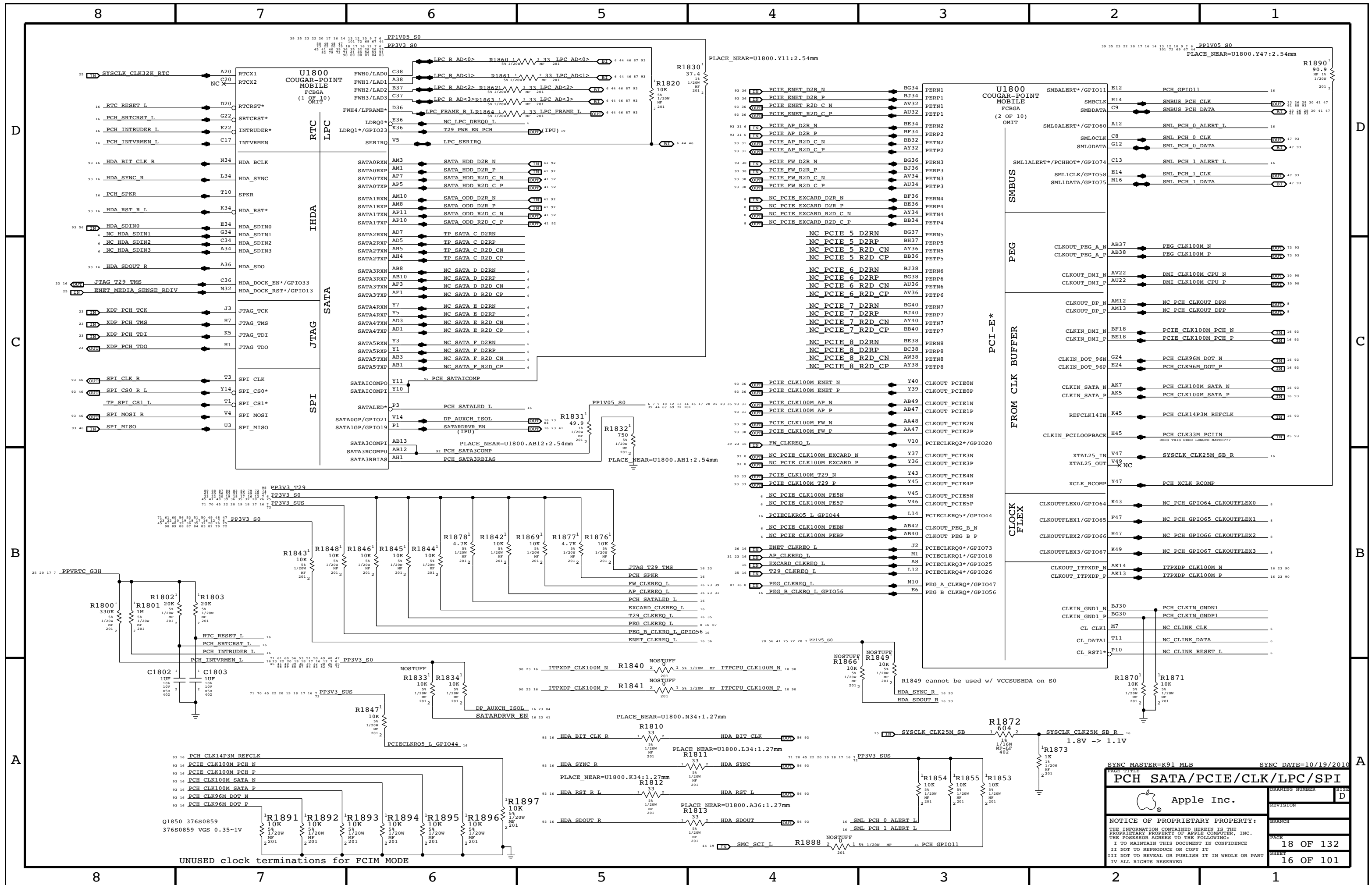


```
Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
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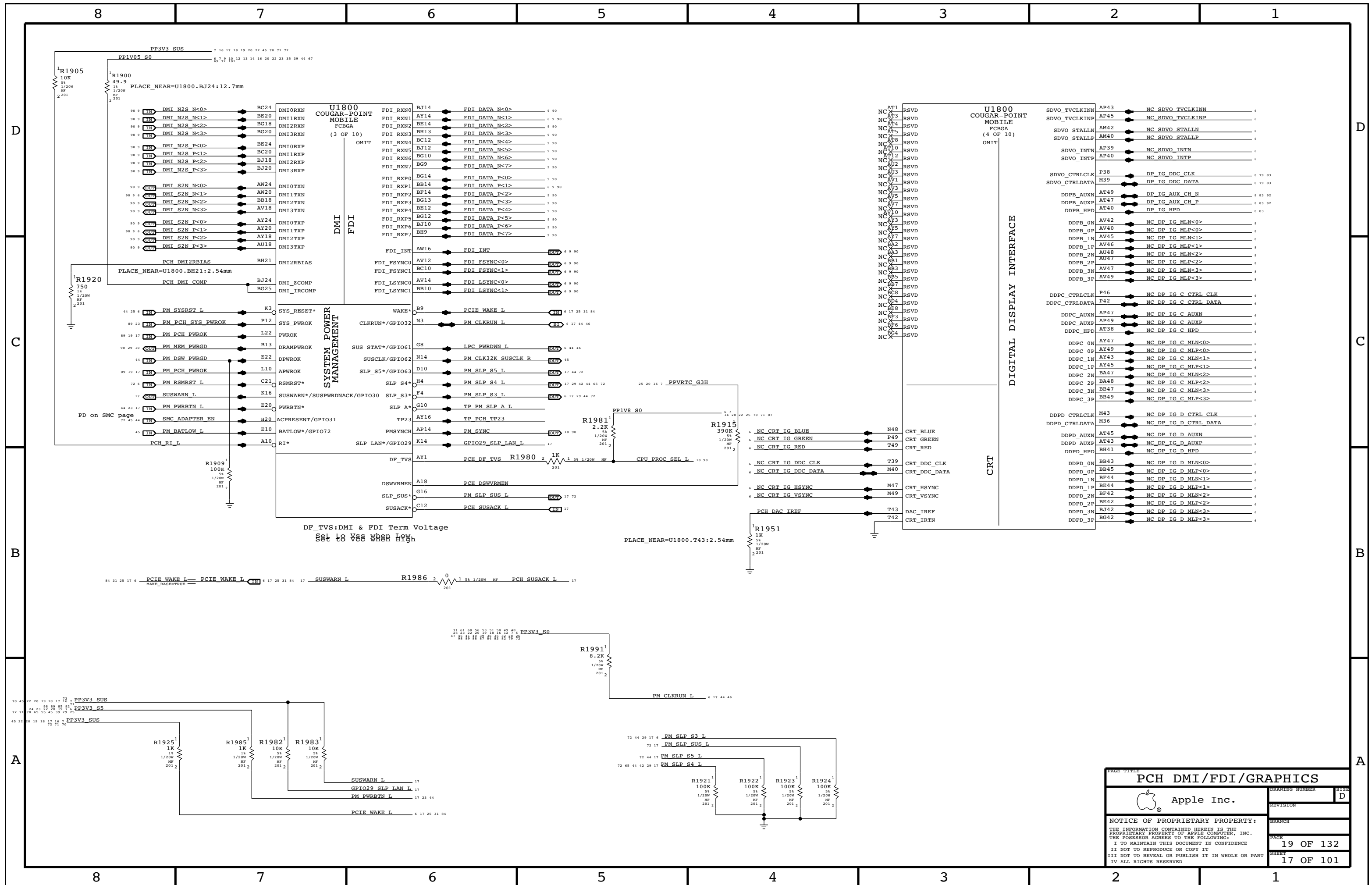
Plot on both sides of 100

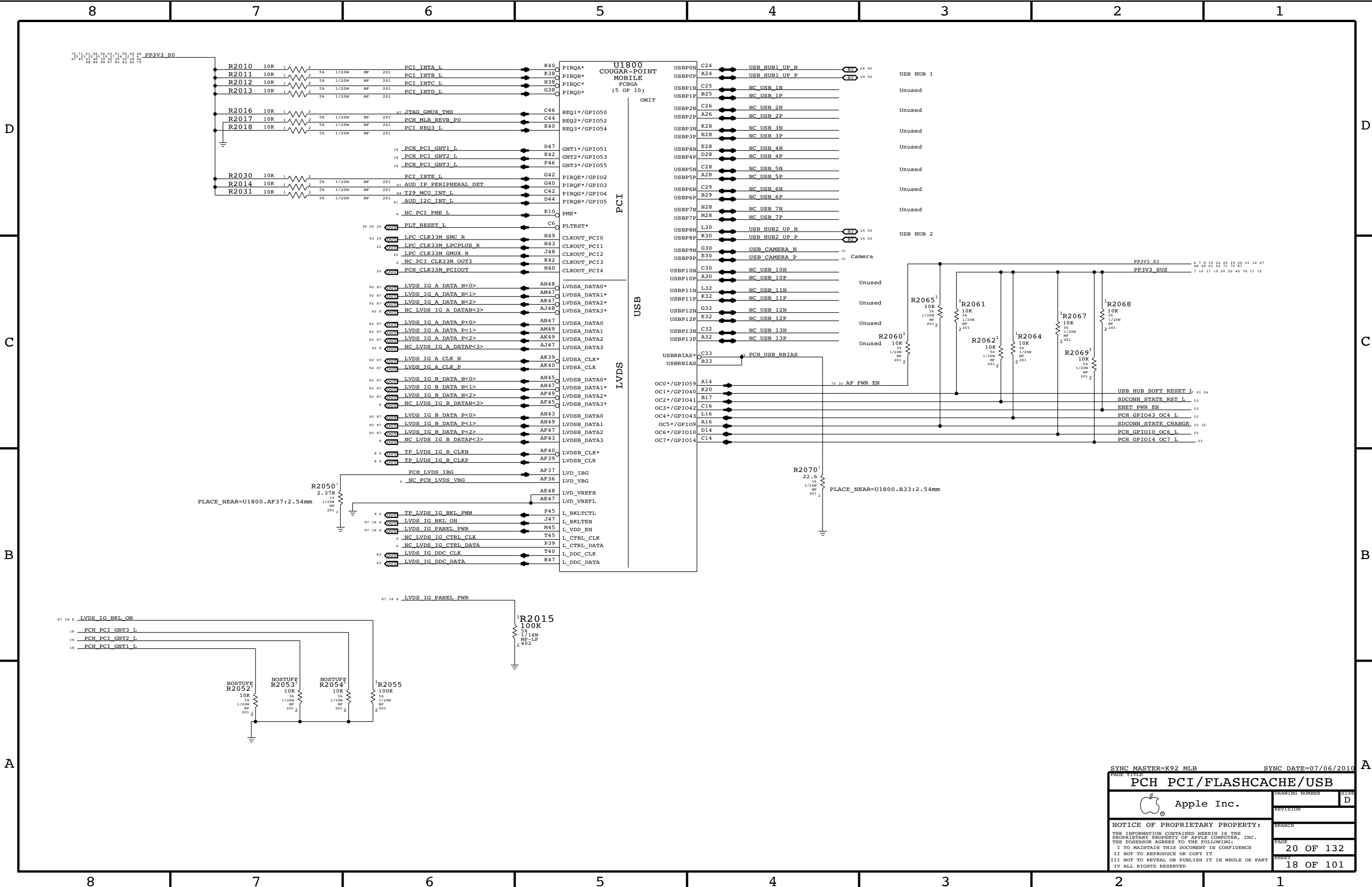
Plot on both sides of x=100

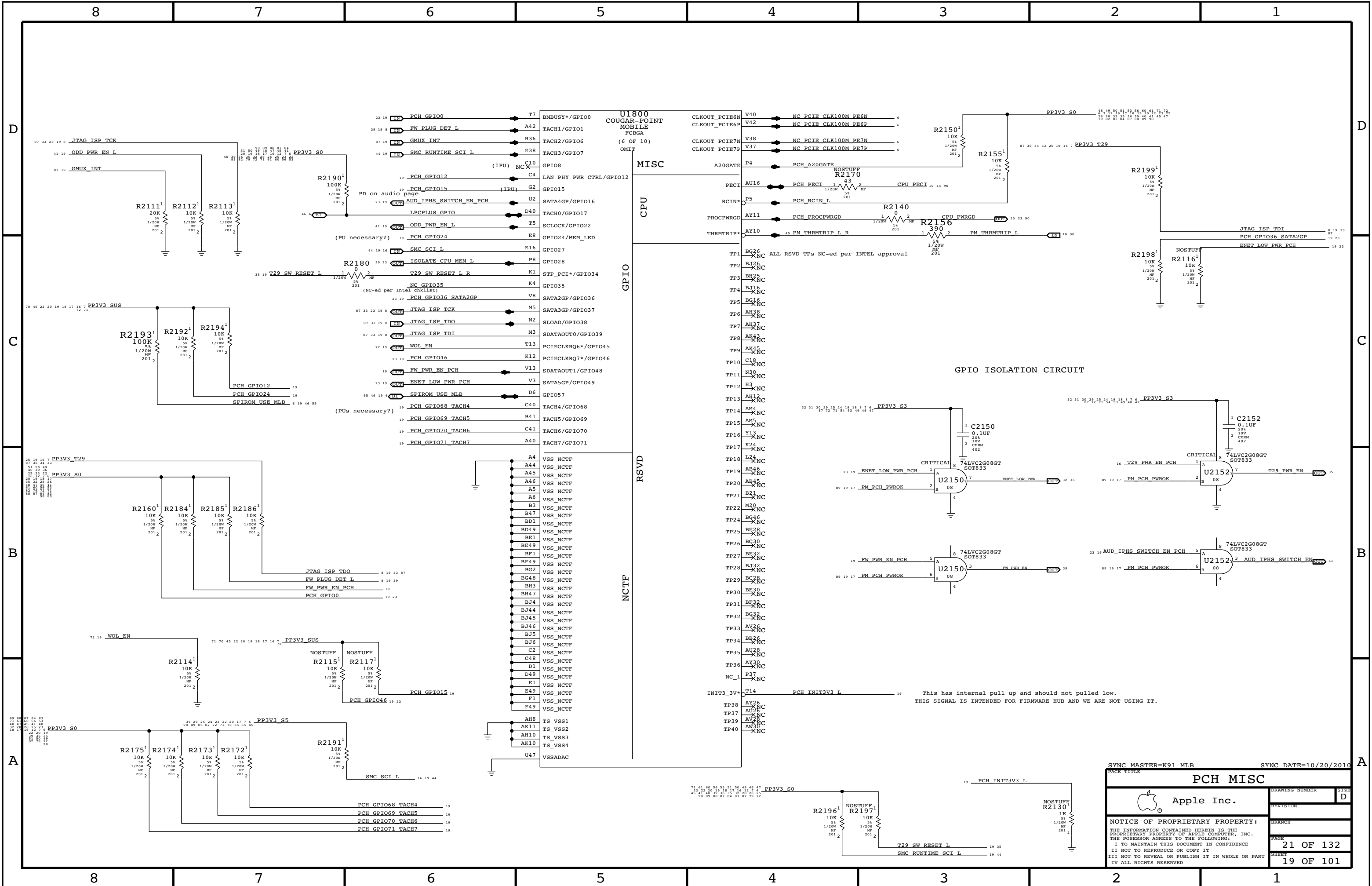














D

C

B

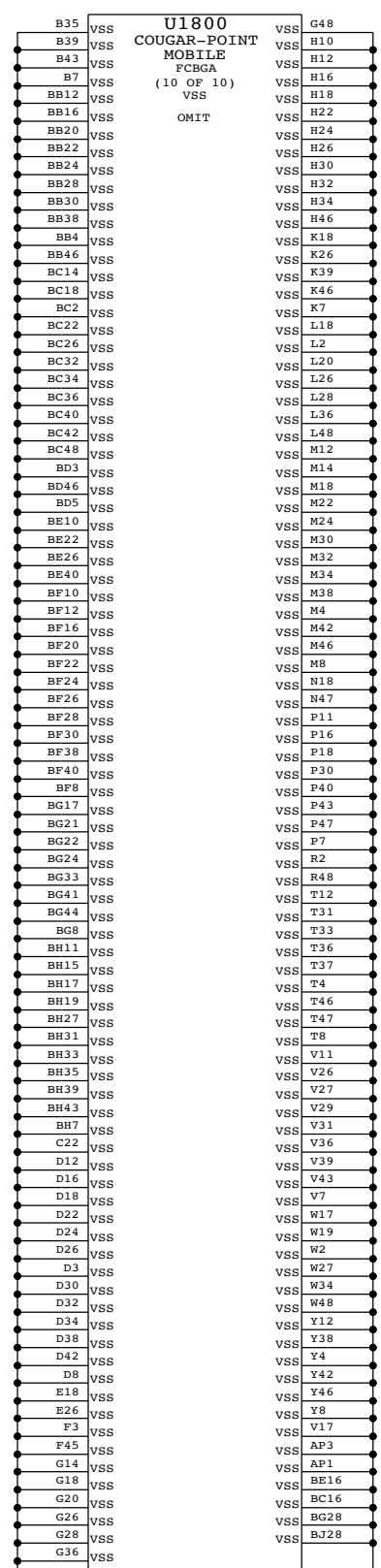
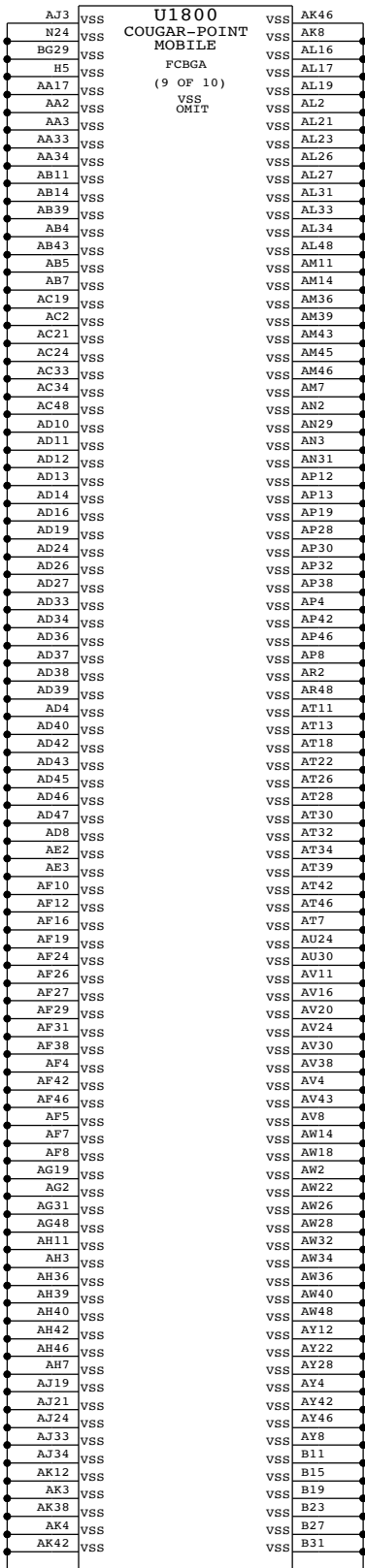
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C


B

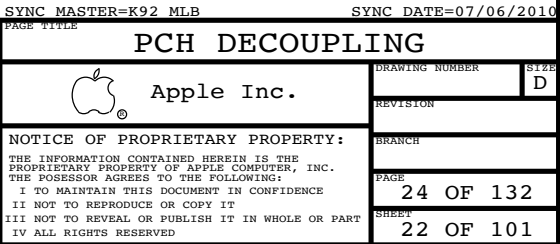
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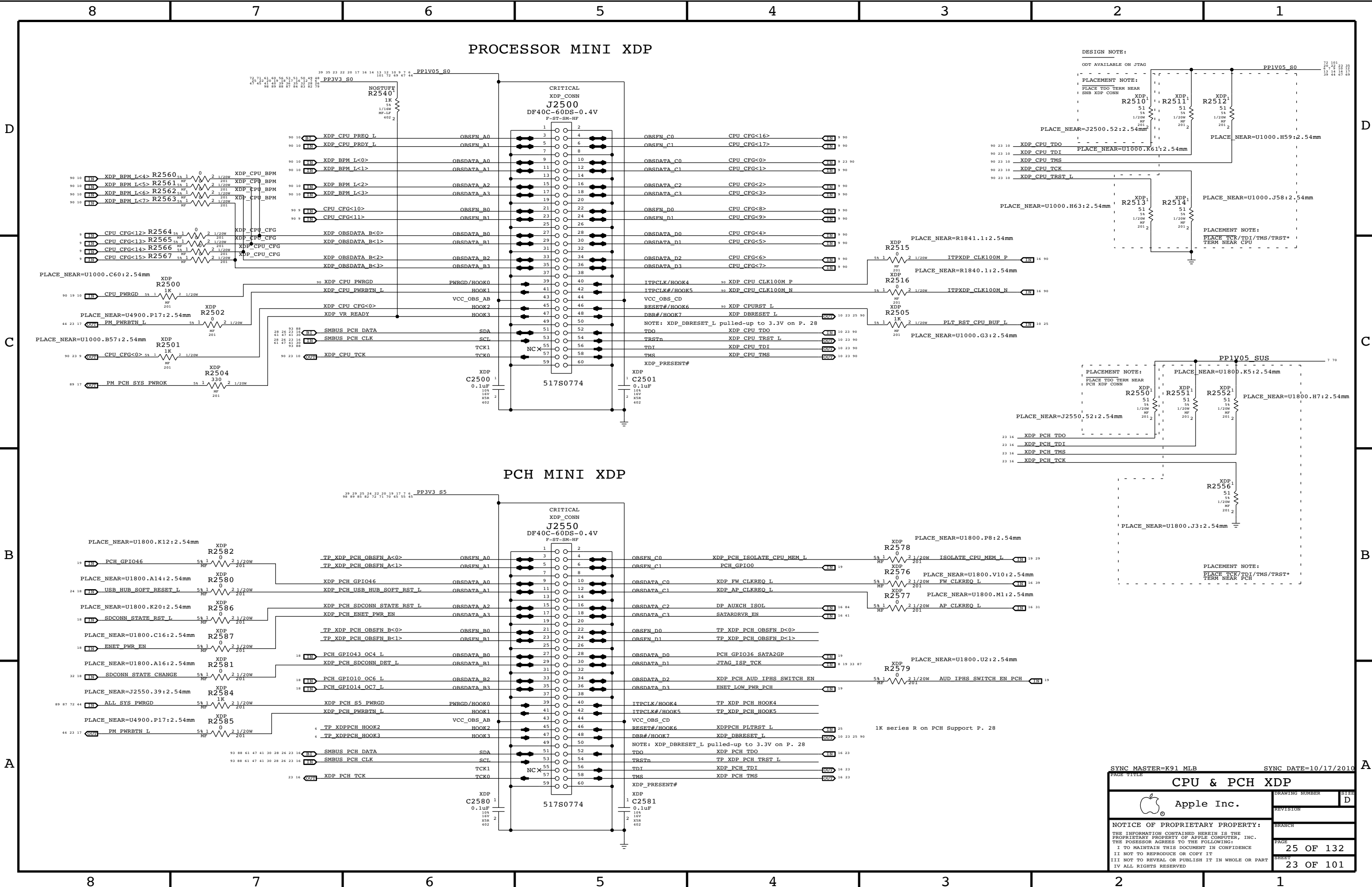


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		BRANCH	
		PAGE	23 OF 132
		SHEET	21 OF 101





DESIGN NOTE:  
ODT AVAILABLE ON JTAG

PLACEMENT NOTE:  
PLACE TDO TERM NEAR  
SMB XDP CONN

PLACE\_NEAR=J2500.52:2.54mm

PLACE\_NEAR=U1000.H59:2.54mm

PLACE\_NEAR=U1000.H63:2.54mm

PLACE\_NEAR=U1000.J58:2.54mm

PLACEMENT NOTE:  
PLACE TCK/TDI/TMS/TRST\*  
TERM NEAR CPU

PLACE\_NEAR=R1841.1:2.54mm

PLACE\_NEAR=R1840.1:2.54mm

PLACE\_NEAR=U1000.G3:2.54mm

PLACE\_NEAR=U1800.K5:2.54mm

PLACE\_NEAR=U1800.H7:2.54mm

PLACE\_NEAR=J2550.52:2.54mm

PLACE\_NEAR=U1800.J3:2.54mm

PLACE\_NEAR=U1800.P8:2.54mm

PLACE\_NEAR=U1800.V10:2.54mm

PLACE\_NEAR=U1800.M1:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PLACEMENT NOTE:  
PLACE TCK/TDI/TMS/TRST\*  
TERM NEAR PCH

PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

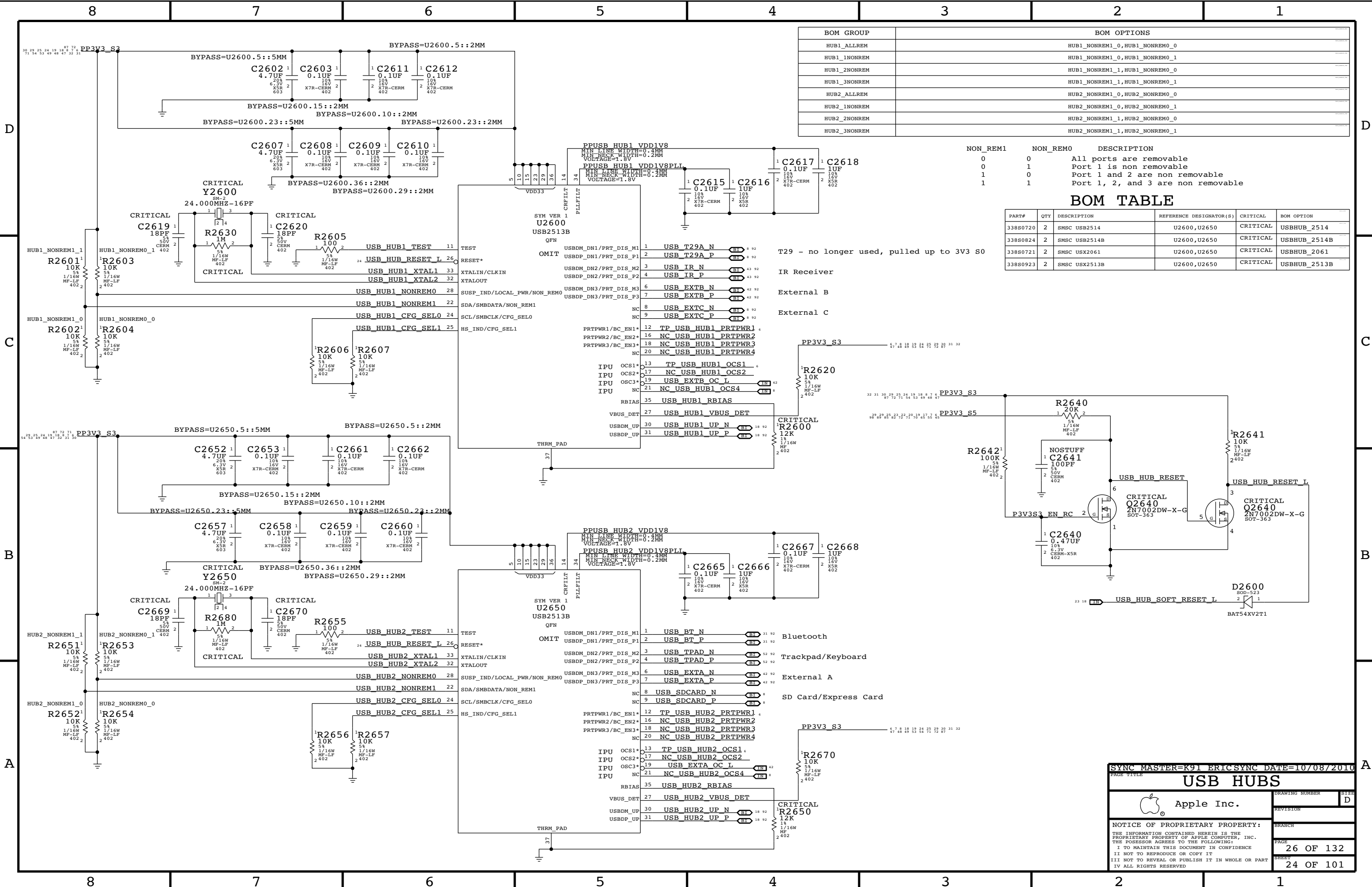
PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PLACE\_NEAR=U1800.U2:2.54mm

PAGE TITLE		SYNC MASTER=K91 MLB		SYNC DATE=10/17/2010	
CPU & PCH XDP		DRAWING NUMBER		SIZE	
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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

T29 - no longer used, pulled up to 3V3 S0

IR Receiver

External B

External C

Bluetooth

Trackpad/Keyboard

External A

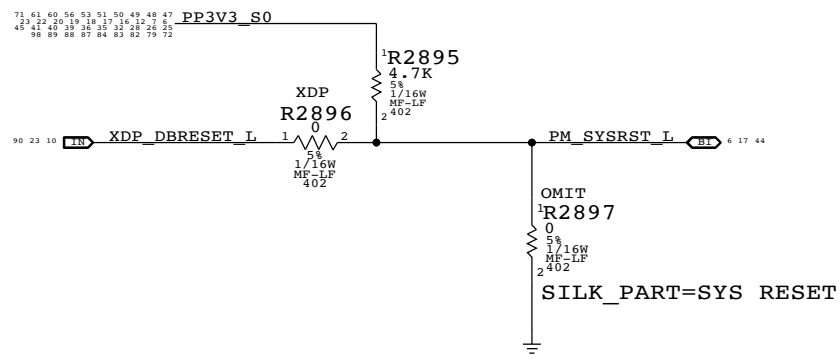
SD Card/Express Card

SYNC MASTER=K91 ERIC SYNC DATE=10/08/2010

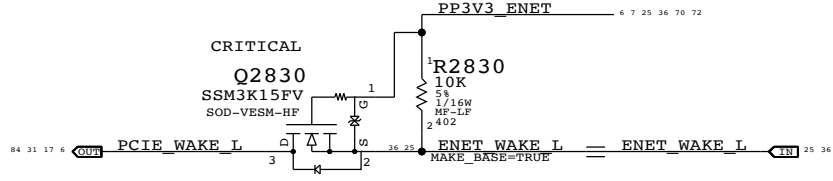
PAGE TITLE		
USB HUBS		
	DRAWING NUMBER	SIZE D
	REVISION	
	BRANCH	
	PAGE	26 OF 132
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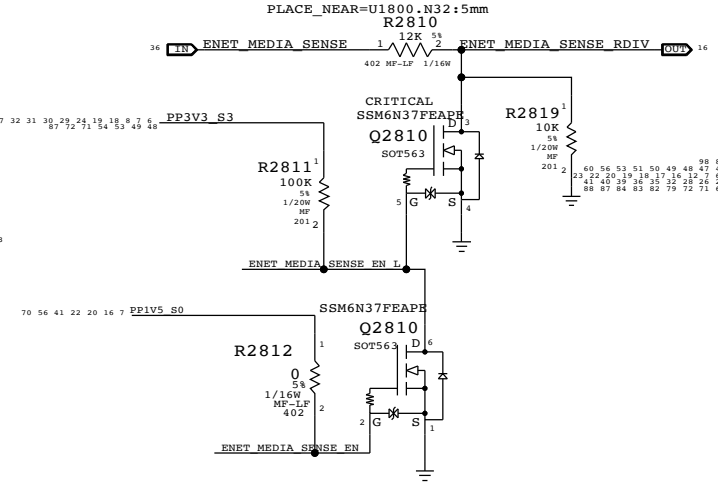
PCH Reset Button



Ethernet WAKE# Isolation

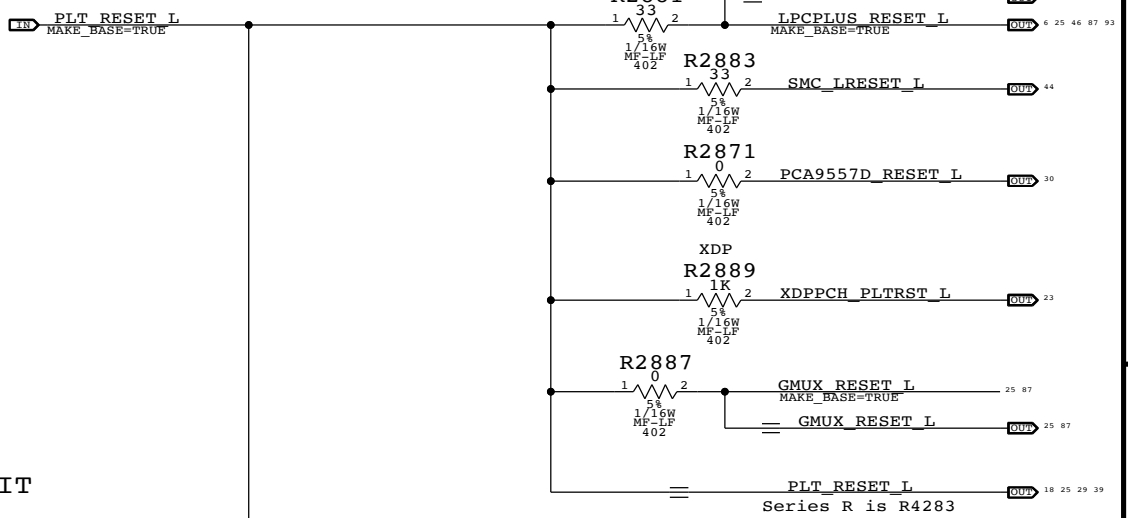


ENET\_MEDIA\_SENSE ISOLATION CIRCUIT



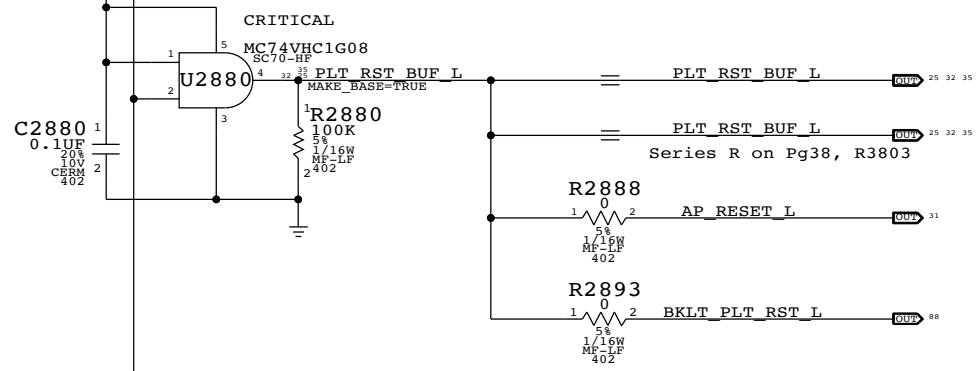
Platform Reset Connections

Unbuffered



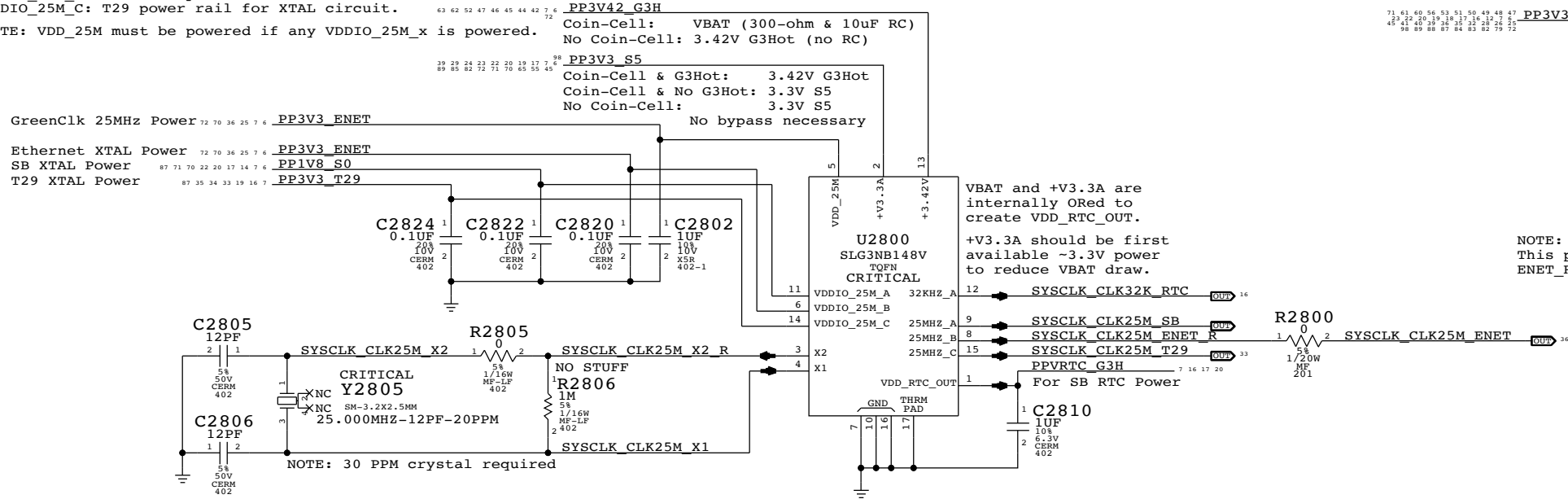
Buffered

Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.

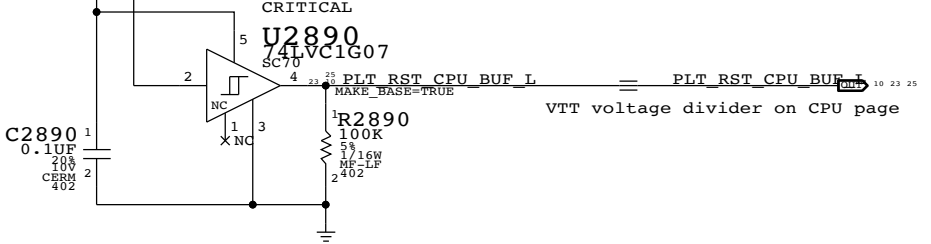


System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO\_25M\_A: SB power rail for XTAL circuit.  
VDDIO\_25M\_B: Ethernet power rail for XTAL circuit.  
VDDIO\_25M\_C: T29 power rail for XTAL circuit.  
NOTE: VDD\_25M must be powered if any VDDIO\_25M\_x is powered.



Buffered CPU reset



NOTE:  
This page is different for K92.  
ENET\_RESET\_L hooked up differently on both the projects.

SYNC MASTER=K92 MLB		SYNC DATE=07/06/2010	
PAGE TITLE		Chipset Support	
Apple Inc.		DRAWING NUMBER	SIZE D
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		PAGE	28 OF 132
		SHEET	25 OF 101





## Page Notes

Power aliases required by this page:

```
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V
```

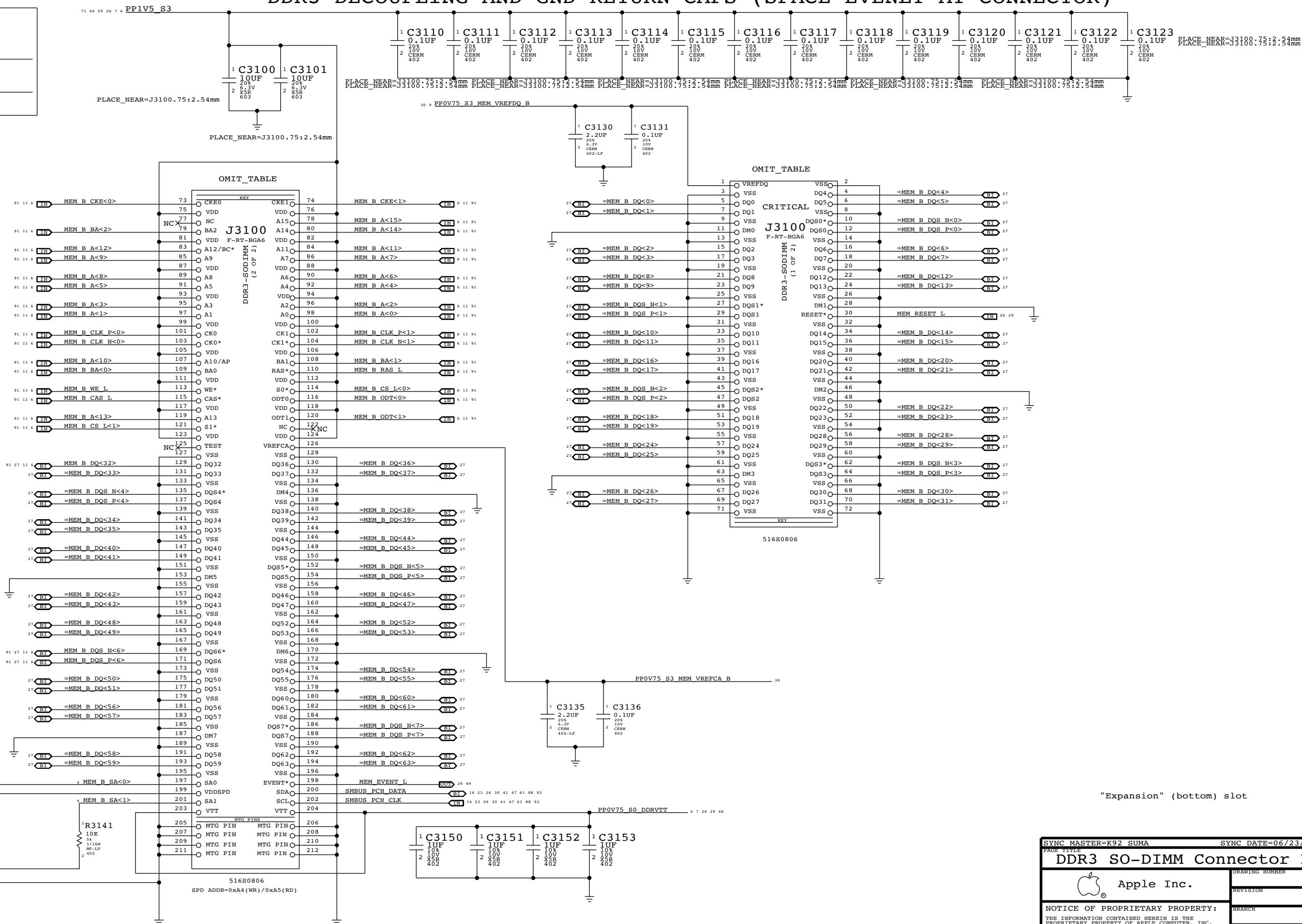
Signal aliases required by this page:

```
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
```


ROM options provided by this page:

(NONE)

## DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



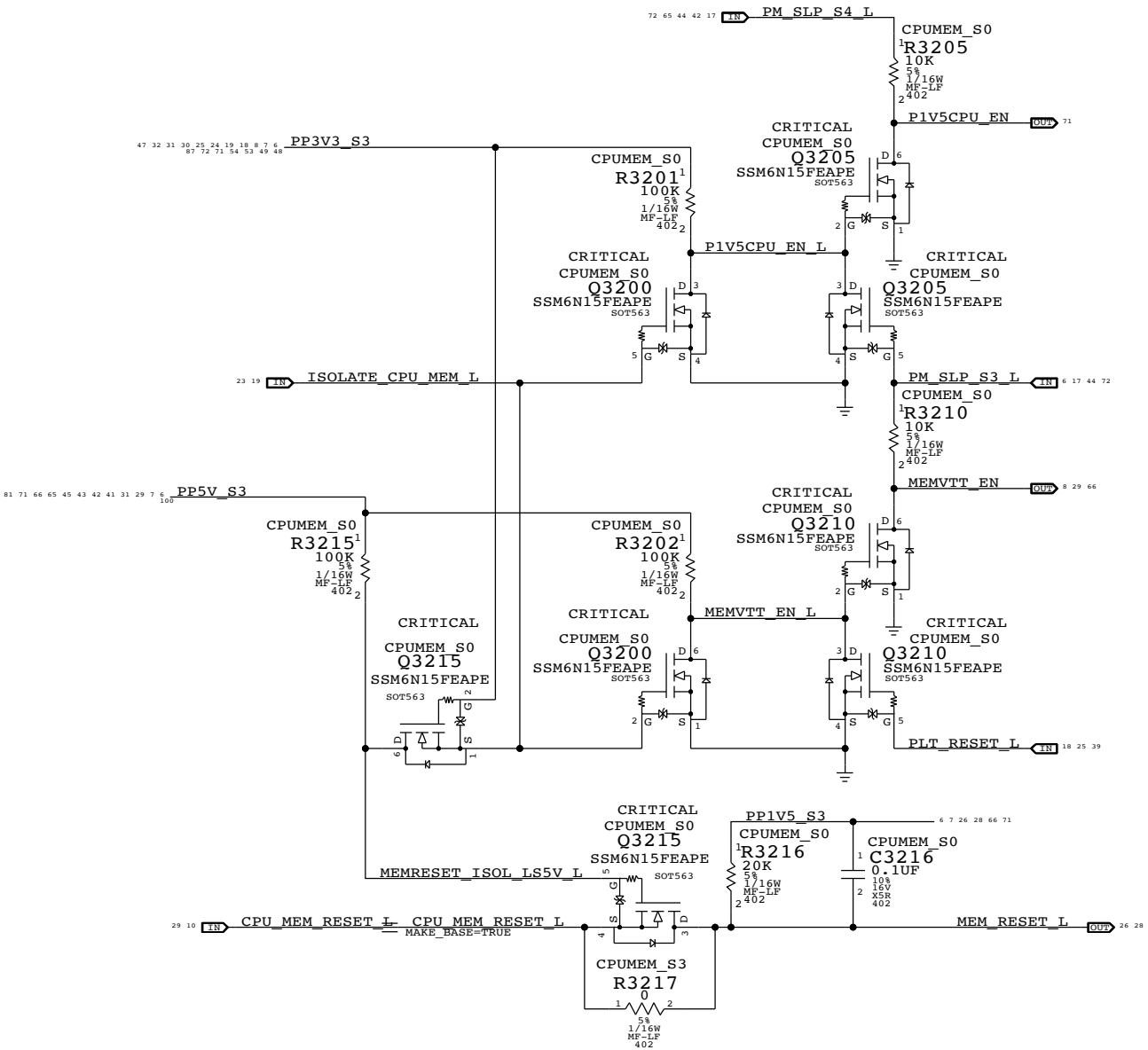
"Expansion" (bottom) slot

SYNCH MASTER-K92 SUMA		SYNCH DATE=06/23/2010	
PAGE TITLE			
DDR3 SO-DIMM Connector B			
 Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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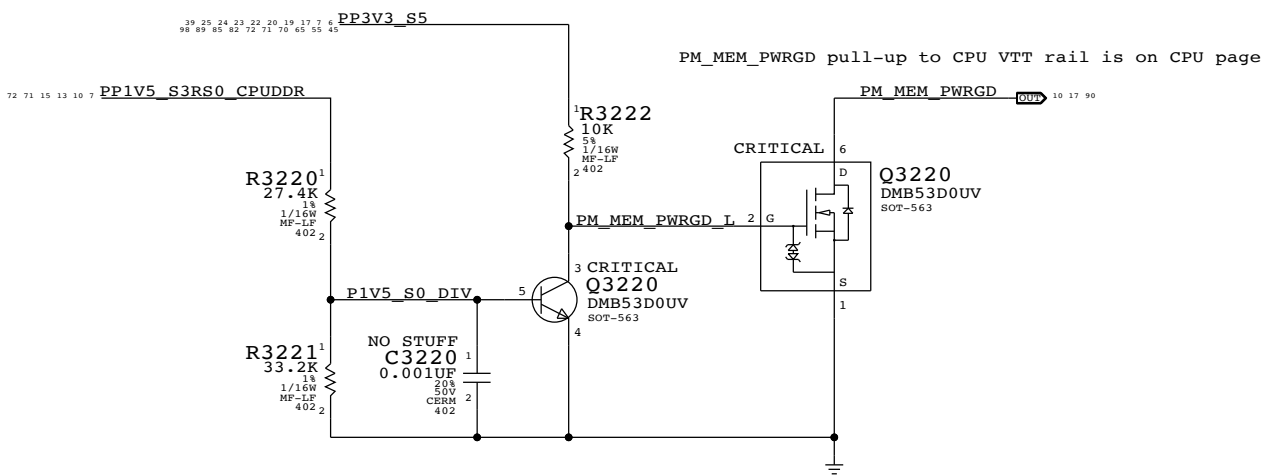
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3->S0 transitions determines behavior of signals.  
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.  
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

P1V5CPU\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) \* PM\_SLP\_S4\_L  
MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) \* PM\_SLP\_S3\_L  
MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L

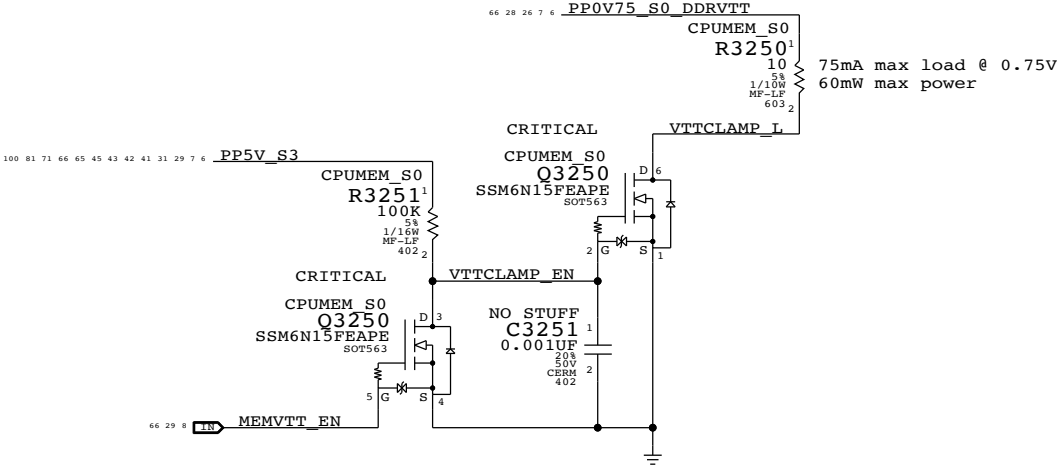


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.

SYNC MASTER=K18 MLB

SYNC DATE=04/27/2010

CPU Memory S3 Support

Apple Inc.

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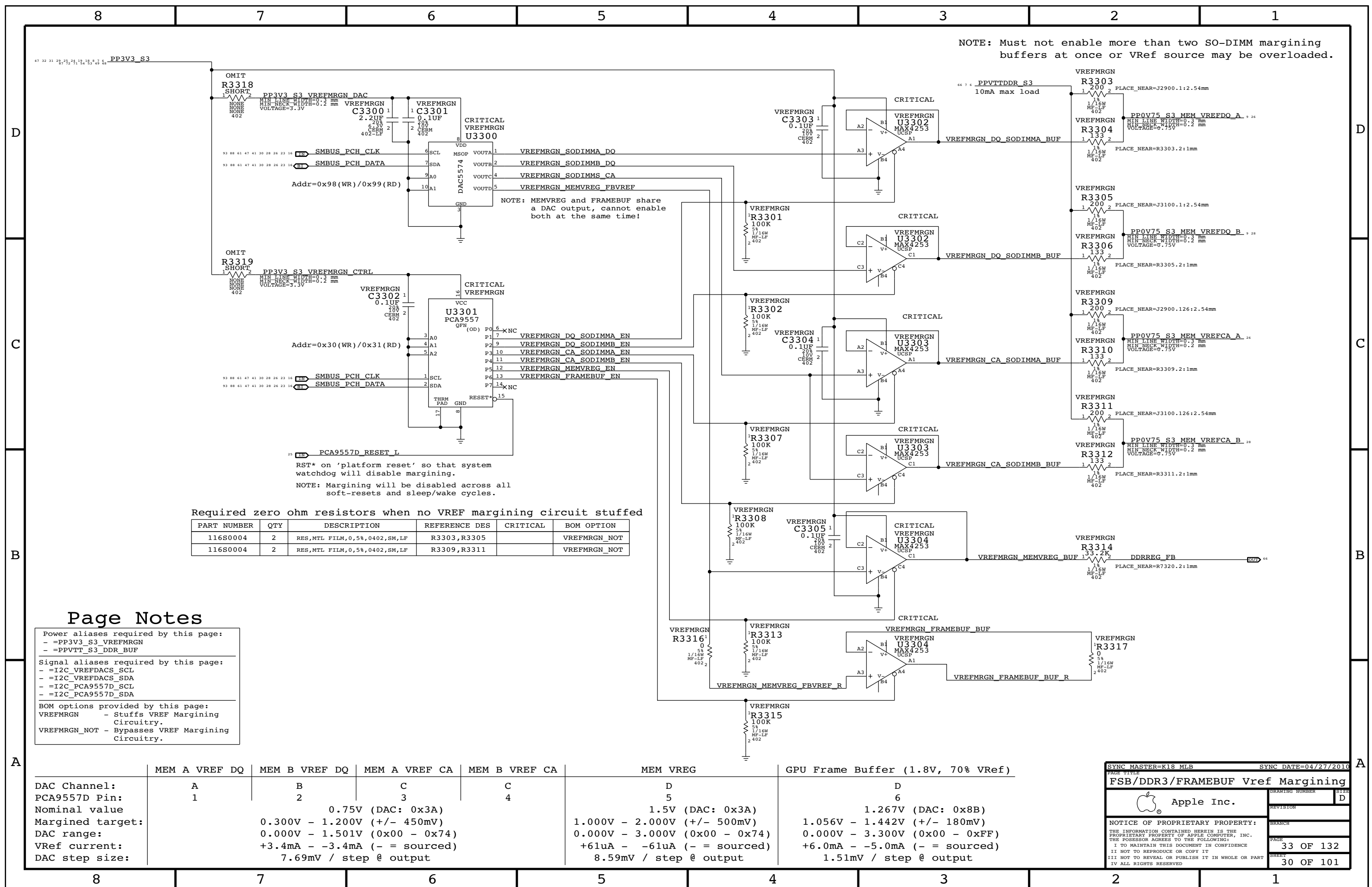
SHEET

SIZE

D

32 OF 132

29 OF 101





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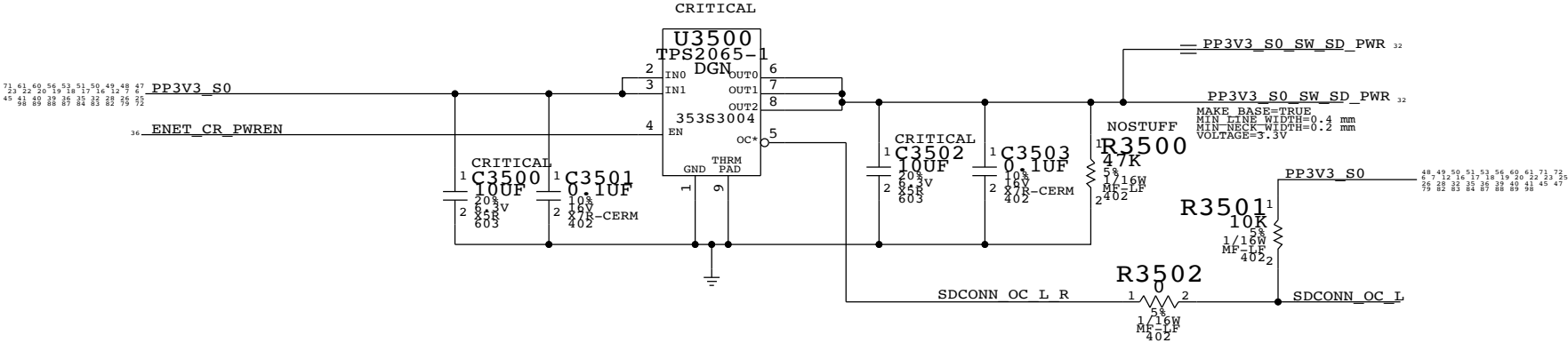
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A

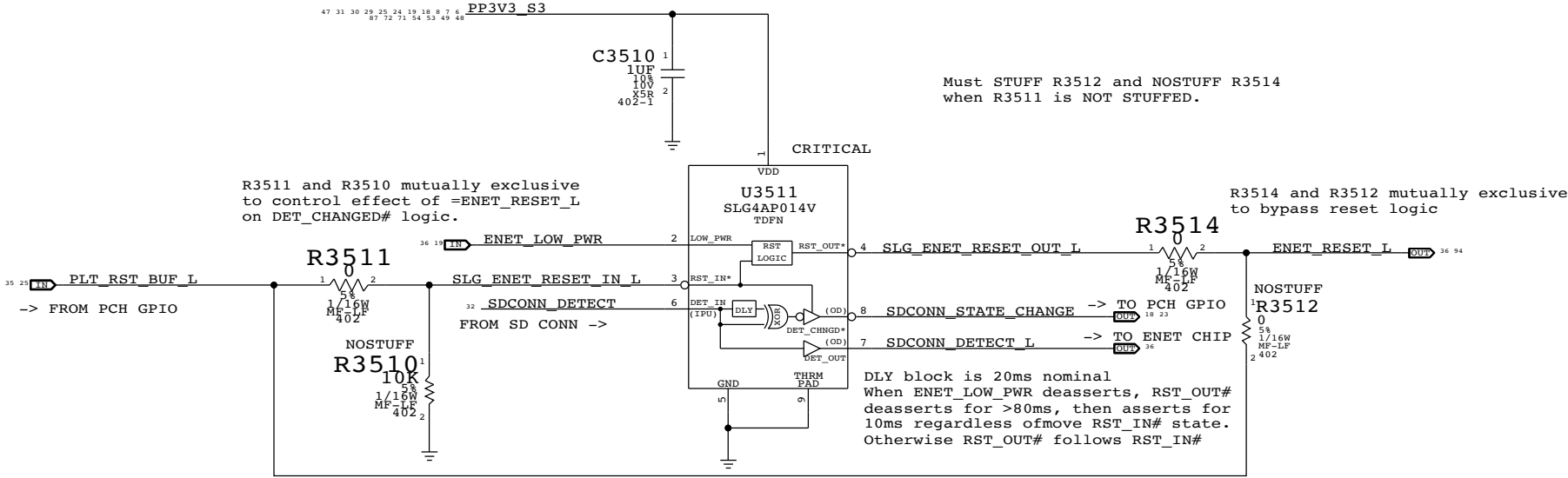
A

SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

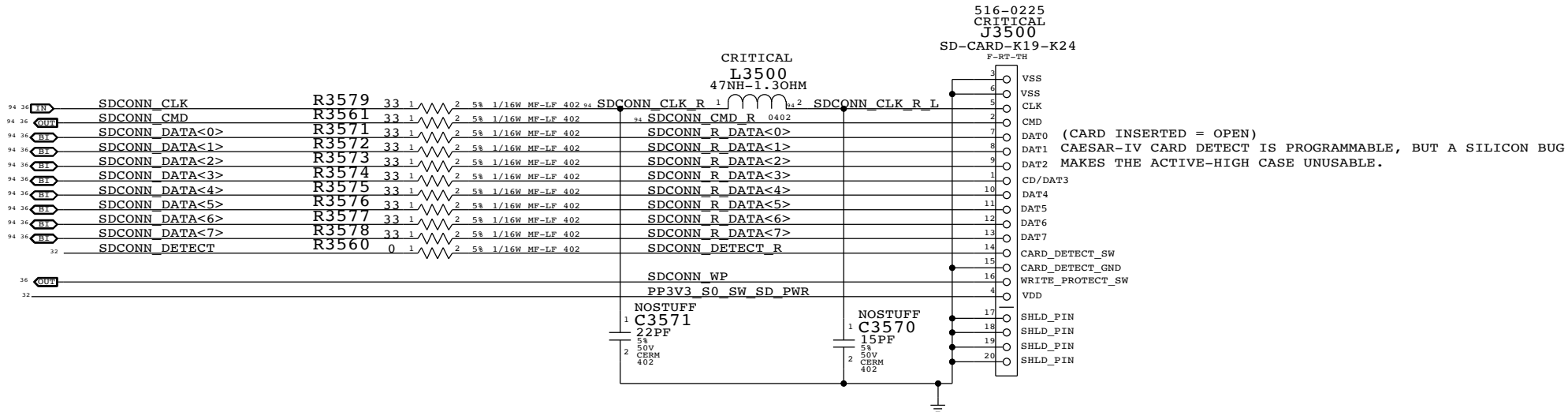
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO LATCH CIRCUIT



SD CARD CONNECTOR



SYNC MASTER=K91 ERIC SYNC DATE=10/08/2010

SD READER CONNECTOR

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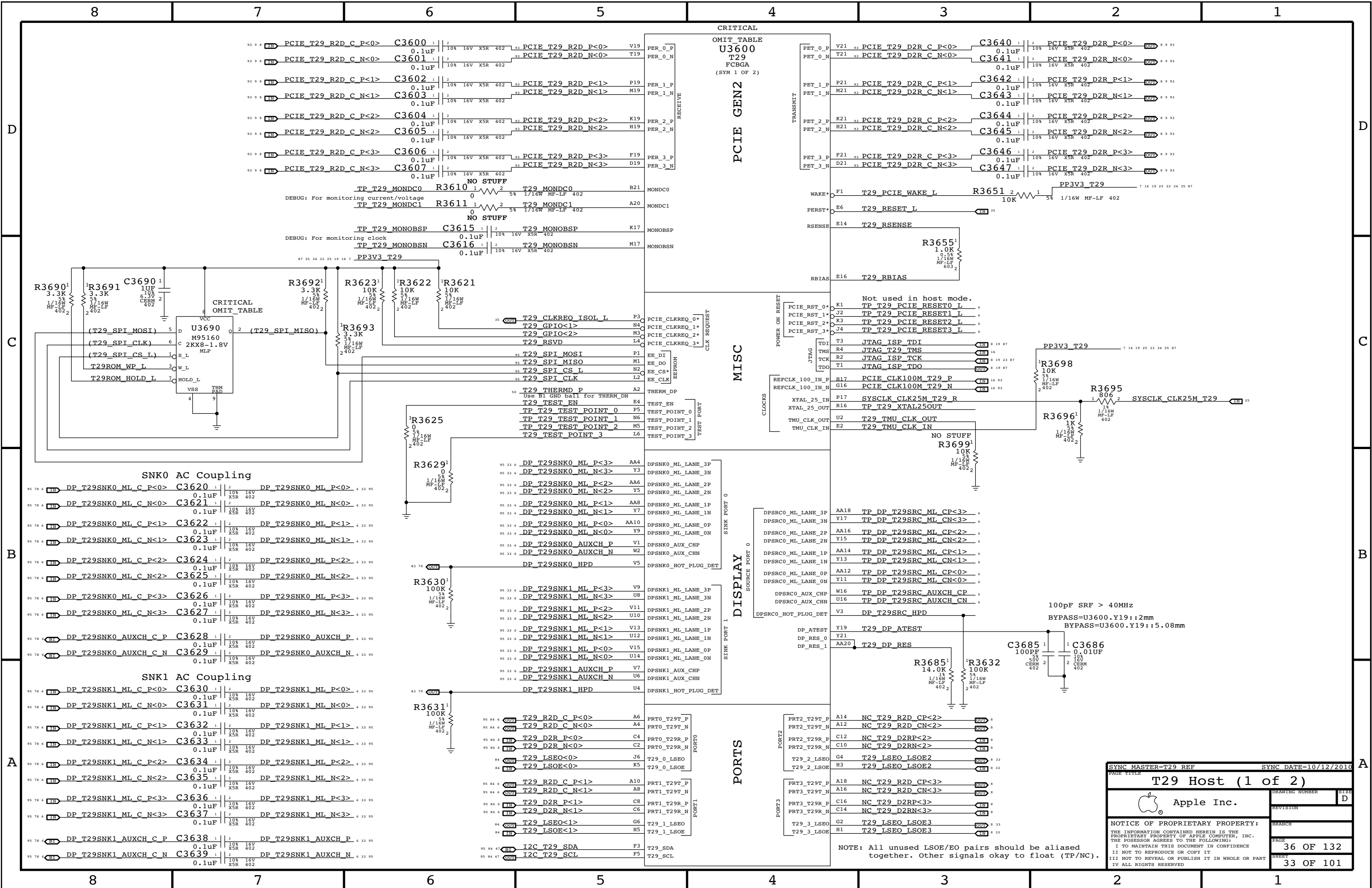
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SHEET

35 OF 132

32 OF 101





D

C

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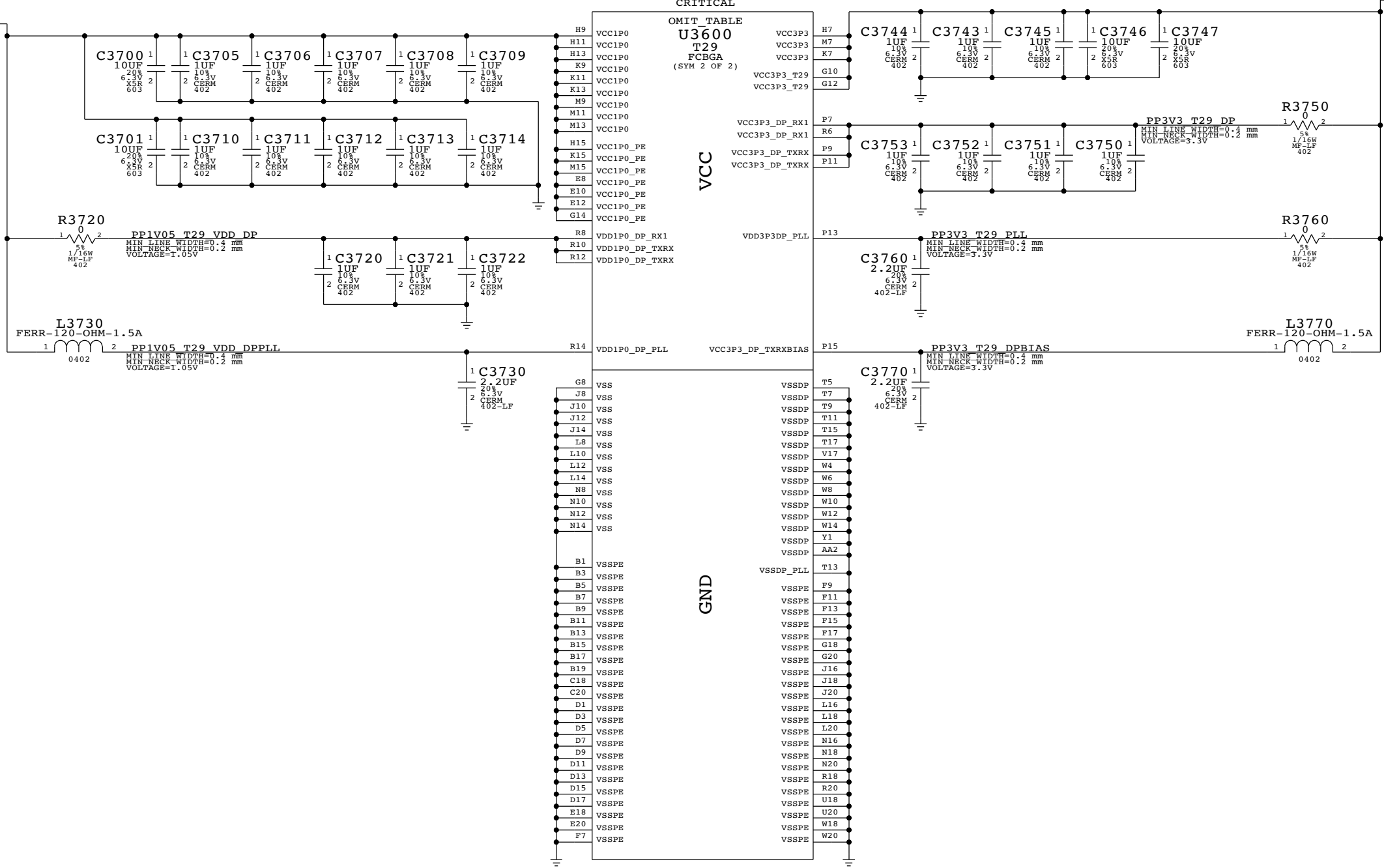
A

8 7 6 5 4 3 2 1

35 7 PP1V05 T29  
2100 mA (Single Port)  
2250 mA (Dual Port)  
EDP: 3000 mA

PP3V3 T29 7 16 19 25 33 35 87  
135 mA (Single-Port)  
152 mA (Dual-Port)  
EDP: 200 mA

0-ohms are placeholders for now, replace with proper values after characterization.



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

8 7 6 5 4 3 2 1

SYNC MASTER=T29 REF		SYNC DATE=10/12/2010	
PAGE TITLE			
T29 Host (2 of 2)			
Apple Inc.		DRAWING NUMBER	SIZE
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8	7	6	5	4	3	2	1
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## 16 1

## A



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16 1

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8	7	6	5	4	3	2	1
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## D



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16 1

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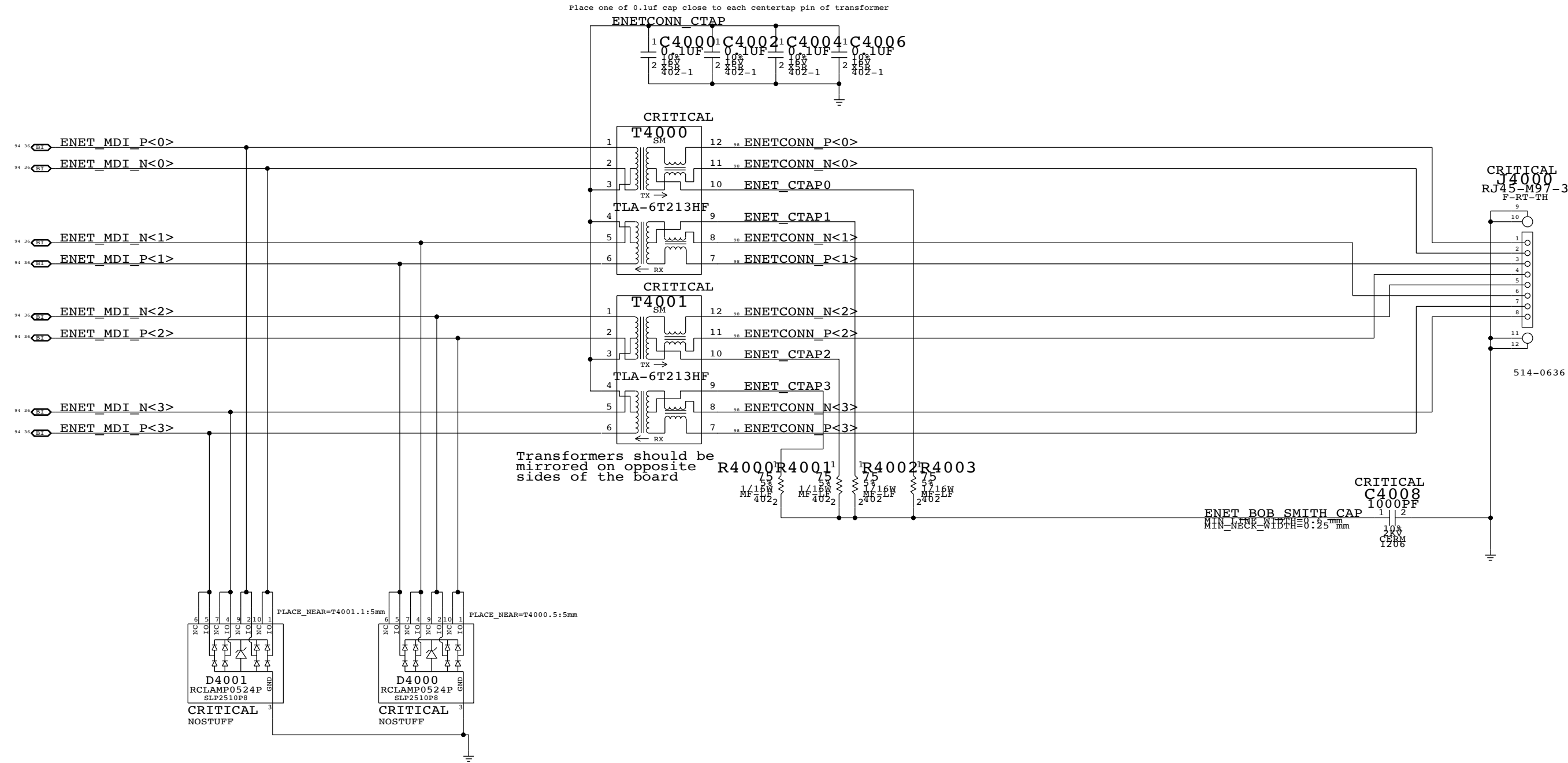


Page Notes

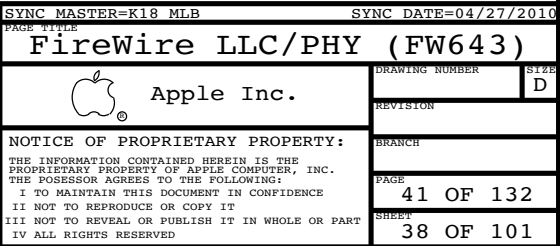
Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



PAGE TITLE		PAGE TITLE	
Ethernet Connector		Ethernet Connector	
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REVISION		REVISION	
BRANCH		BRANCH	
PAGE		PAGE	
40 OF 132		40 OF 132	
SHEET		SHEET	
37 OF 101		37 OF 101	



Page Notes

Power aliases required by this page:

- PPBUS\_S5\_FWPWRSW (FW VP FET Input)
- PPBUS\_FW\_FET (FW VP FET Output)
- PP3V3\_FW\_P3V3FWFET (3.3V FET Input)
- PP3V3\_FW\_FET (3.3V FET Output)
- PP3V3\_FW\_FWPHY (PHY 3.3V Power)
- PP3V3\_S0\_FWLATEVG
- PP3V3\_S0\_FWPWRCTL
- PP1V05\_S0\_FWPWRCTL (5KPD Bias Rail)
- PP1V05\_FW\_P1V0FWFET (1.0V FET Input)
- PP1V0\_FW\_FET\_R (1.0V FET Output)
- PP1V0\_FW\_FWPHY (PHY 1.0V)

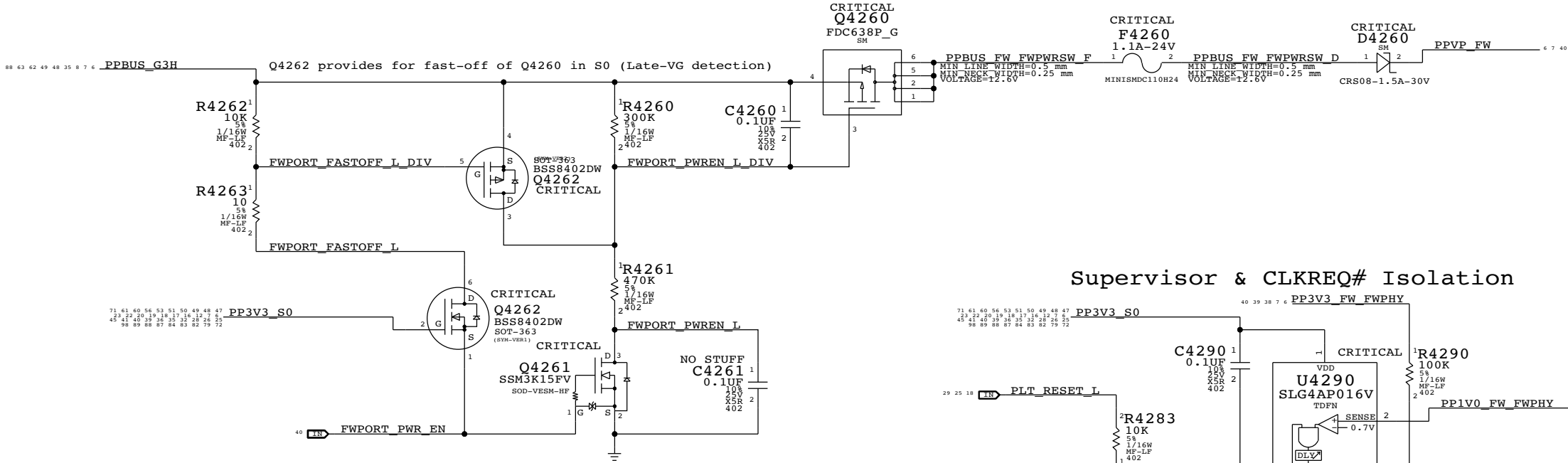
Signal aliases required by this page:

- FW\_CLKREQ\_L
- FW\_PME\_L

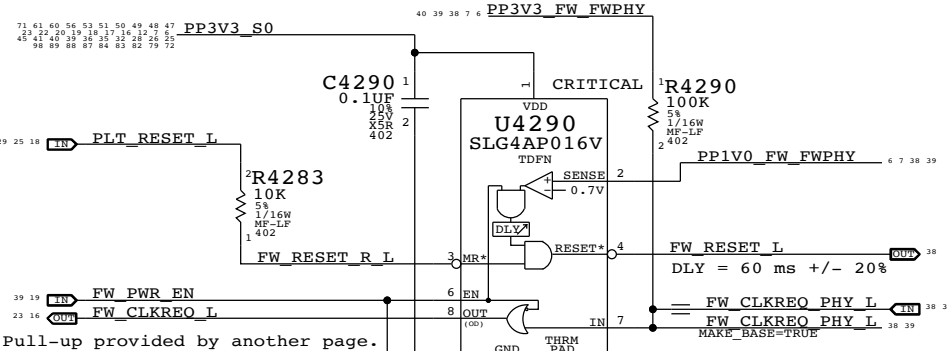
BOM options provided by this page:

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FireWire Port Power Switch

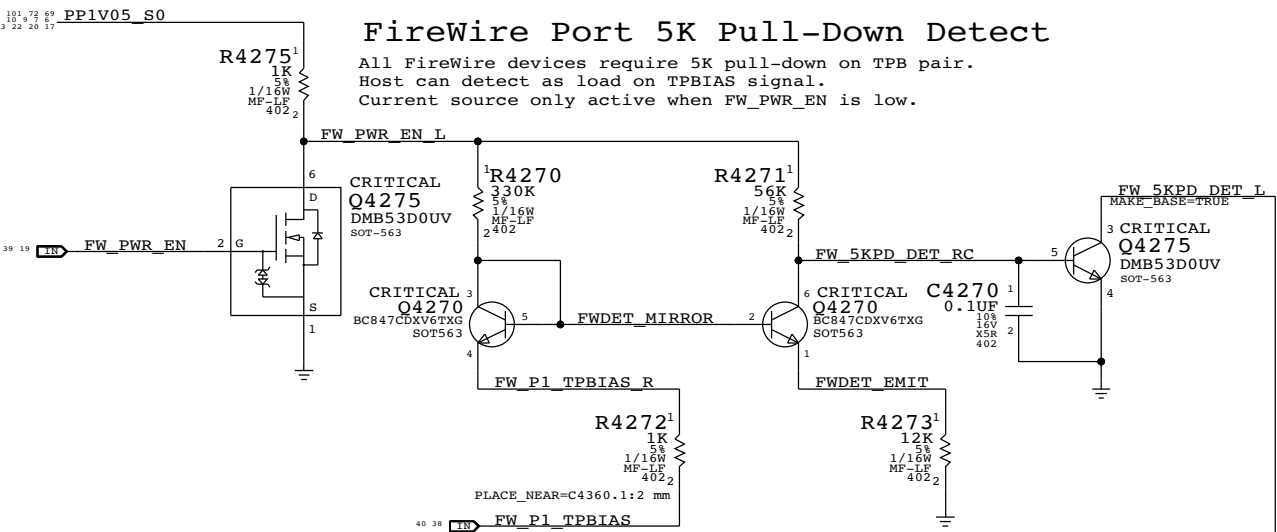


Supervisor & CLKREQ# Isolation



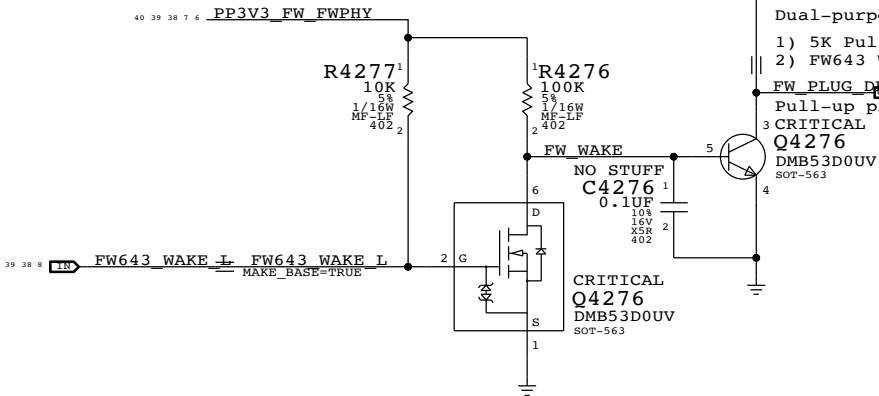
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.  
Host can detect as load on TPBIAS signal.  
Current source only active when FW\_PWR\_EN is low.



FireWire PHY WAKE# Support

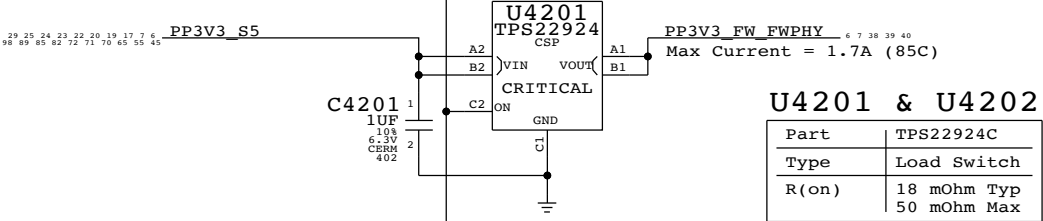
When PHY is powered, FW\_5KPD\_DET\_L acts as legacy PME# signal.



- Dual-purpose output:
- 1) 5K Pull-down Detect when FW\_PWR\_EN is low.
  - 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

3.3V FW Switch

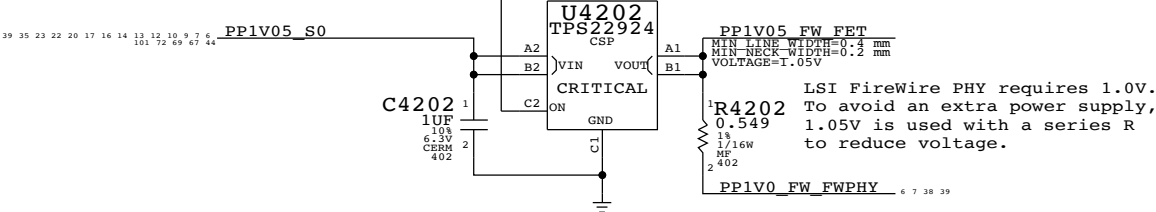



U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



SYNC MASTER=T27 REF		SYNC DATE=06/10/2010	
PAGE TITLE		FireWire Port & PHY Power	
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		42 OF 132	SHEET
		39 OF 101	

## A

1394b implementation based on Apple  
FireWire Design Guide (FWDG 0.6, 5/



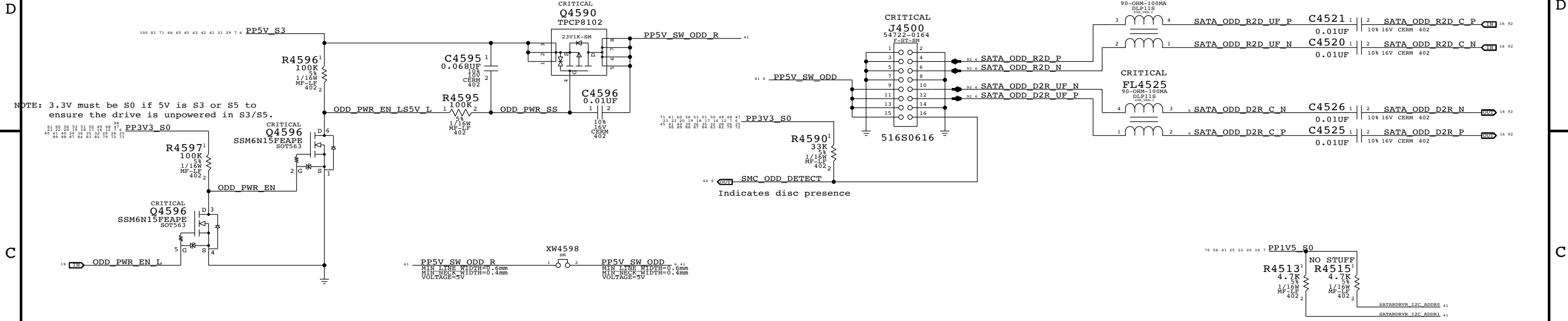
ODD Power Control

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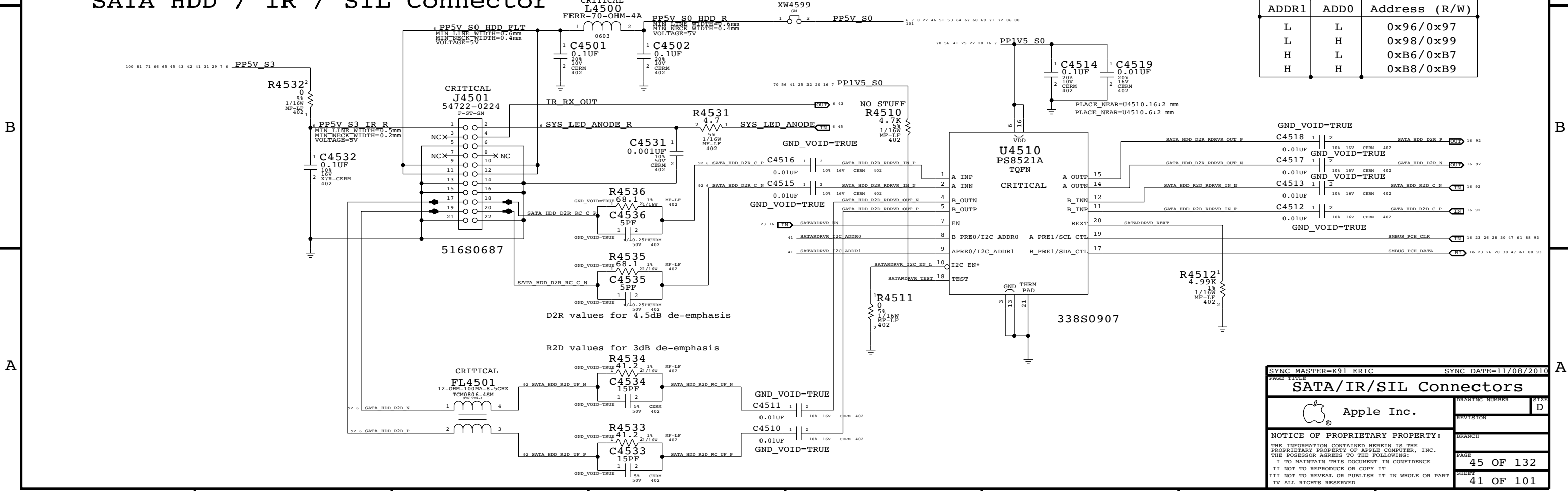


SATA HDD / IR / SIL Connector

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SYNC MASTER=K91 ERIC

SYNC DATE=11/08/2010

SATA/IR/SIL Connectors

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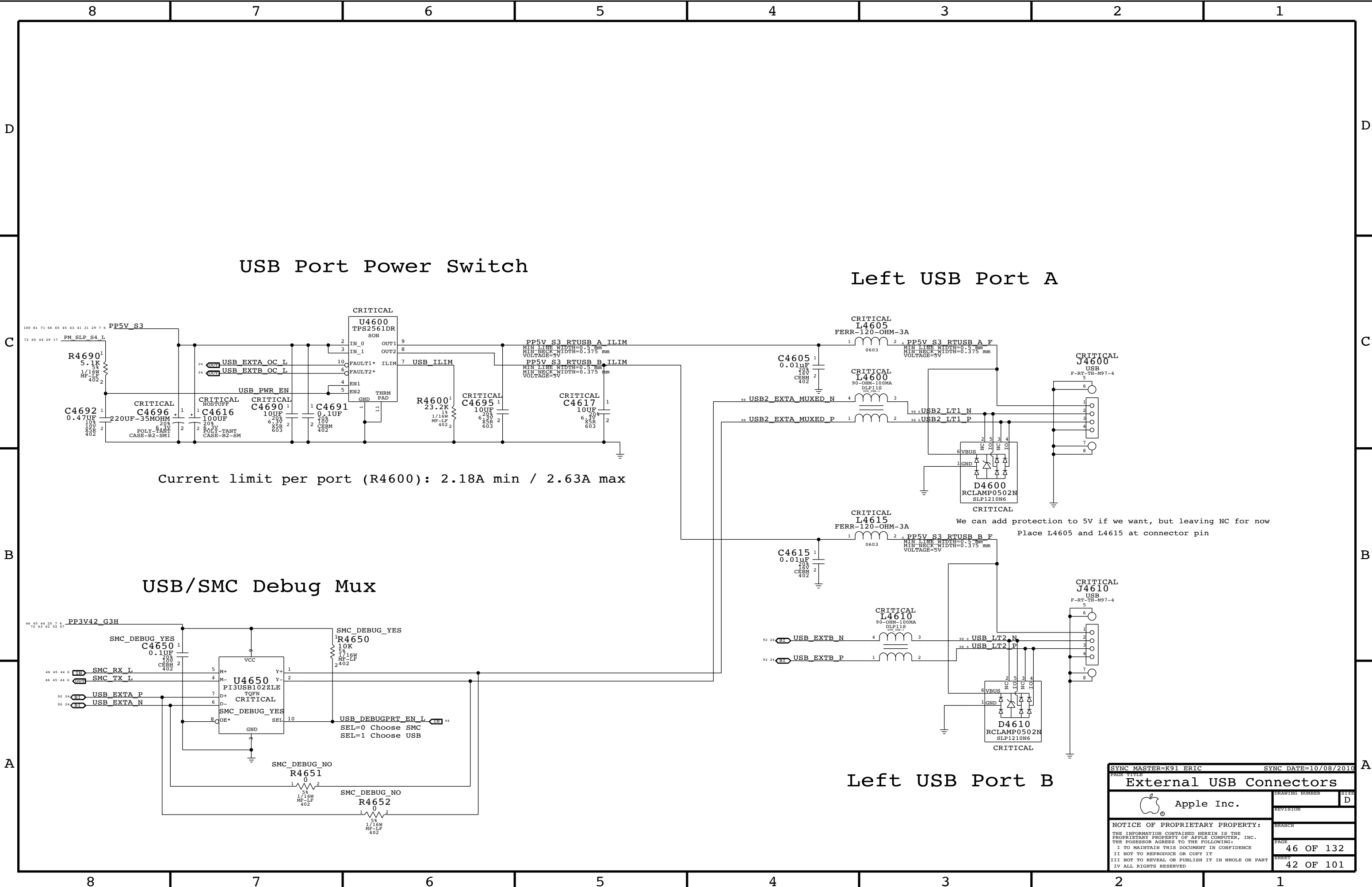
SHEET

SIZE

D

45 OF 132

41 OF 101



USB Port Power Switch


Left USB Port A

USB/SMC Debug Mux

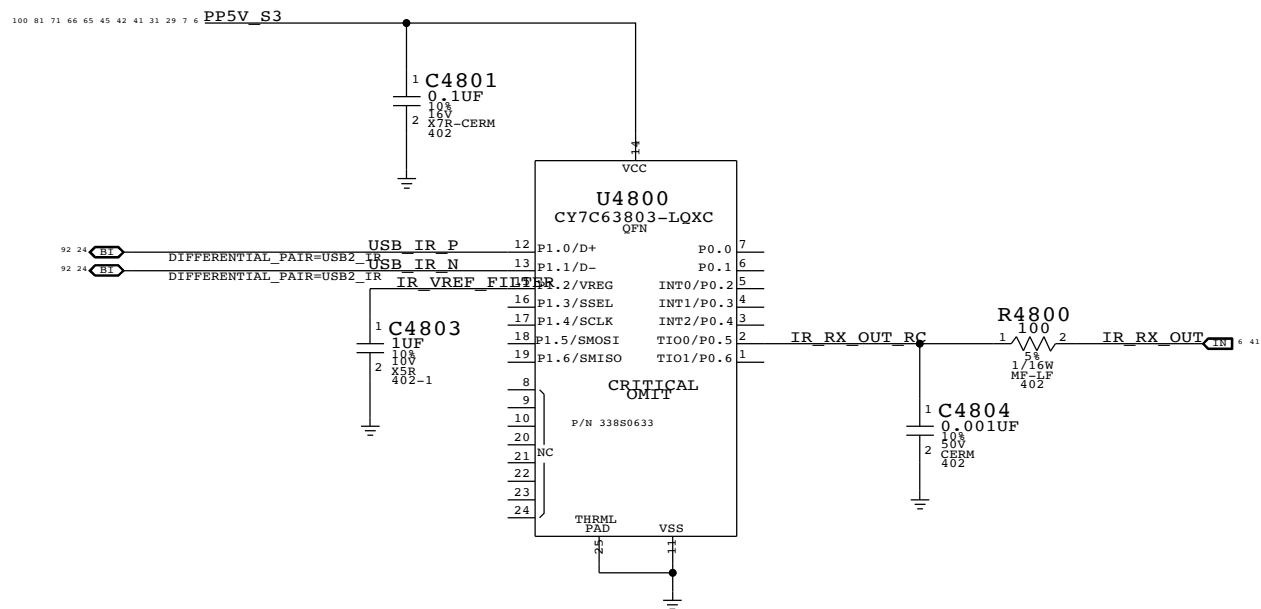
Left USB Port B

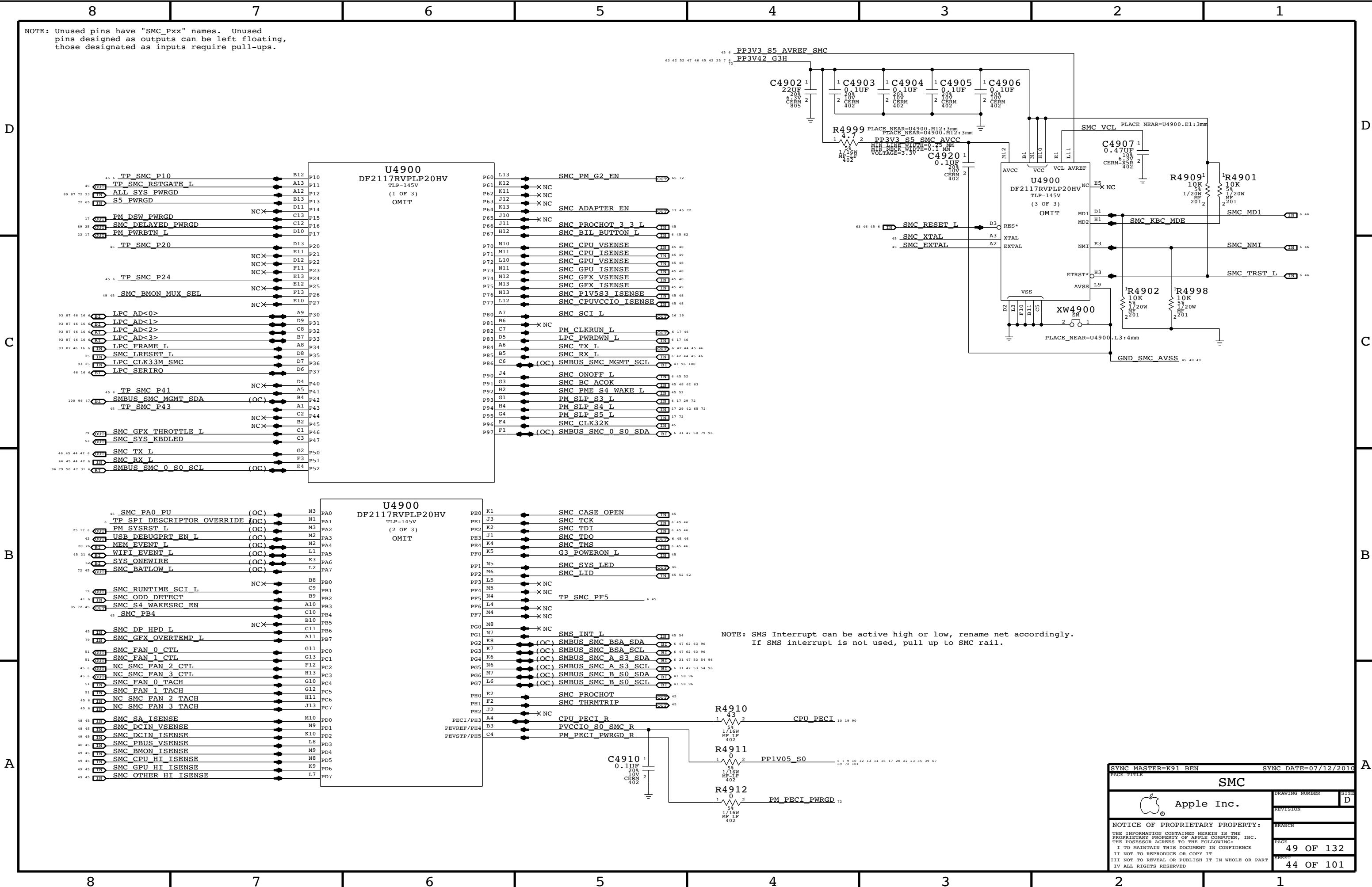
Current limit per port (R4600): 2.18A min / 2.63A max

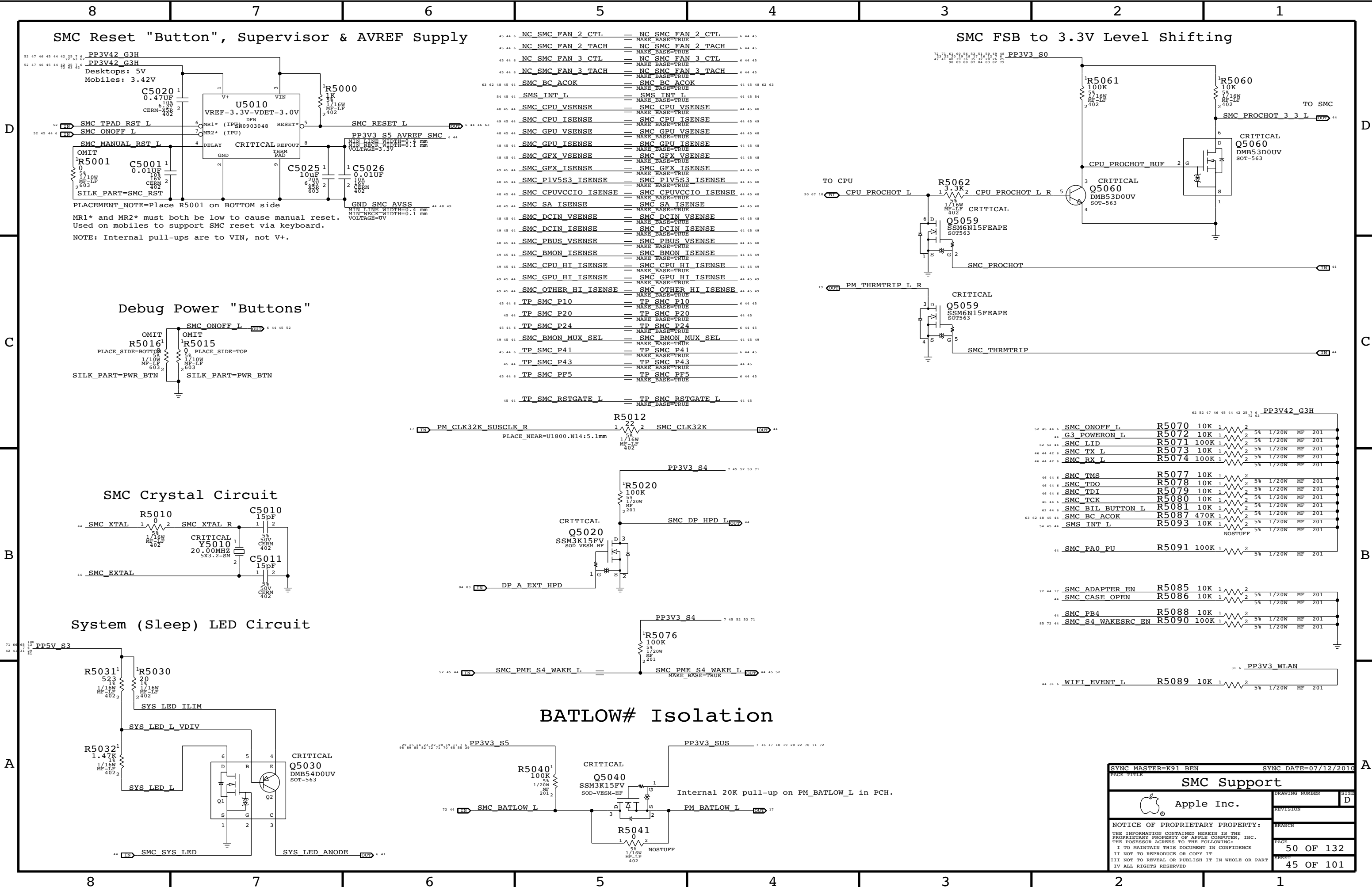
We can add protection to 5V if we want, but leaving NC for now  
Place L4605 and L4615 at connector pin


SYNC MASTER=K91 ERIC		SYNC DATE=10/08/2010	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	46 OF 132
		SHEET	42 OF 101

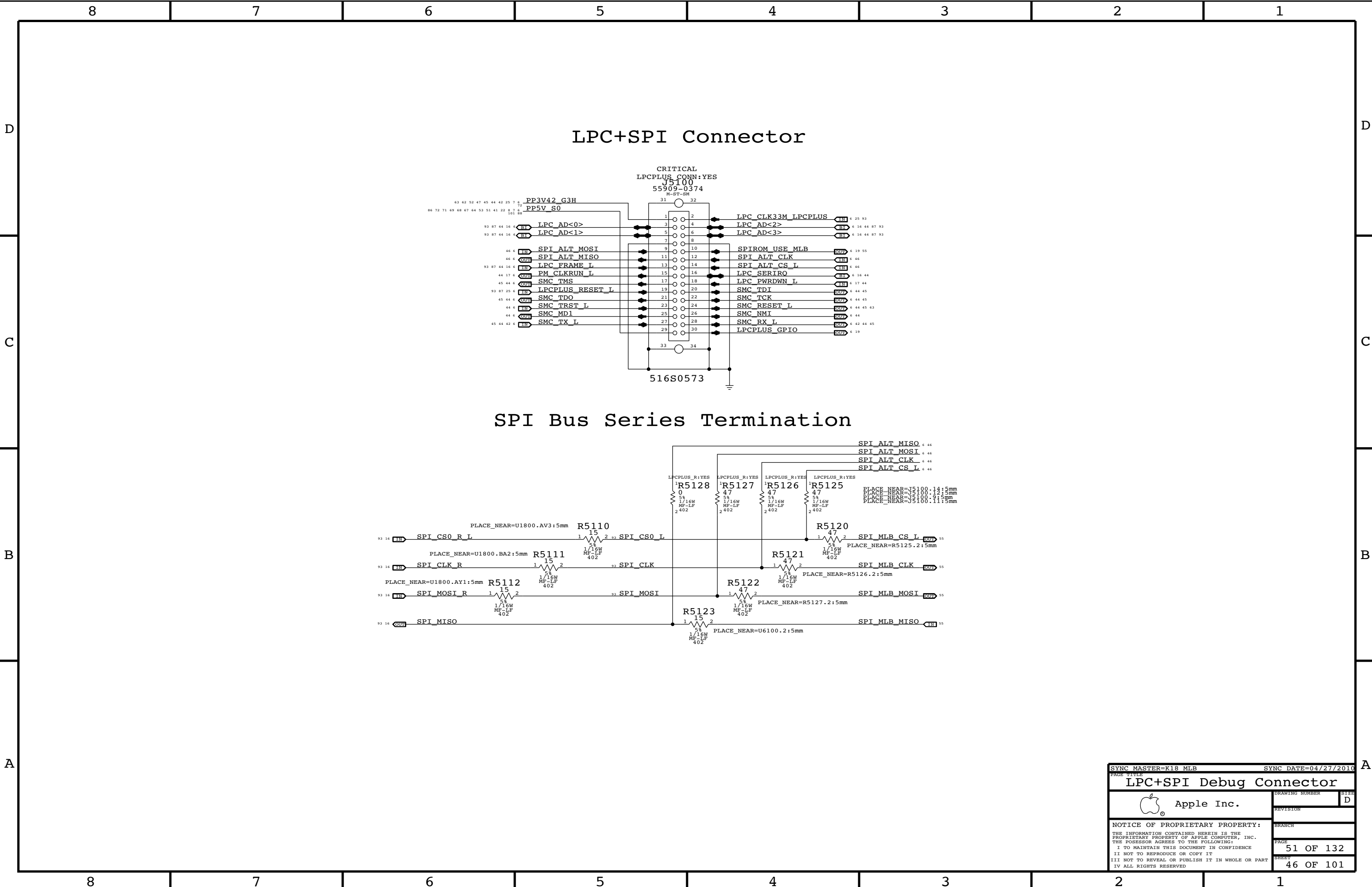
## IR SUPPORT



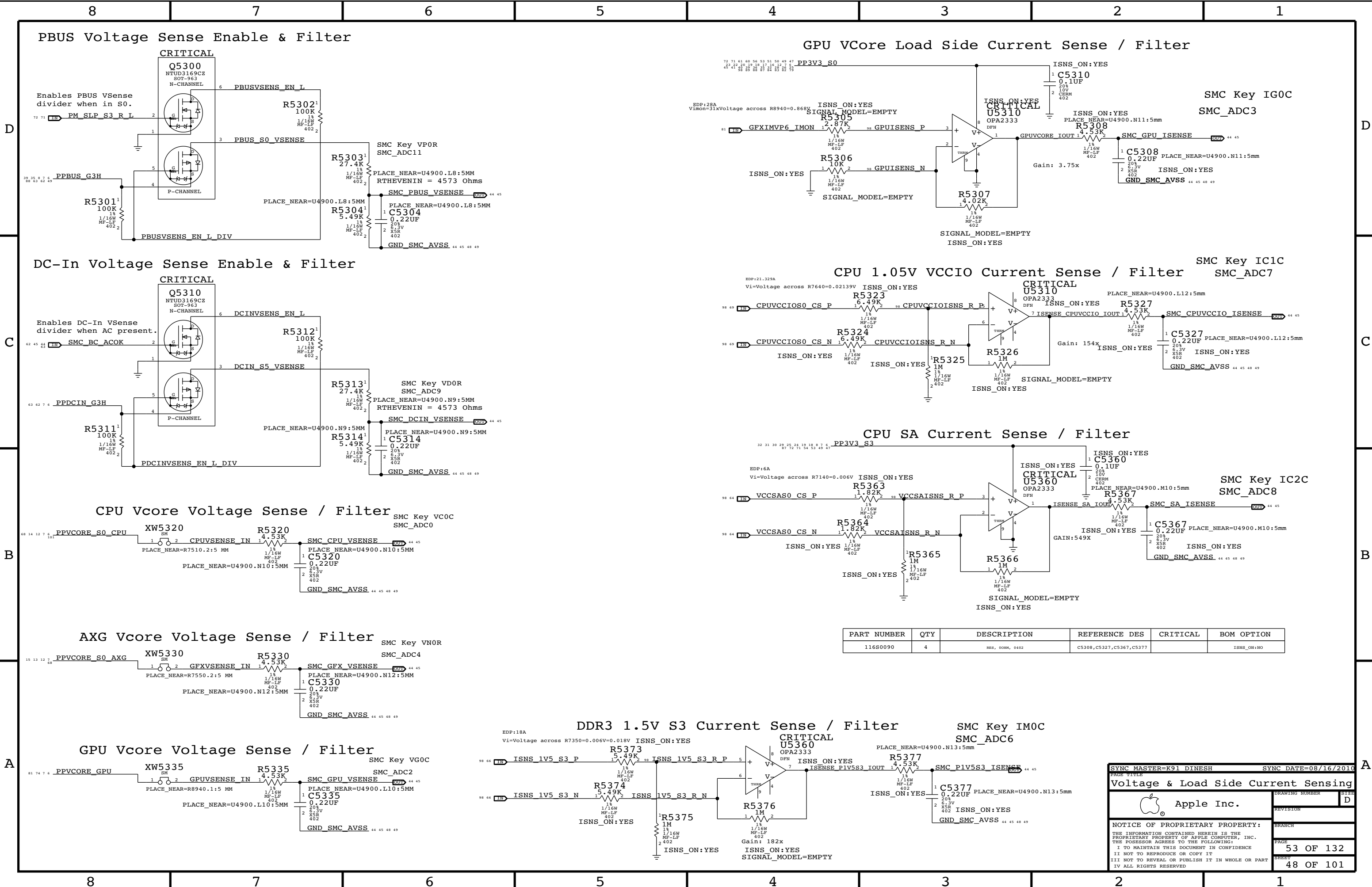




SYNC MASTER=K91 BEN		SYNC DATE=07/12/2010	
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SMC Support			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	4	RES, 00HM, 0402	C5308,C5327,C5367,C5377		ISNS_ON:NO

SYNC MASTER=K91 DINESH

SYNC DATE=08/16/2010

Voltage & Load Side Current Sensing

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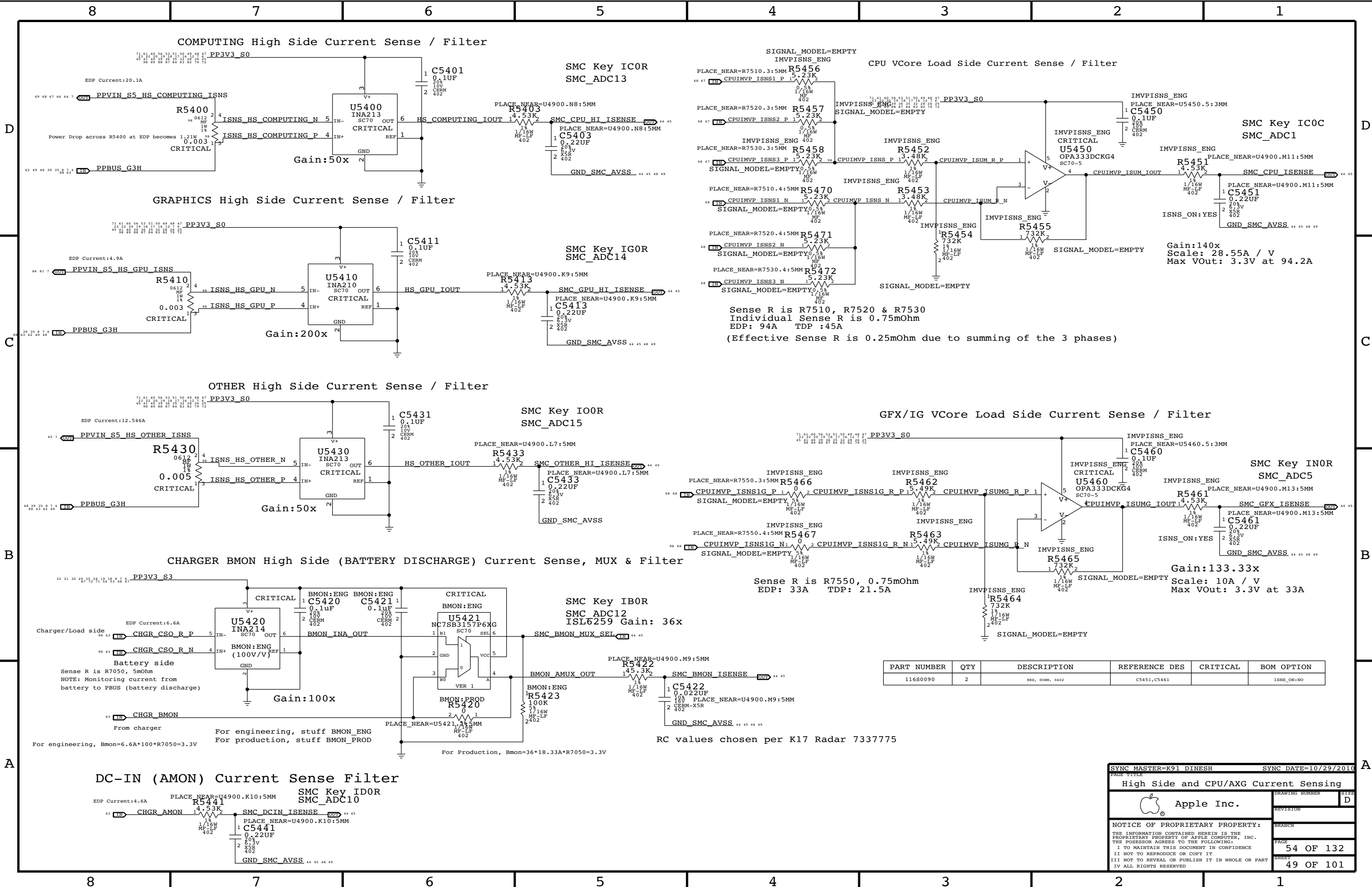
DRAWING NUMBER

53 OF 132

SIZE

48 OF 101





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	2	RES, 00HM, 0402	C5451,C5461		ISNS_ON:NO

SYNC MASTER=K91 DINESH

SYNC DATE=10/29/2010

High Side and CPU/AXG Current Sensing

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SIZE

REVISION

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PAGE

SHEET

49 OF 101

54 OF 132

8	7	6	5	4	3	2	1
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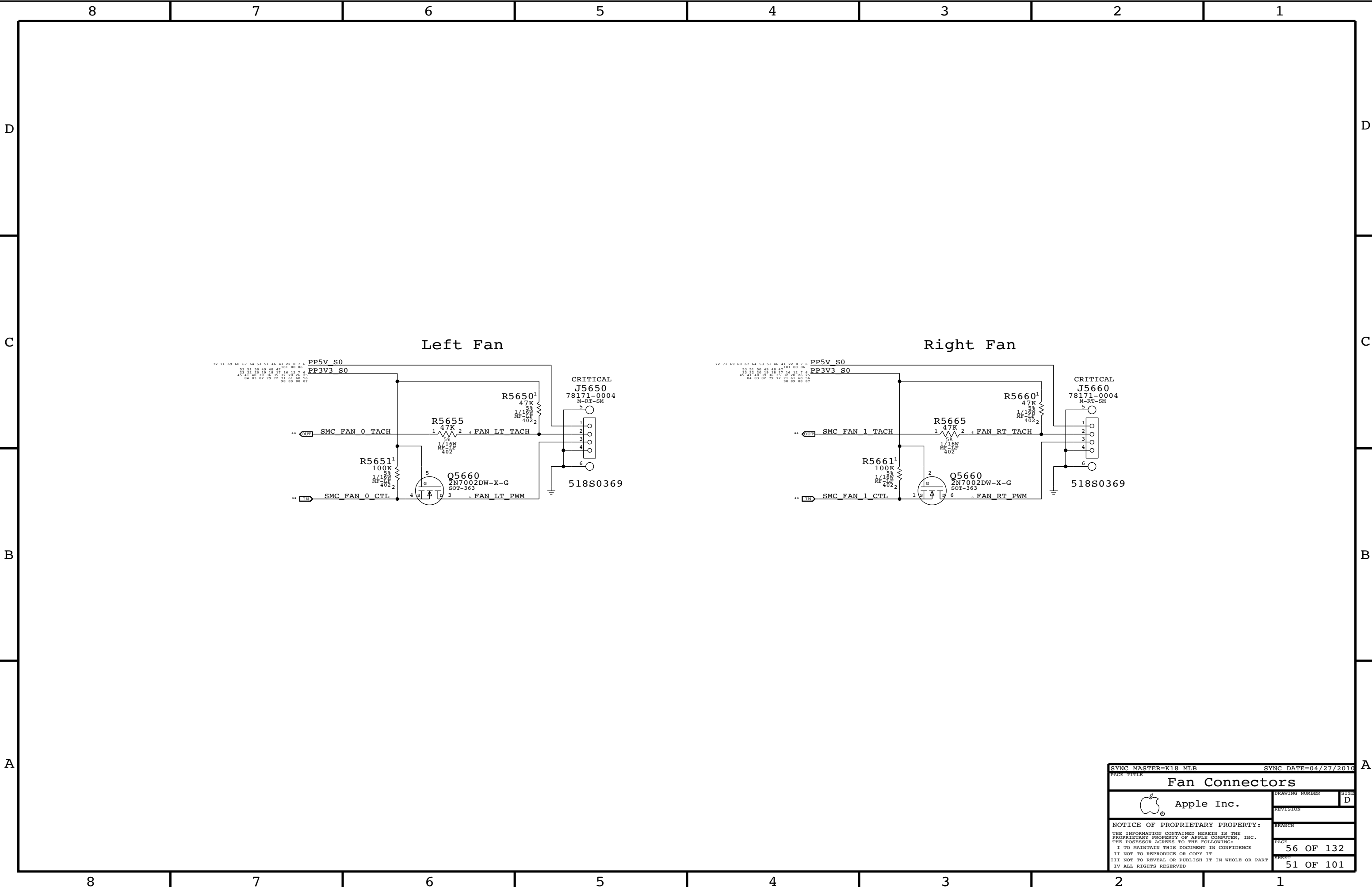


## C



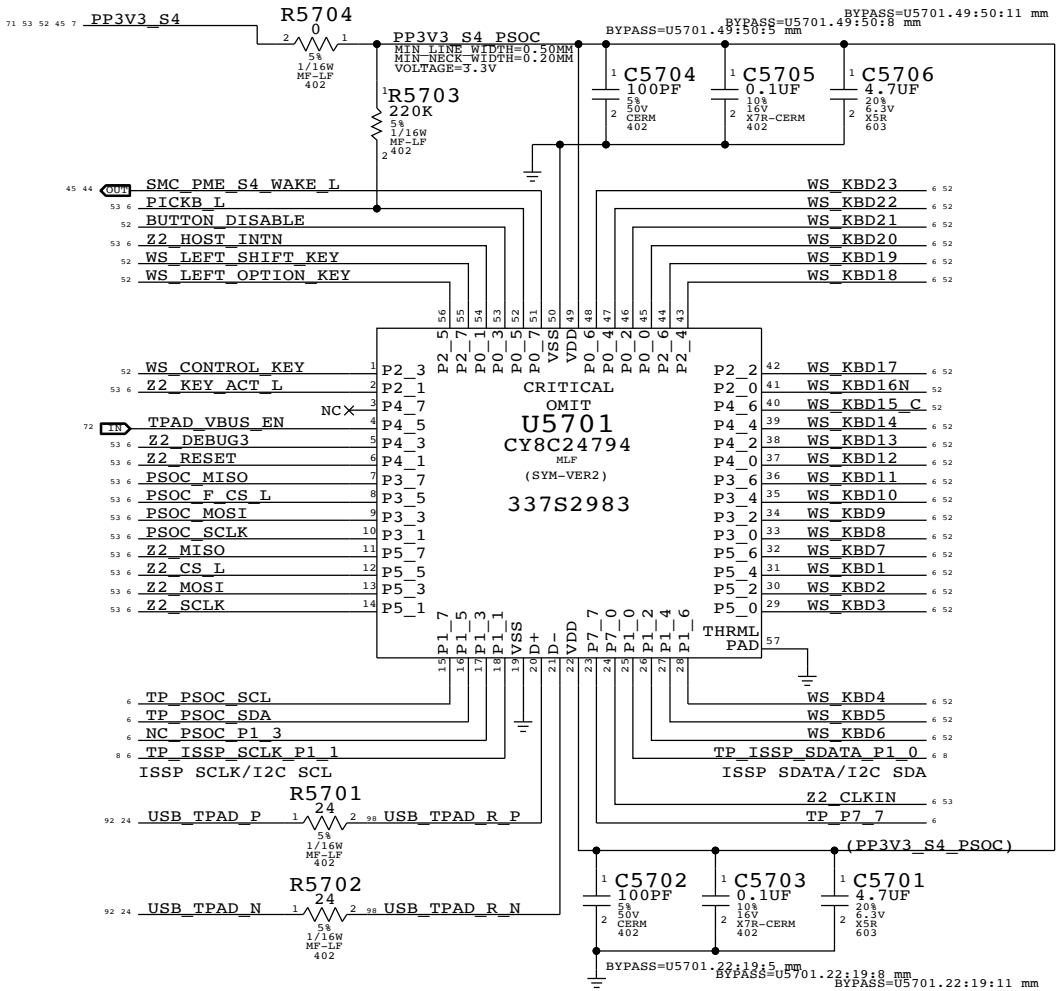
A



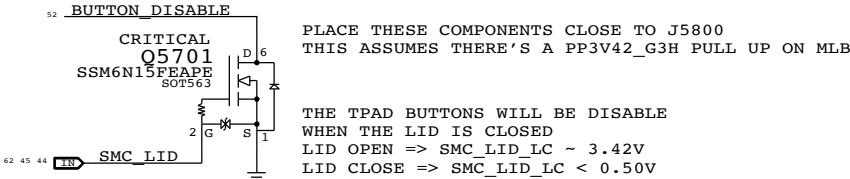


PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

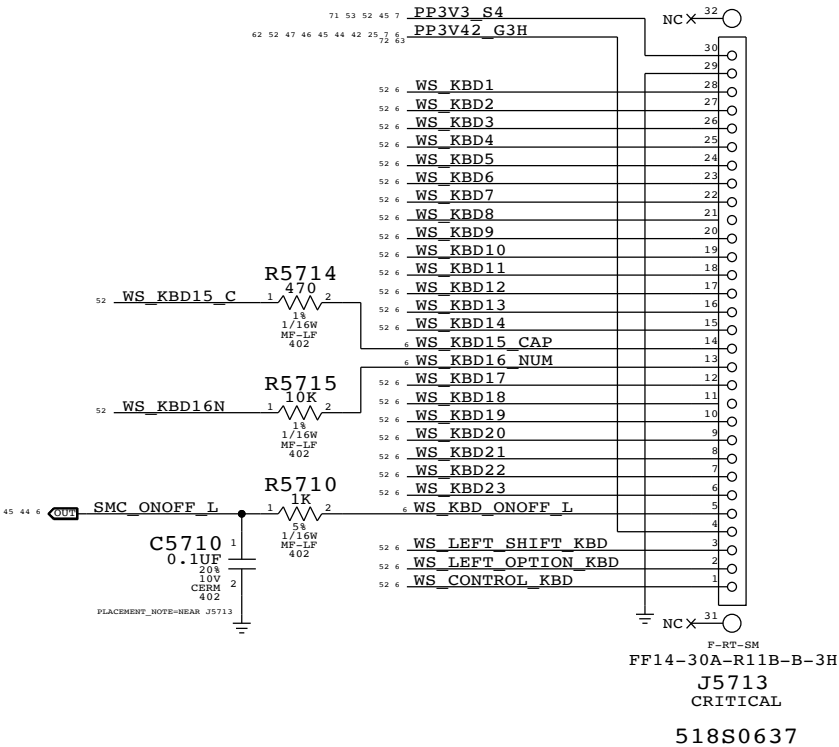


TPAD Buttons Disable



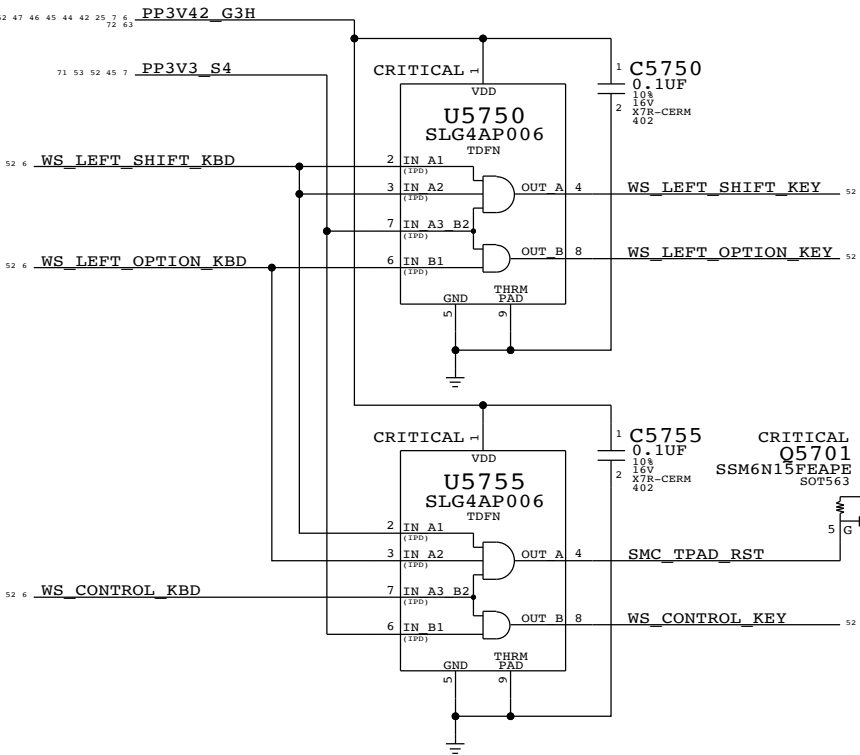
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector



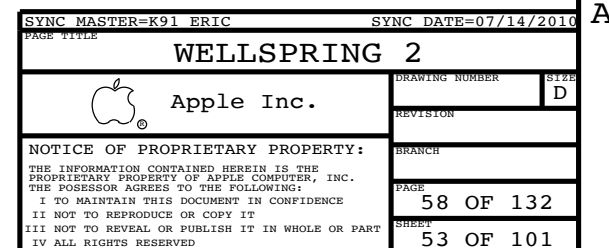
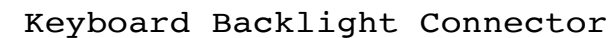
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSOC power to isolate when PSOC is not powered.

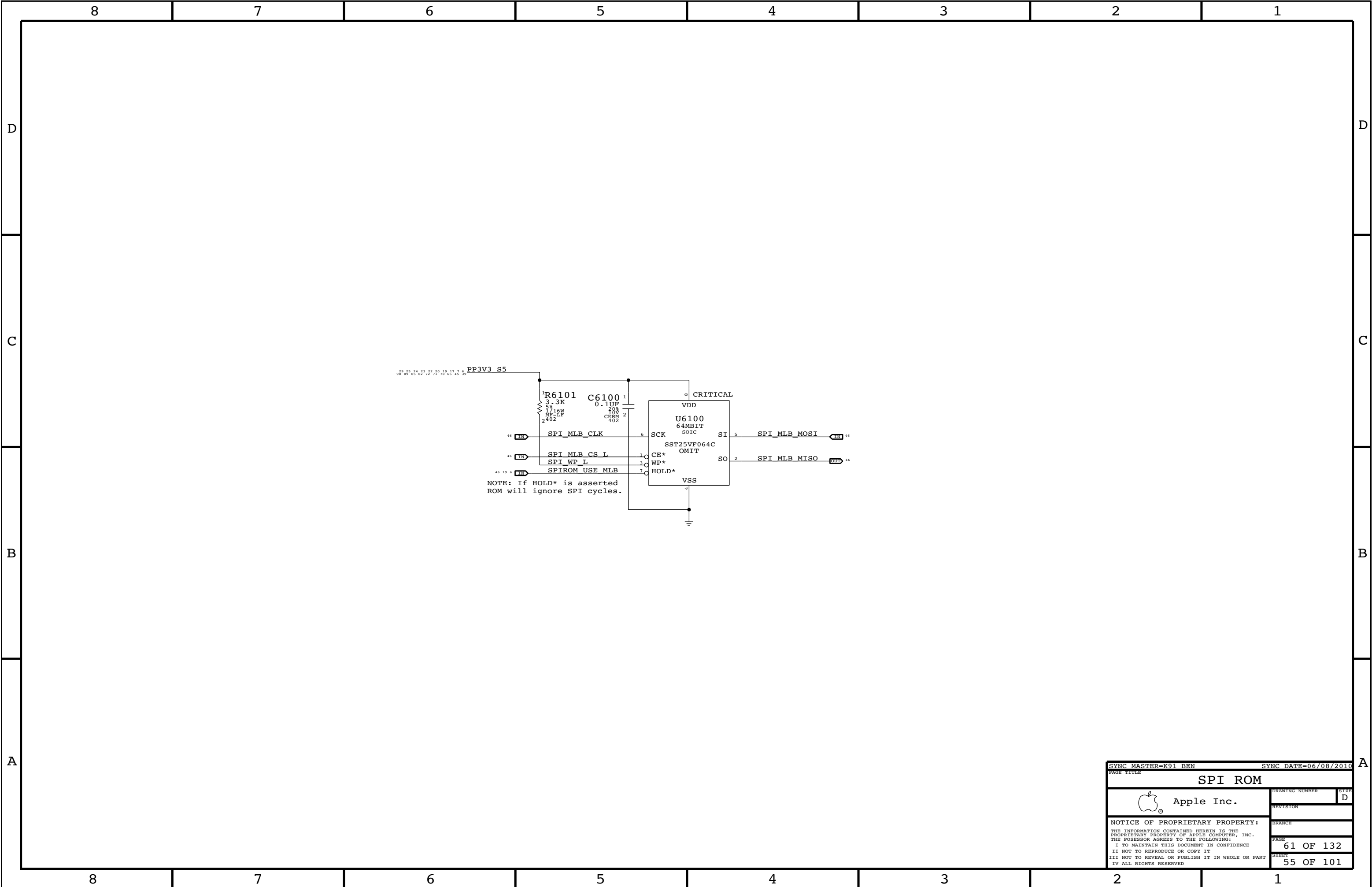


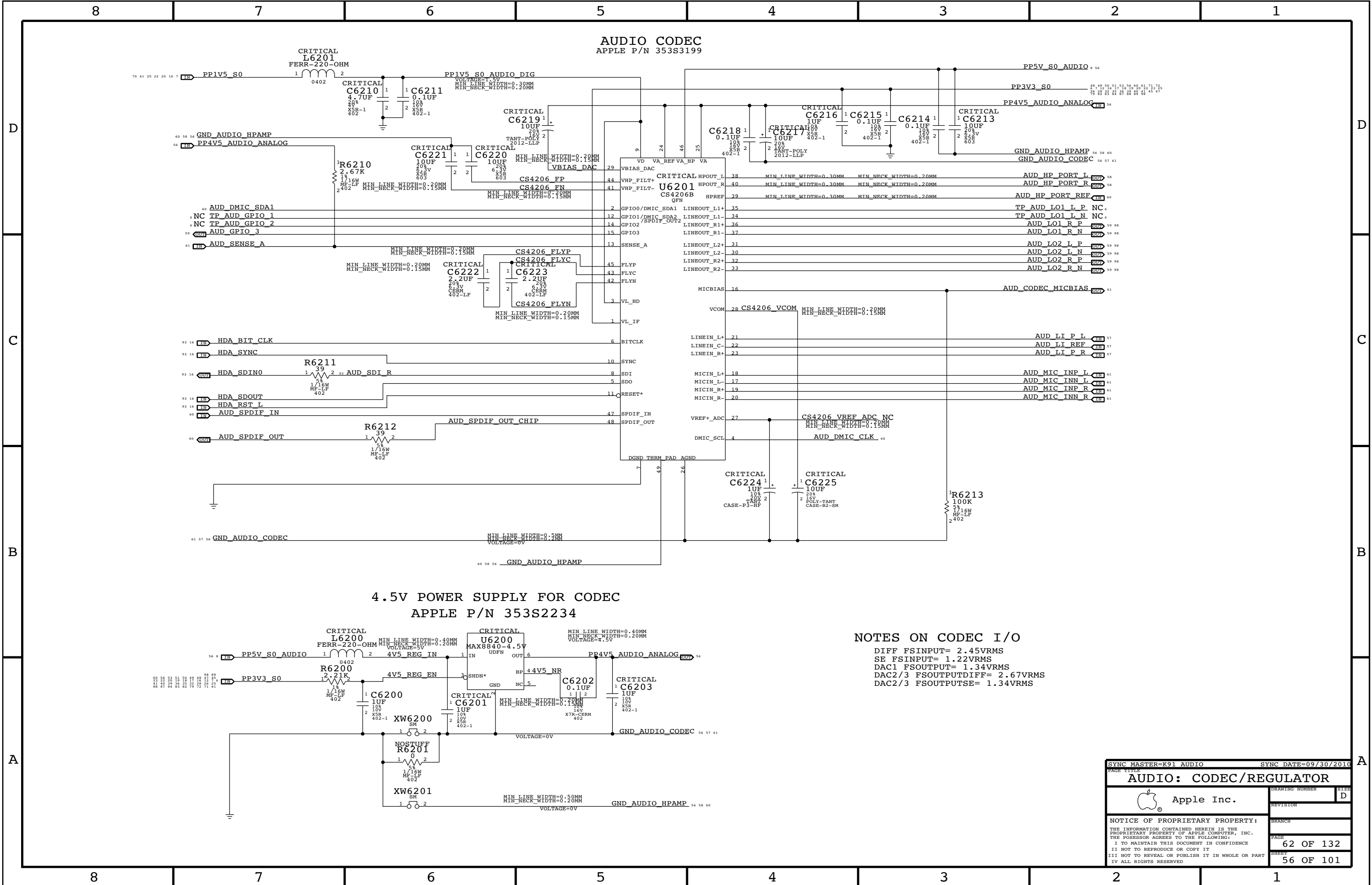
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WELLSPRING 1		DRAWING NUMBER		SIZE D	
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```
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED
```










NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS  
SE FSINPUT= 1.22VRMS  
DAC1 FSOUTPUT= 1.34VRMS  
DAC2/3 FSOUTPUTDIFF= 2.67VRMS  
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=K91 AUDIO		SYNC DATE=09/30/2010	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
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		BRANCH	
		PAGE	62 OF 132
		SHEET	56 OF 101



8 7 6 5 4 3 2 1

D

C

B

A

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS  
NET RIN = 18K OHMS  
FC = 8 HZ  
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

CRITICAL  
C6300  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI L  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6300  
7.87K  
1%  
1/16W  
MF-LF  
402

AUD LI L DIV  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6301  
21.5K  
1%  
1/16W  
MF-LF  
402

NOSTUFF  
C6301  
820PF  
10%  
50V  
CERM  
402

AUD LI P L  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

CRITICAL  
C6302  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI GND  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6303  
10  
1%  
1/16W  
MF-LF  
402

GND\_AUDIO\_CODEC

AUD LI REF  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

NOSTUFF  
C6304  
820PF  
10%  
50V  
CERM  
402

AUD LI R  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6306  
7.87K  
1%  
1/16W  
MF-LF  
402

AUD LI R DIV  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

CRITICAL  
C6303  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI P R  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

SYNC MASTER=K91 AUDIO SYNC DATE=07/12/2010

PAGE TITLE

AUDIO: LINE INPUT FILTER

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REVISION  
BRANCH  
PAGE  
SHEET

63 OF 132  
57 OF 101

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

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8 7 6 5 4 3 2 1

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS  
NET RIN = 18K OHMS  
FC = 8 HZ  
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

CRITICAL  
C6300  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI L  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6300  
7.87K  
1%  
1/16W  
MF-LF  
402

AUD LI L DIV  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6301  
21.5K  
1%  
1/16W  
MF-LF  
402

NOSTUFF  
C6301  
820PF  
10%  
50V  
CERM  
402

AUD LI P L  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

CRITICAL  
C6302  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI GND  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6303  
10  
1%  
1/16W  
MF-LF  
402

GND\_AUDIO\_CODEC

AUD LI REF  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

NOSTUFF  
C6304  
820PF  
10%  
50V  
CERM  
402

AUD LI R  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6306  
7.87K  
1%  
1/16W  
MF-LF  
402

AUD LI R DIV  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

CRITICAL  
C6303  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI P R  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

SYNC MASTER=K91 AUDIO SYNC DATE=07/12/2010

PAGE TITLE

AUDIO: LINE INPUT FILTER

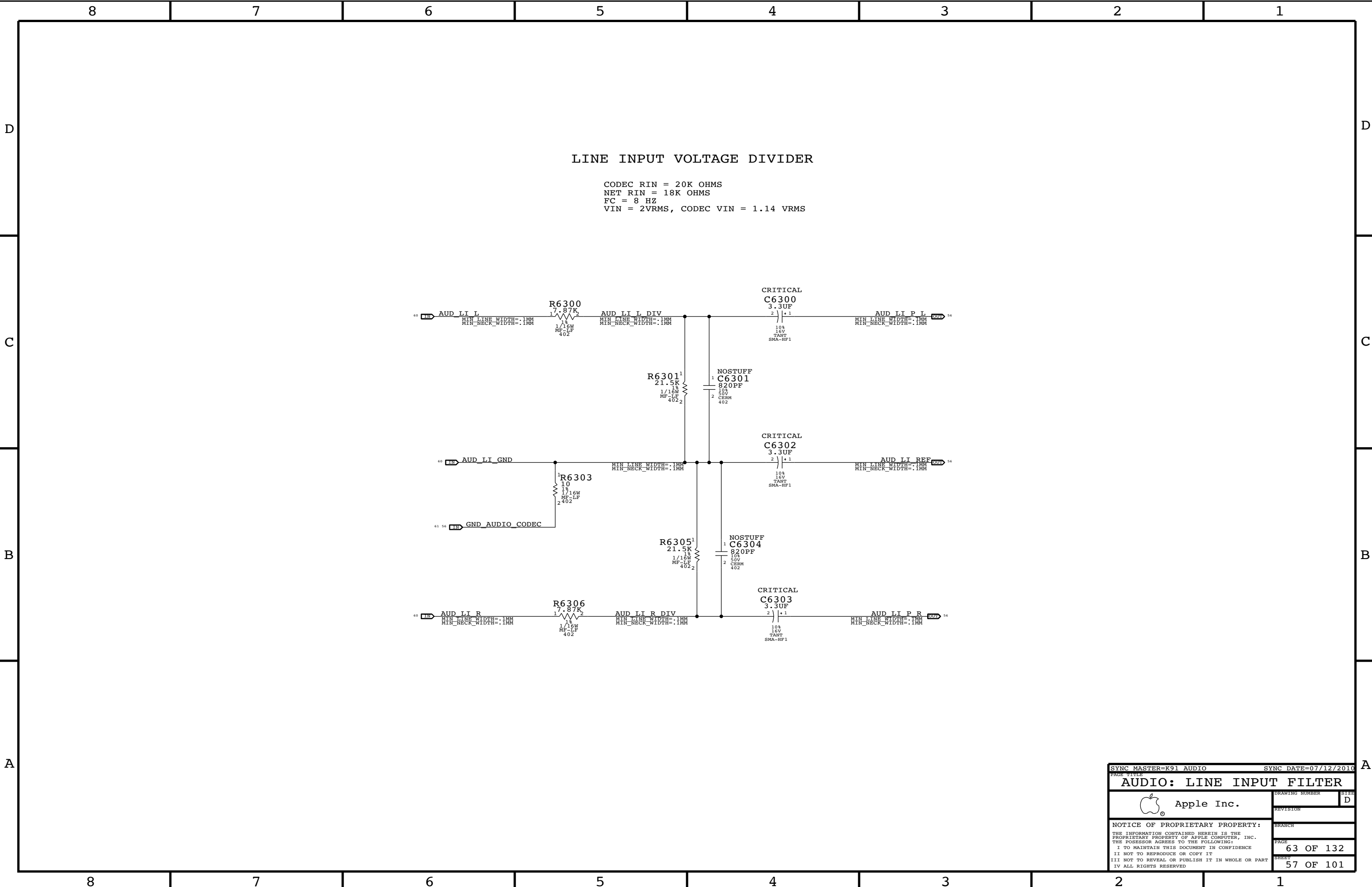
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REVISION  
BRANCH  
PAGE  
SHEET

63 OF 132  
57 OF 101

D



8 7 6 5 4 3 2 1

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8 7 6 5 4 3 2 1

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS  
NET RIN = 18K OHMS  
FC = 8 HZ  
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

CRITICAL  
C6300  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI L  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6300  
7.87K  
1%  
1/16W  
MF-LF  
402

AUD LI L DIV  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6301  
21.5K  
1%  
1/16W  
MF-LF  
402

NOSTUFF  
C6301  
820PF  
10%  
50V  
CERM  
402

AUD LI P L  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

CRITICAL  
C6302  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI GND  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6303  
10  
1%  
1/16W  
MF-LF  
402

GND\_AUDIO\_CODEC

AUD LI REF  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

NOSTUFF  
C6304  
820PF  
10%  
50V  
CERM  
402

AUD LI R  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

R6306  
7.87K  
1%  
1/16W  
MF-LF  
402

AUD LI R DIV  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

CRITICAL  
C6303  
3.3UF  
10%  
16V  
TANT  
SMA-HF1

AUD LI P R  
MIN LINE WIDTH=.1MM  
MIN NECK WIDTH=.1MM

SYNC MASTER=K91 AUDIO SYNC DATE=07/12/2010

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AUDIO: LINE INPUT FILTER

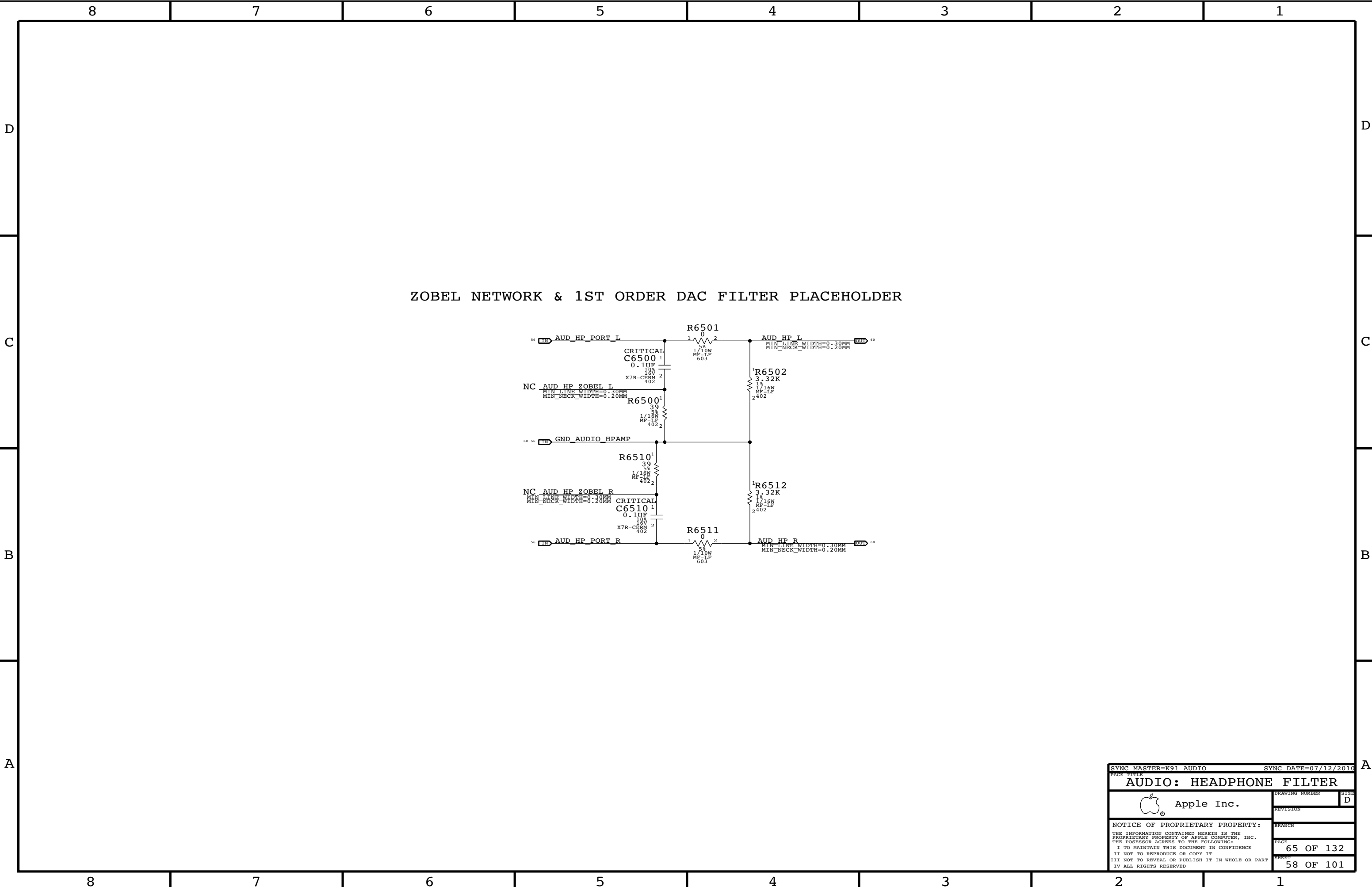
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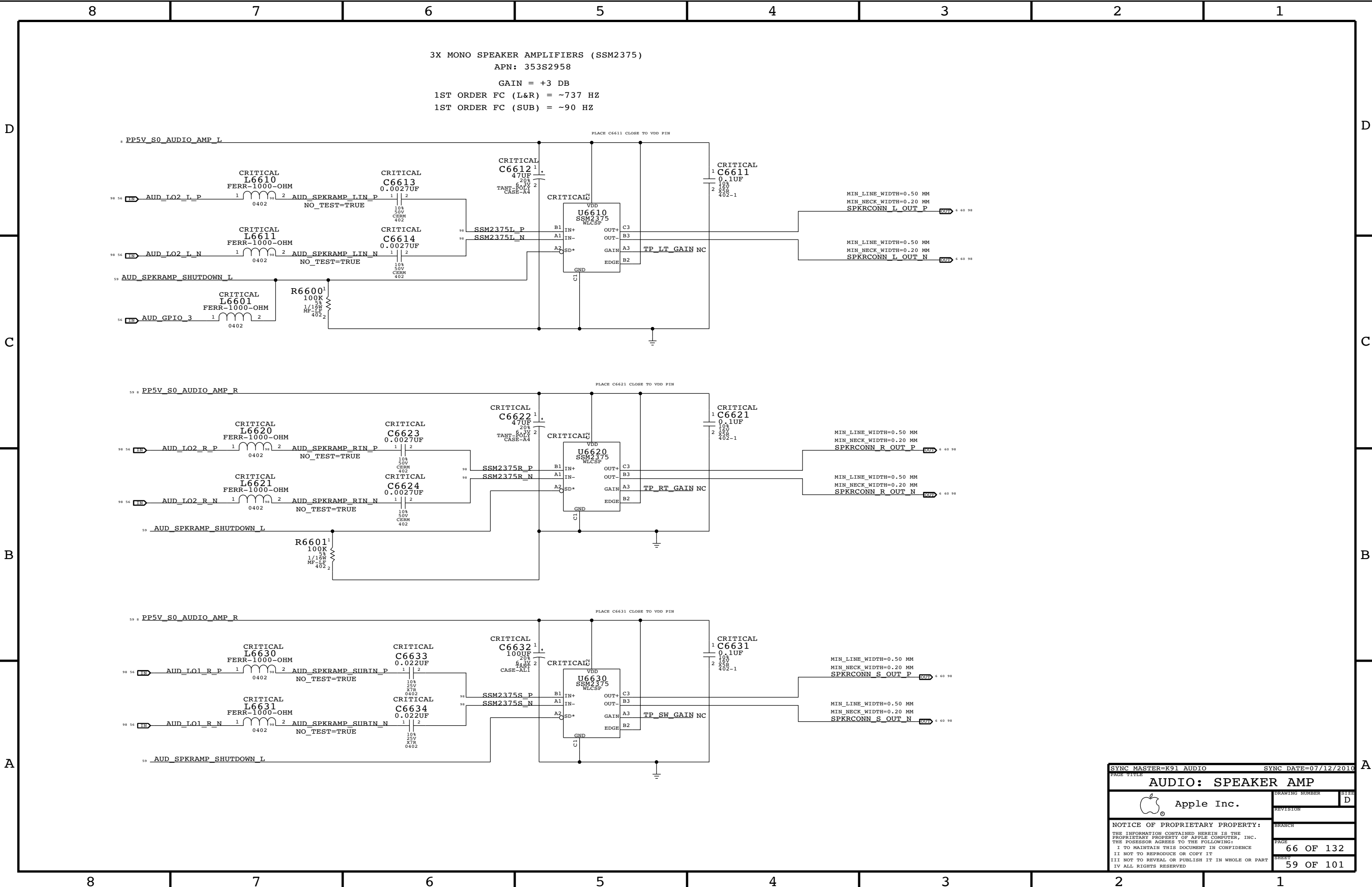
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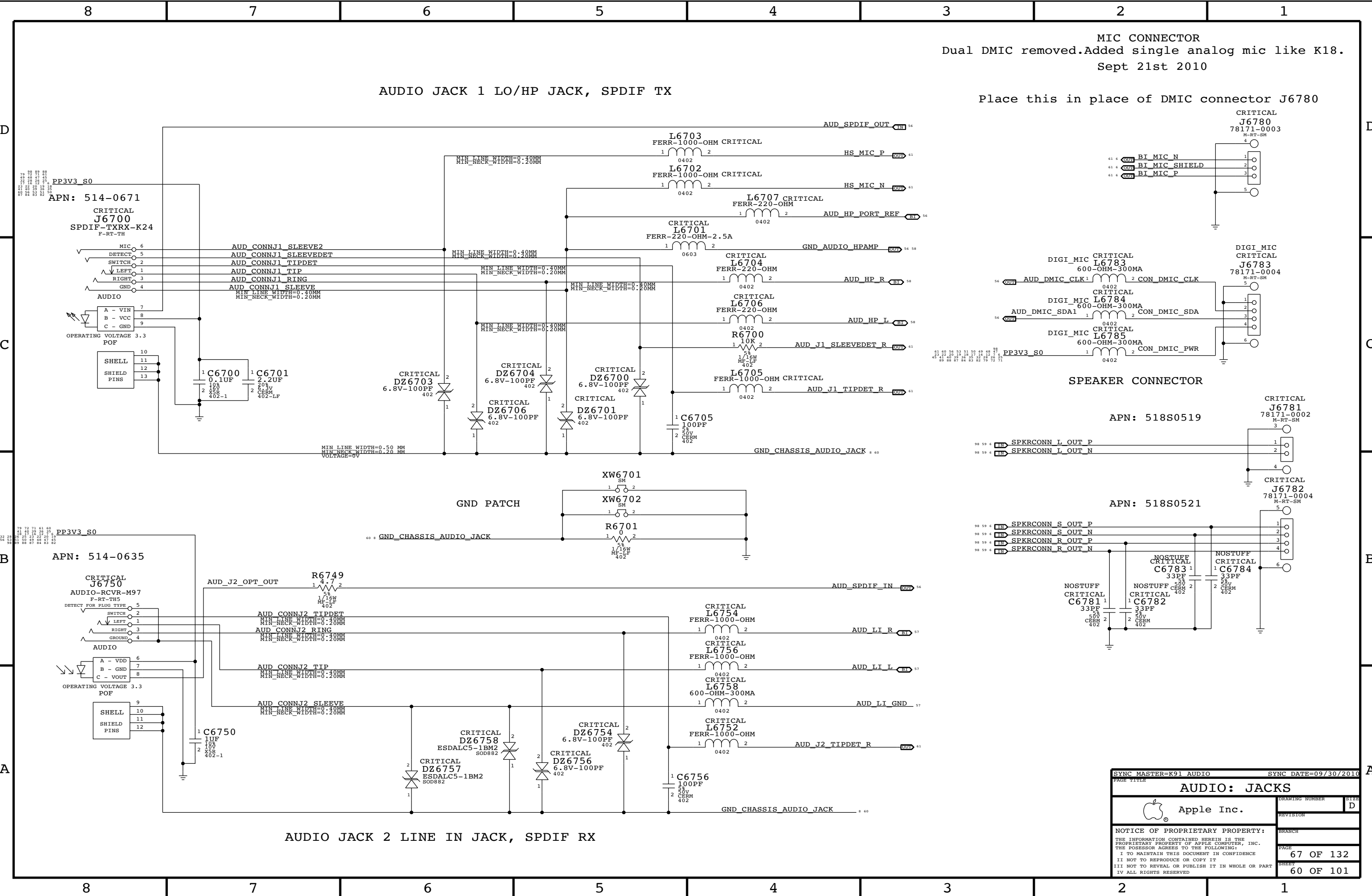
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PAGE  
SHEET

63 OF 132  
57 OF 101

D

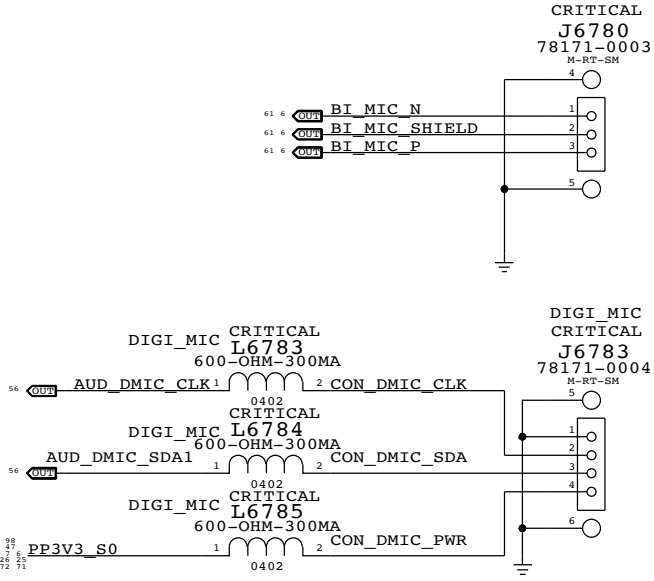




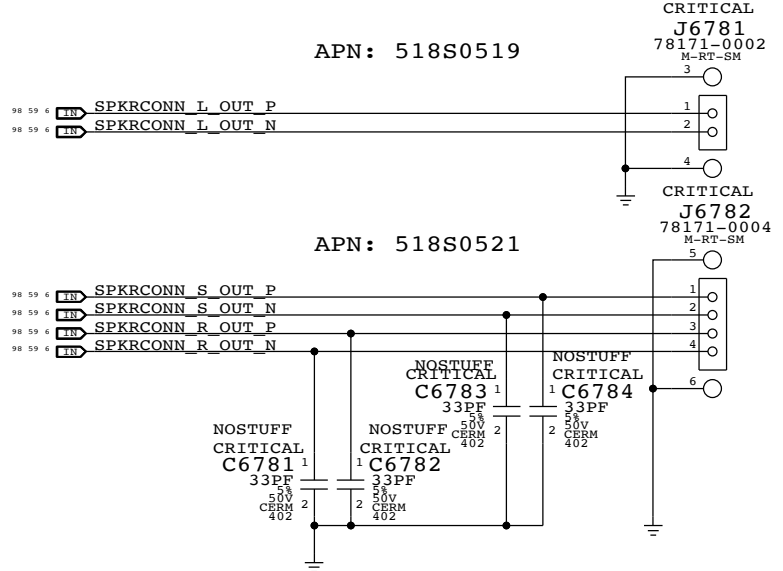


MIC CONNECTOR  
Dual DMIC removed.Added single analog mic like K18.  
Sept 21st 2010

Place this in place of DMIC connector J6780



SPEAKER CONNECTOR

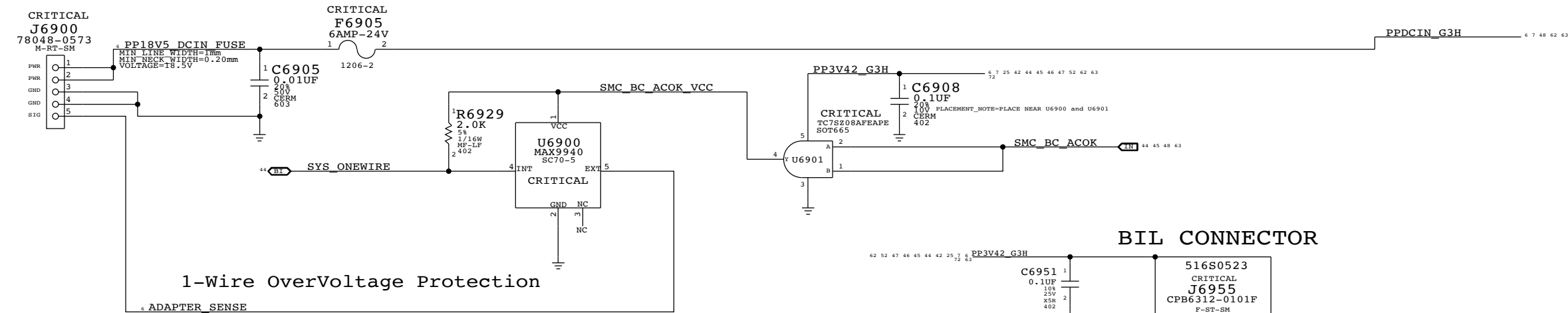


AUDIO JACK 2 LINE IN JACK, SPDIF RX

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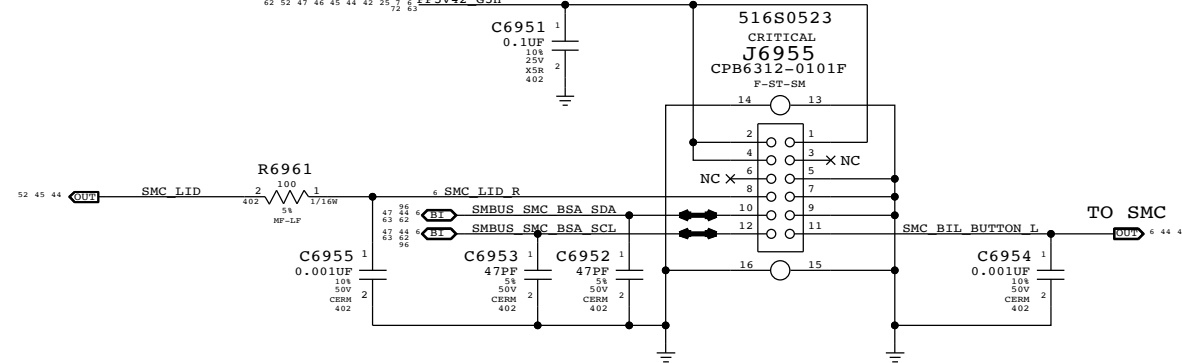


MagSafe DC Power Jack



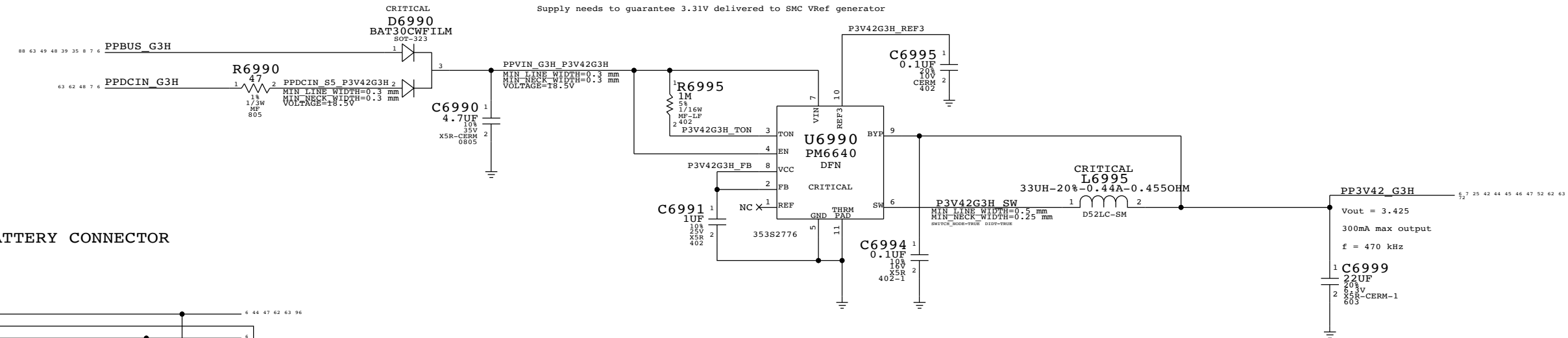
The chassis ground will otherwise float and can send transients onto ADAPTER\_SENSE when AC is connected.

BIL CONNECTOR

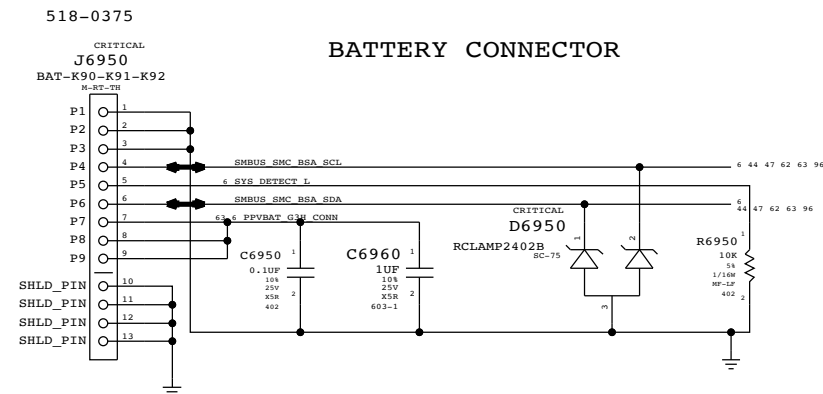


3.425V "G3Hot" Supply

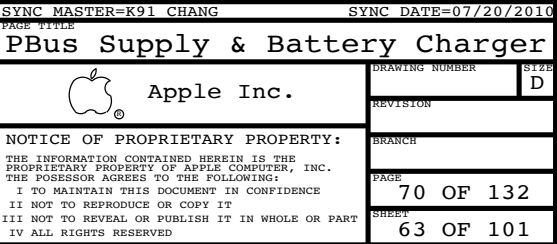
Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR

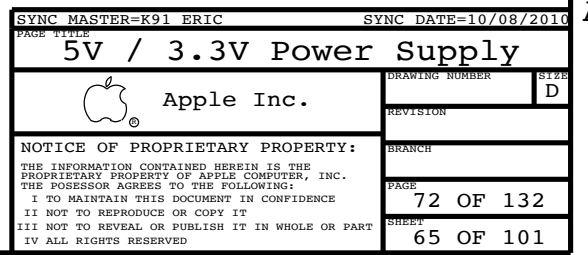


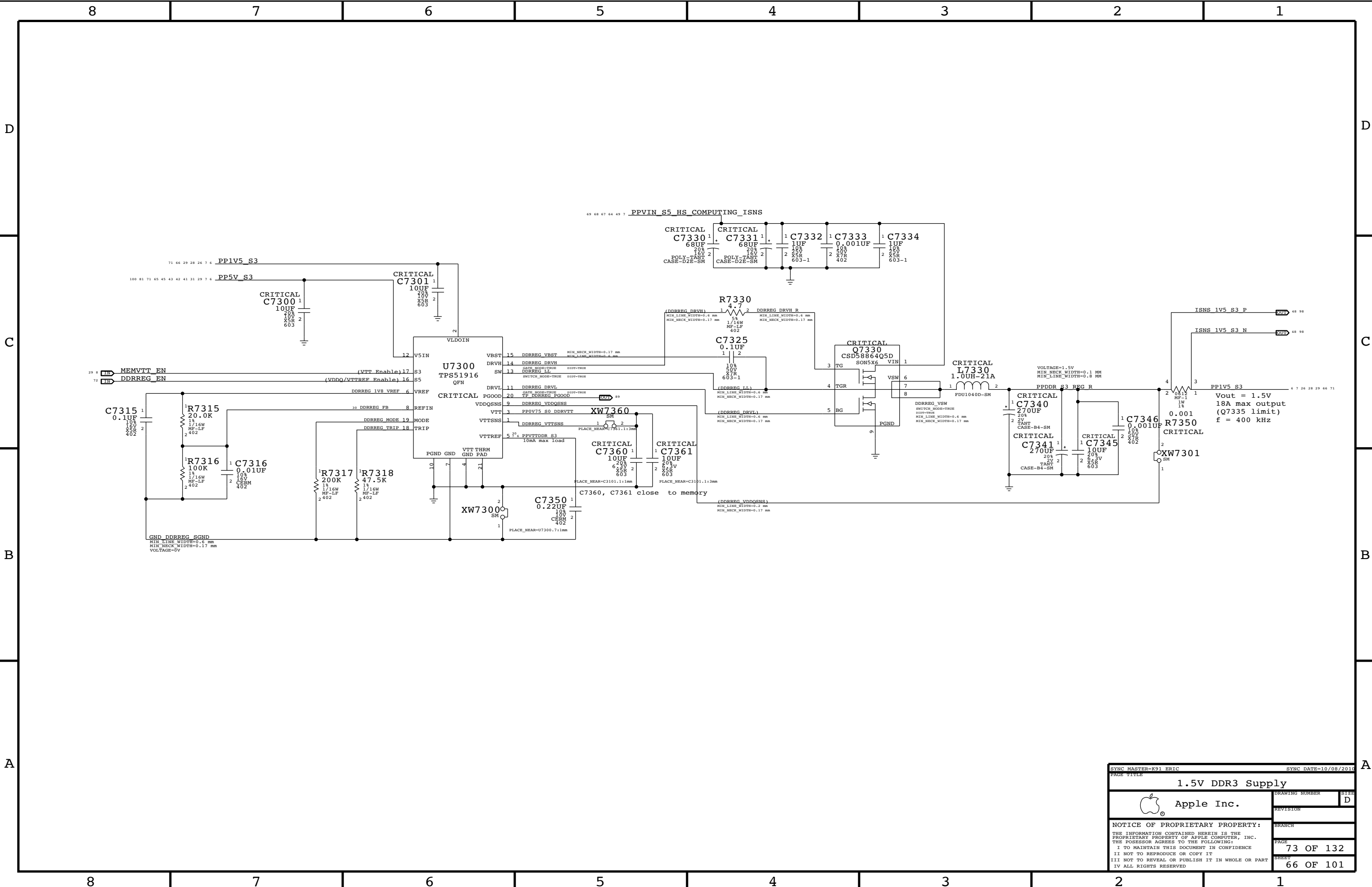
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PAGE TITLE		DRAWING NUMBER	
DC-In & Battery Connectors		SIZE	
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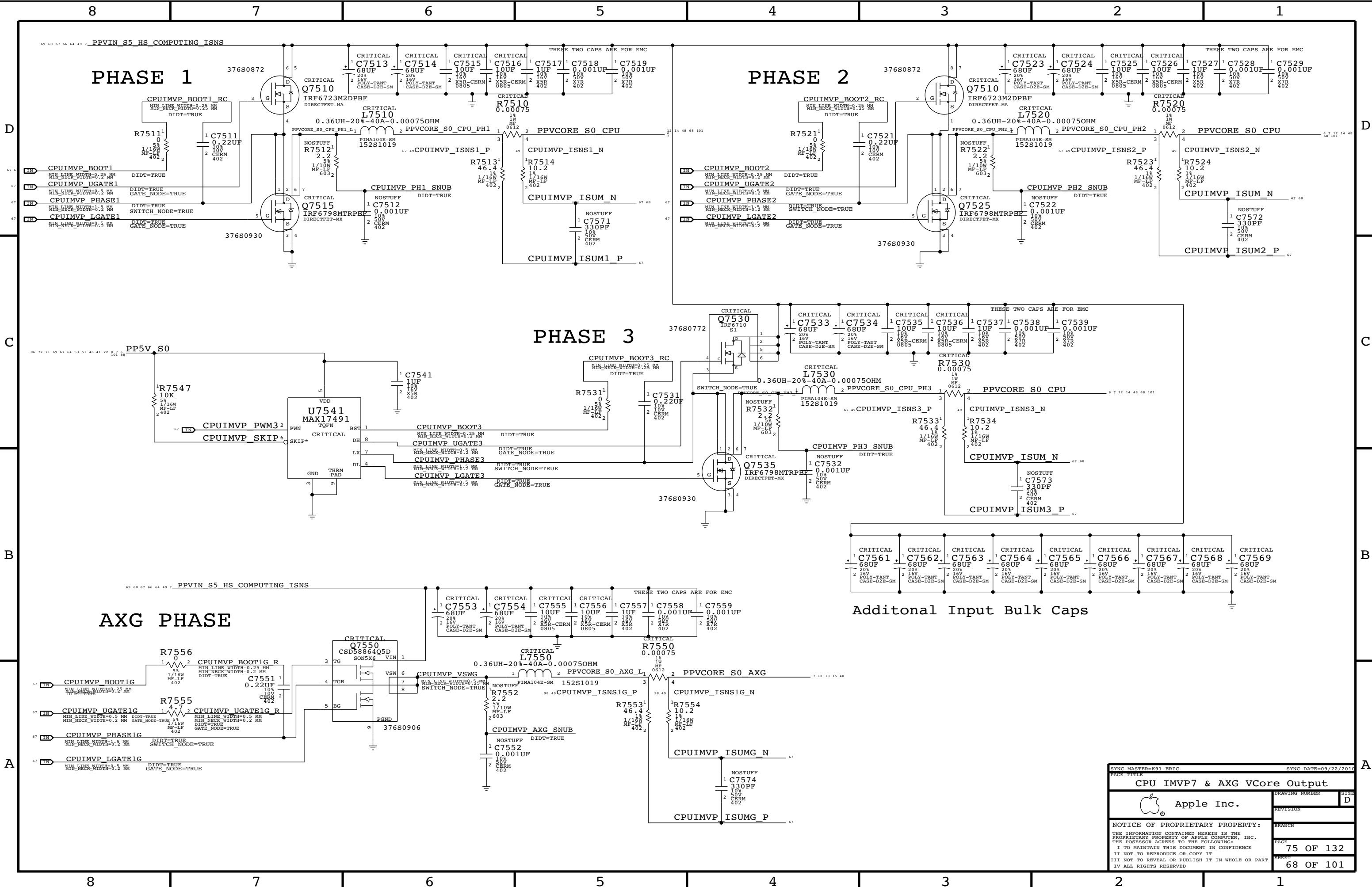




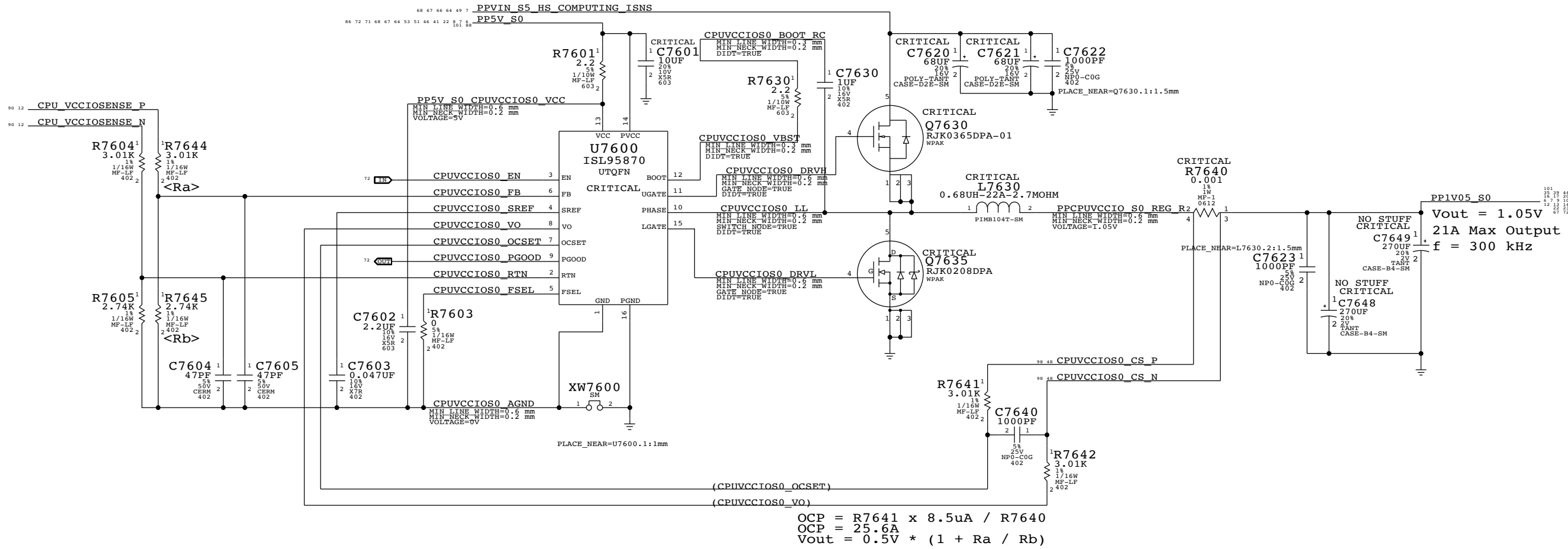




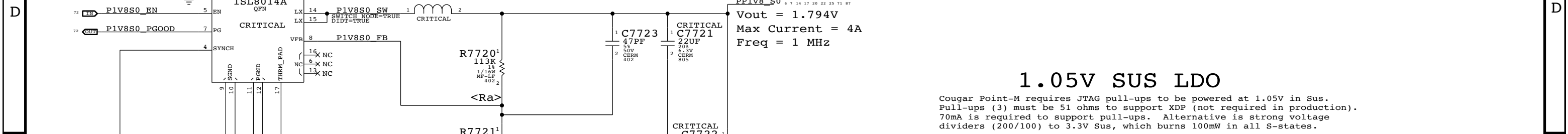




CPU VCCIO (1.05V S0) Regulator

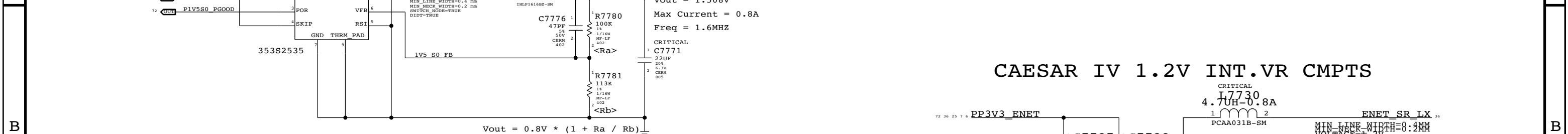
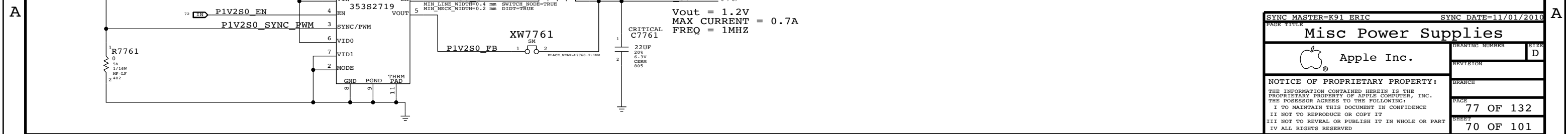


8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



C 1 5V S0 Regulator

Diagram illustrating a project network with activities and their durations. The network includes a start node, a node for 'PF3V3\_S5' (duration 98), and a 'CRITICAL' path. The 'CRITICAL' path is highlighted in red and includes activities with durations 29, 25, 24, 23, 22, 20, 19, 17, 7, 5, 39, 89, 85, 82, 72, 71, 70, 65, 55, 45, and 39.

[illegible]

CRITICAL

XDP\_PCH

U7740  
TPS720105  
SON

PP3V3\_SUS

PP1V05\_SUS

Vout = 1.05V  
Max Current = 0.35A

XDP\_PCH  
C7740  
10µF  
10%  
6.3V  
CERM  
402

XDP\_PCH  
C7741  
2.2µF  
10%  
6.3V  
X5R  
402

BIAS  
IN  
EN  
GND  
THRM PAD  
OUT  
NC

72 71 45 22 20 19 18 17 16 7

7 23

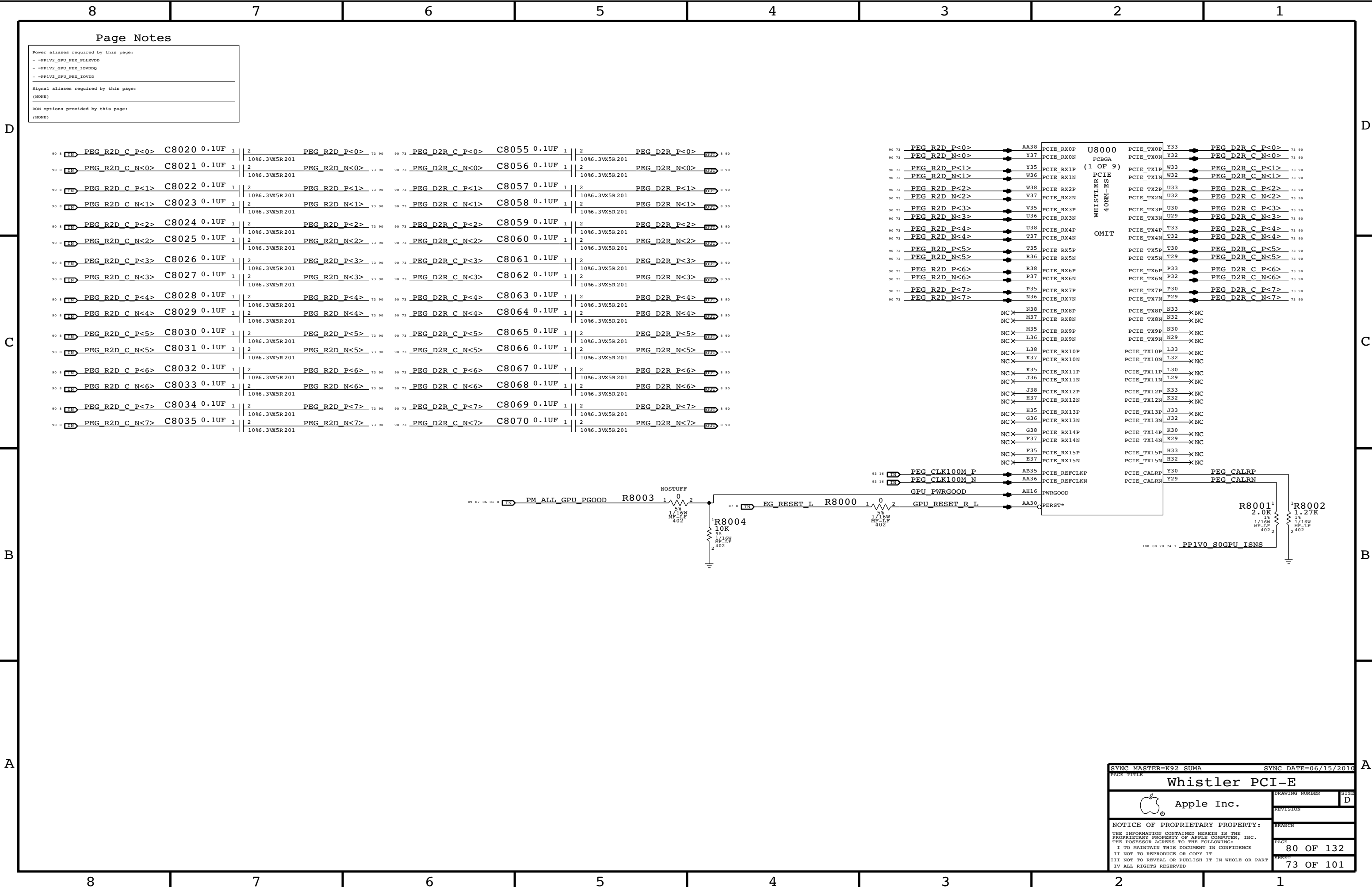
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8	7	6	5	4	3	2	1
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Page Notes

Power aliases required by this page:


- =PP1V2\_GPU\_PEX\_PLLXVDD
- =PP1V2\_GPU\_PEX\_IOVDDQ
- =PP1V2\_GPU\_PEX\_IOVDD

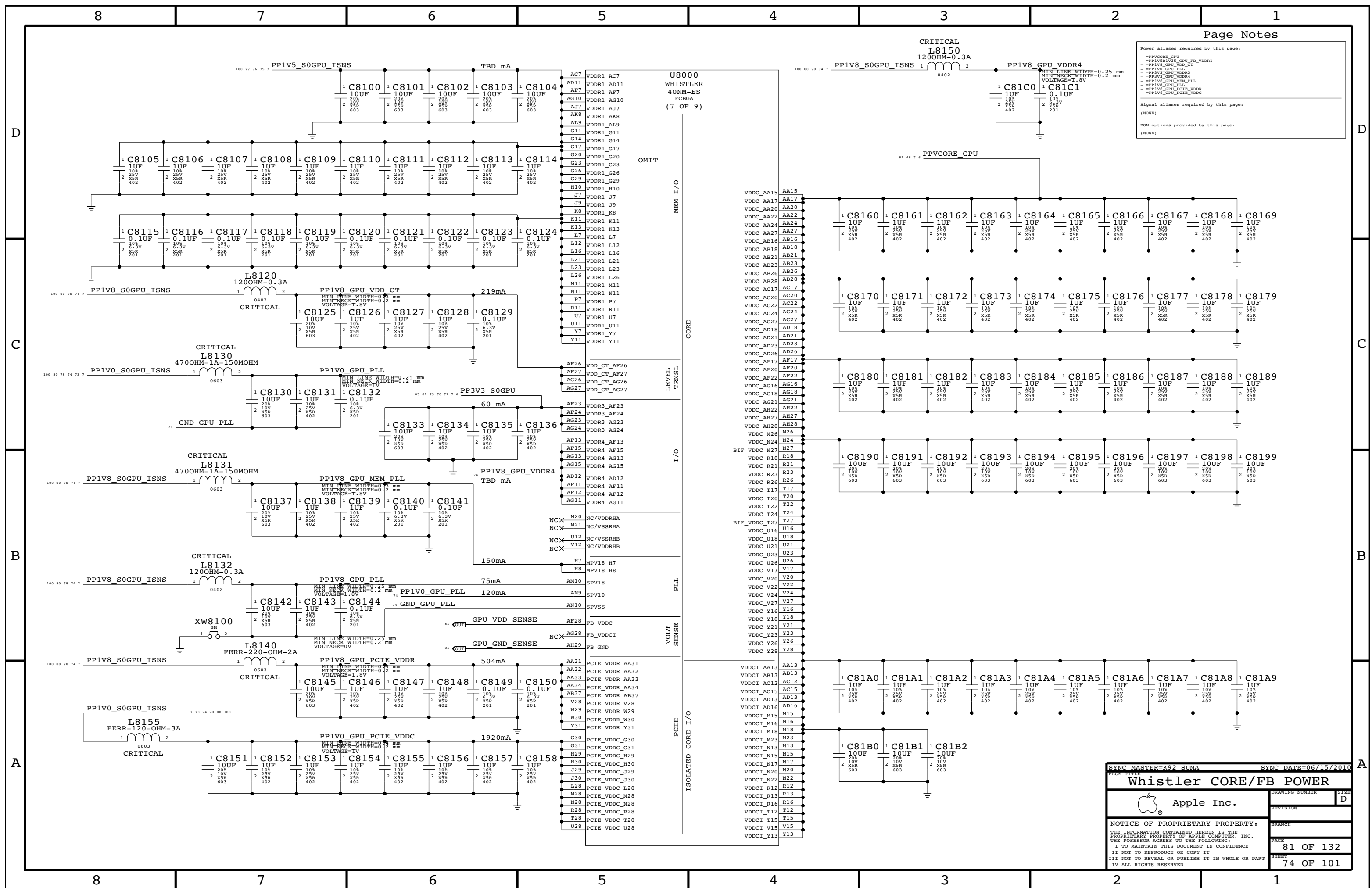
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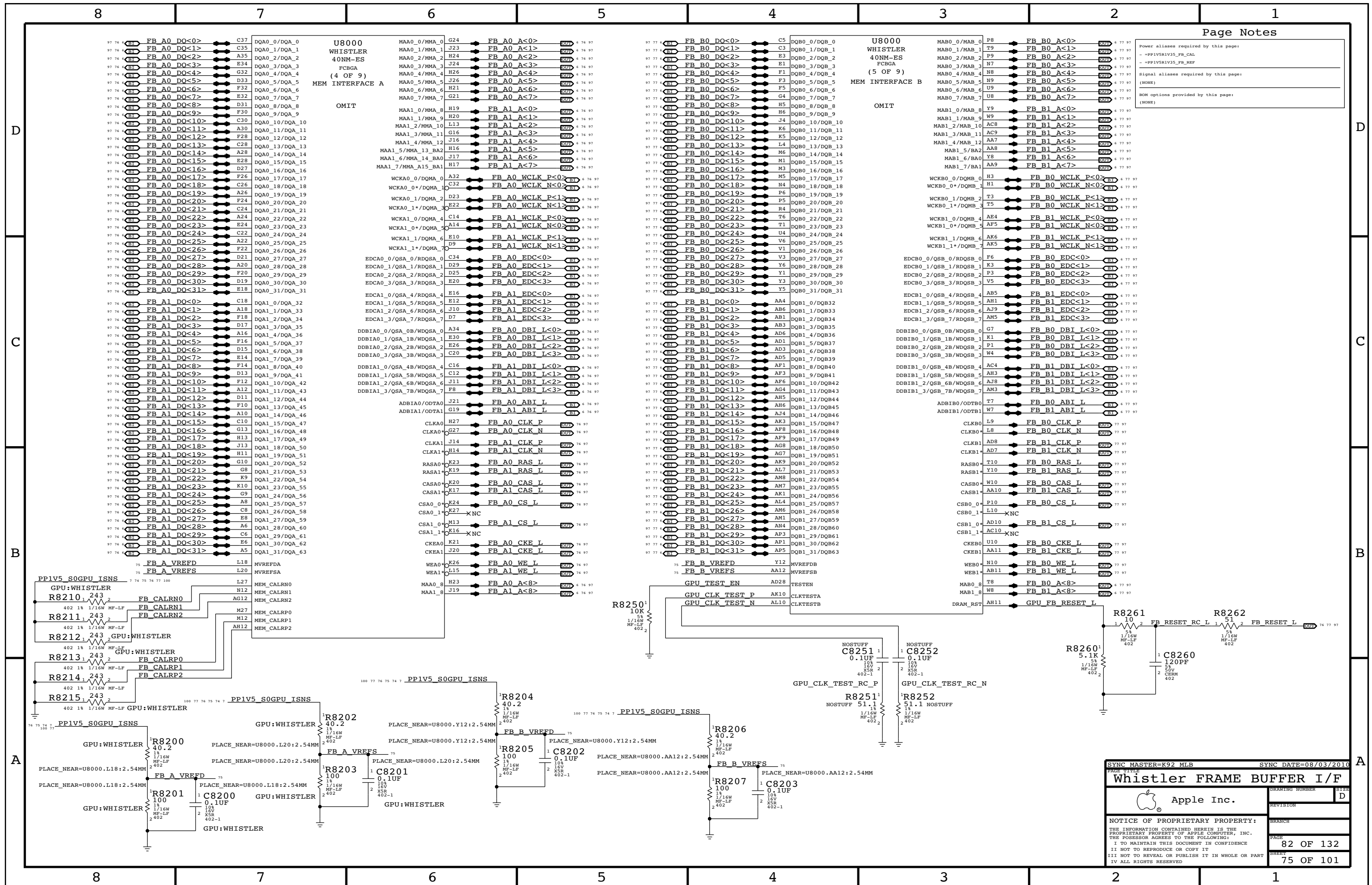
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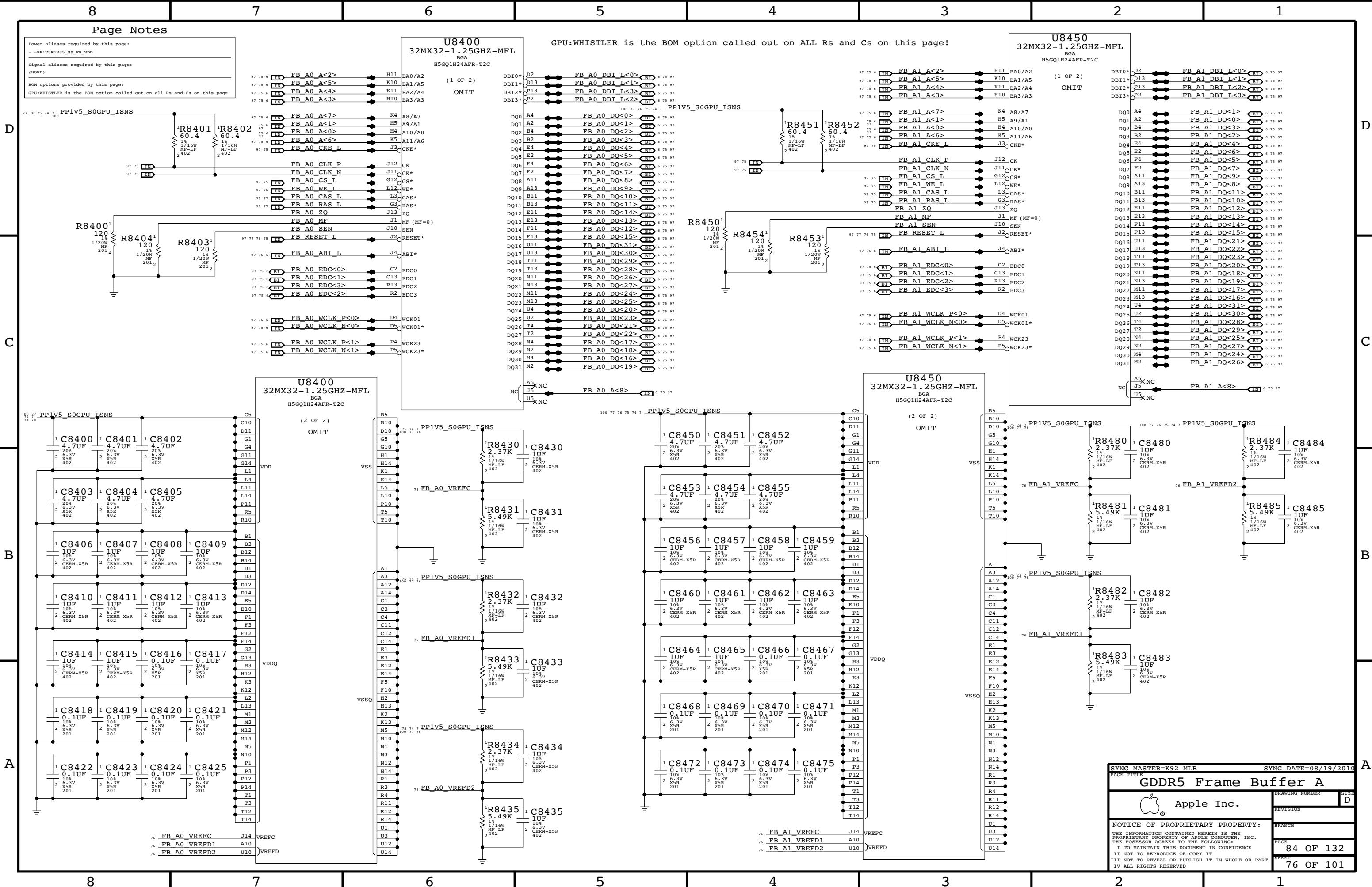
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Power aliases required by this page:  
- =PP1V5S0GPU\_ISNS

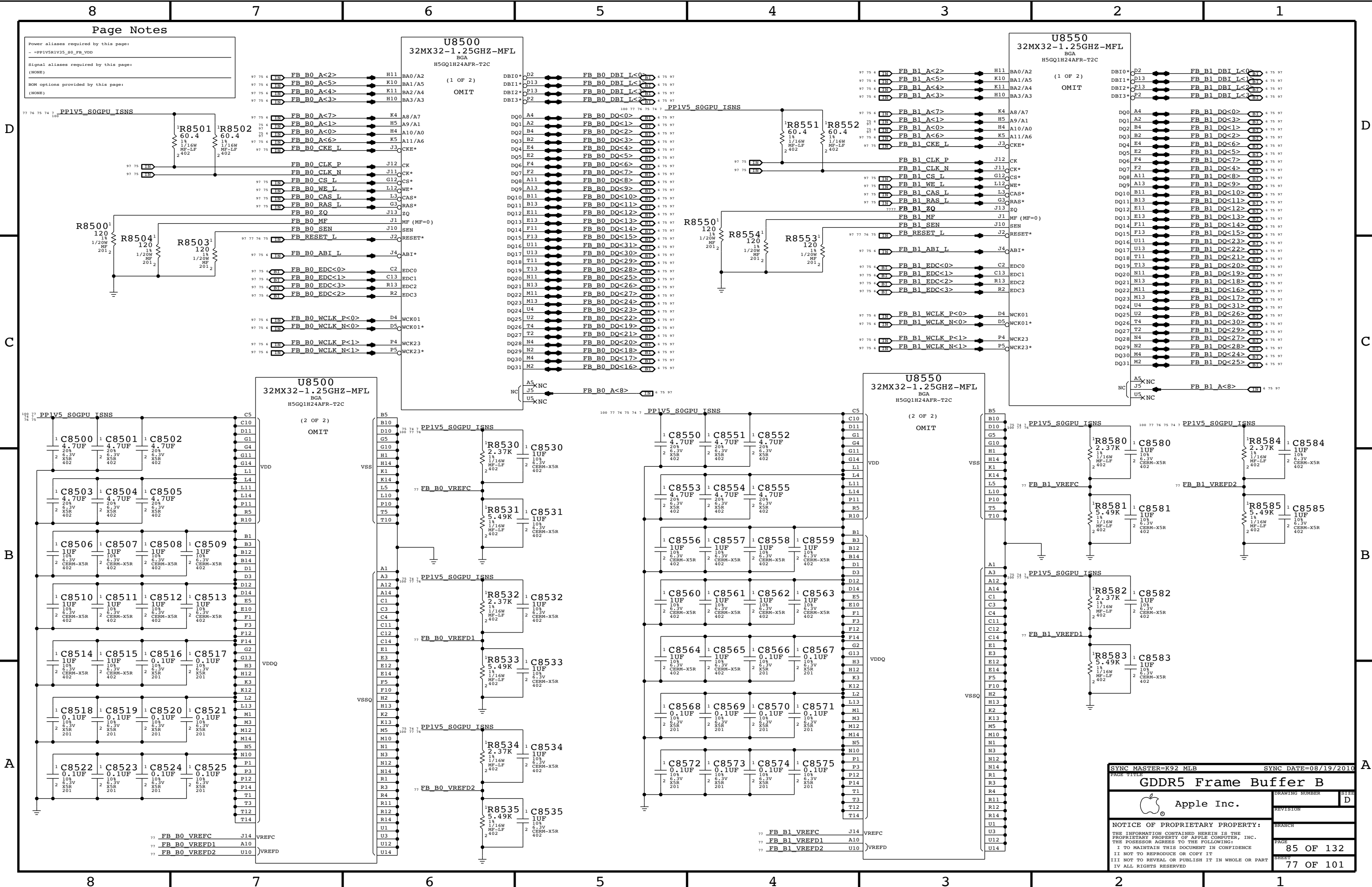
Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
GPU:WHISTLER is the BOM option called out on all Rs and Cs on this page

U8400  
32MX32-1.25GHZ-MFL  
BGA  
H5GQ1H24AFR-T2C  
(1 OF 2)  
OMIT

GPU:WHISTLER is the BOM option called out on ALL Rs and Cs on this page!

U8450  
32MX32-1.25GHZ-MFL  
BGA  
H5GQ1H24AFR-T2C  
(1 OF 2)  
OMIT



Page Notes

Power aliases required by this page:  
- PP1V5R1V35\_00\_FB\_VDD

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
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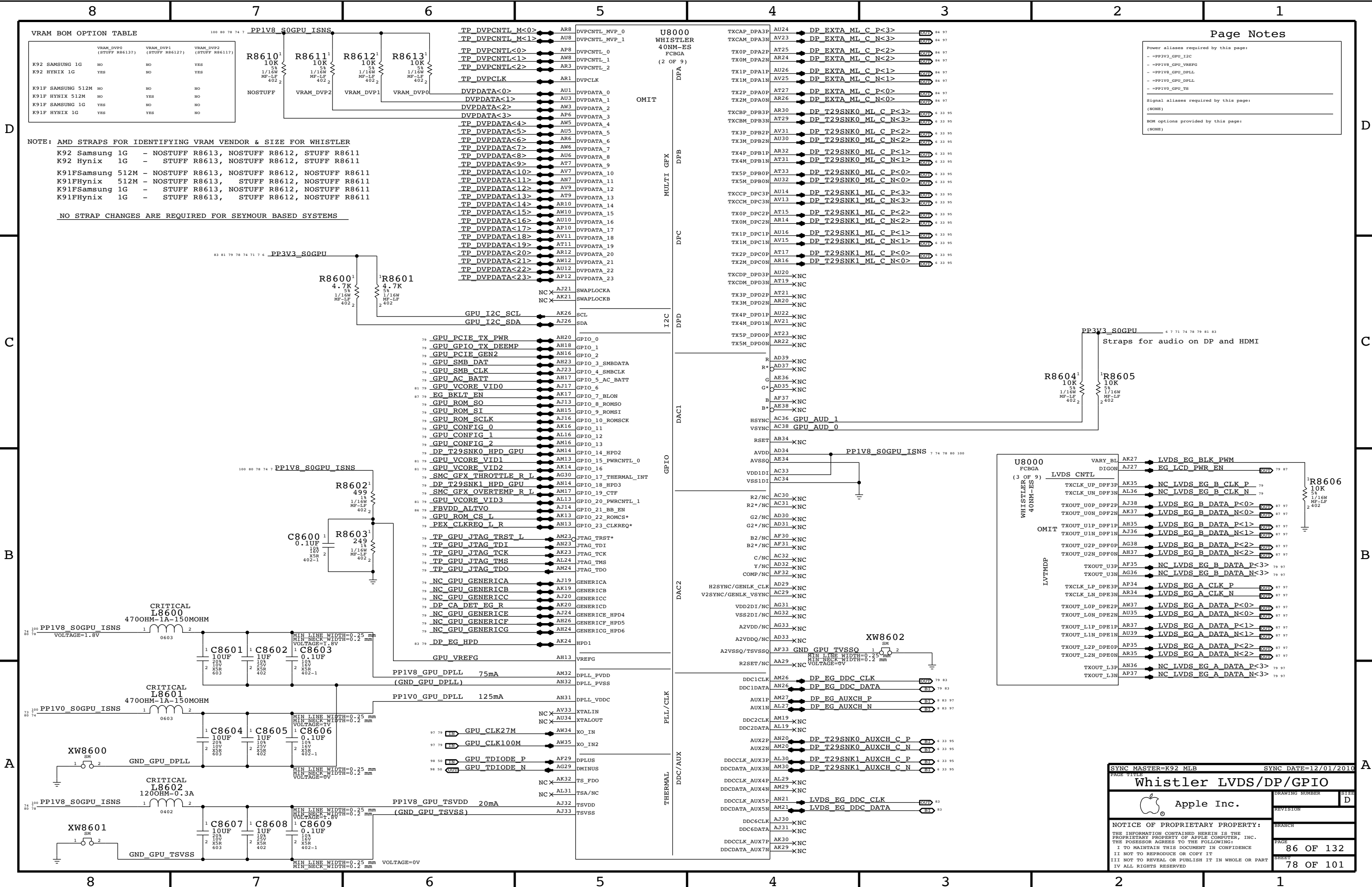
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32MX32-1.25GHZ-MFL  
BGA  
H5GQ1H24AFR-T2C  
(1 OF 2)  
OMIT

U8550  
32MX32-1.25GHZ-MFL  
BGA  
H5GQ1H24AFR-T2C  
(1 OF 2)  
OMIT

U8550  
32MX32-1.25GHZ-MFL  
BGA  
H5GQ1H24AFR-T2C  
(2 OF 2)  
OMIT

U8550  
32MX32-1.25GHZ-MFL  
BGA  
H5GQ1H24AFR-T2C  
(2 OF 2)  
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SYNC MASTER=K92 MLB		SYNC DATE=08/19/2010	
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GDDR5 Frame Buffer B			
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85 OF 132		77 OF 101	



VRAM BOM OPTION TABLE			
	VRAM_DVP0 (STUFF R8613?)	VRAM_DVP1 (STUFF R8612?)	VRAM_DVP2 (STUFF R8611?)
K92 SAMSUNG 1G	NO	NO	YES
K92 HYNIX 1G	YES	NO	YES
K91F SAMSUNG 512M	NO	NO	NO
K91F HYNIX 512M	NO	YES	NO
K91F SAMSUNG 1G	YES	NO	NO
K91F HYNIX 1G	YES	YES	NO

NOTE: AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611  
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

K91FSamsung 512M - NOSTUFF R8613, NOSTUFF R8612, NOSTUFF R8611  
K91FHynix 512M - NOSTUFF R8613, STUFF R8612, NOSTUFF R8611  
K91FSamsung 1G - STUFF R8613, NOSTUFF R8612, NOSTUFF R8611  
K91FHynix 1G - STUFF R8613, STUFF R8612, NOSTUFF R8611

NO STRAP CHANGES ARE REQUIRED FOR SEYMOUR BASED SYSTEMS

Page Notes

Power aliases required by this page:  
- PP3V3\_GPU\_I2C  
- PP1V8\_GPU\_VREFG  
- PP1V8\_GPU\_DPLL  
- PP1V0\_GPU\_DPLL  
- PP1V0\_GPU\_TS

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

SYNC MASTER=K92 MLB

SYNC DATE=12/01/2010

Whistler LVDS/DP/GPIO

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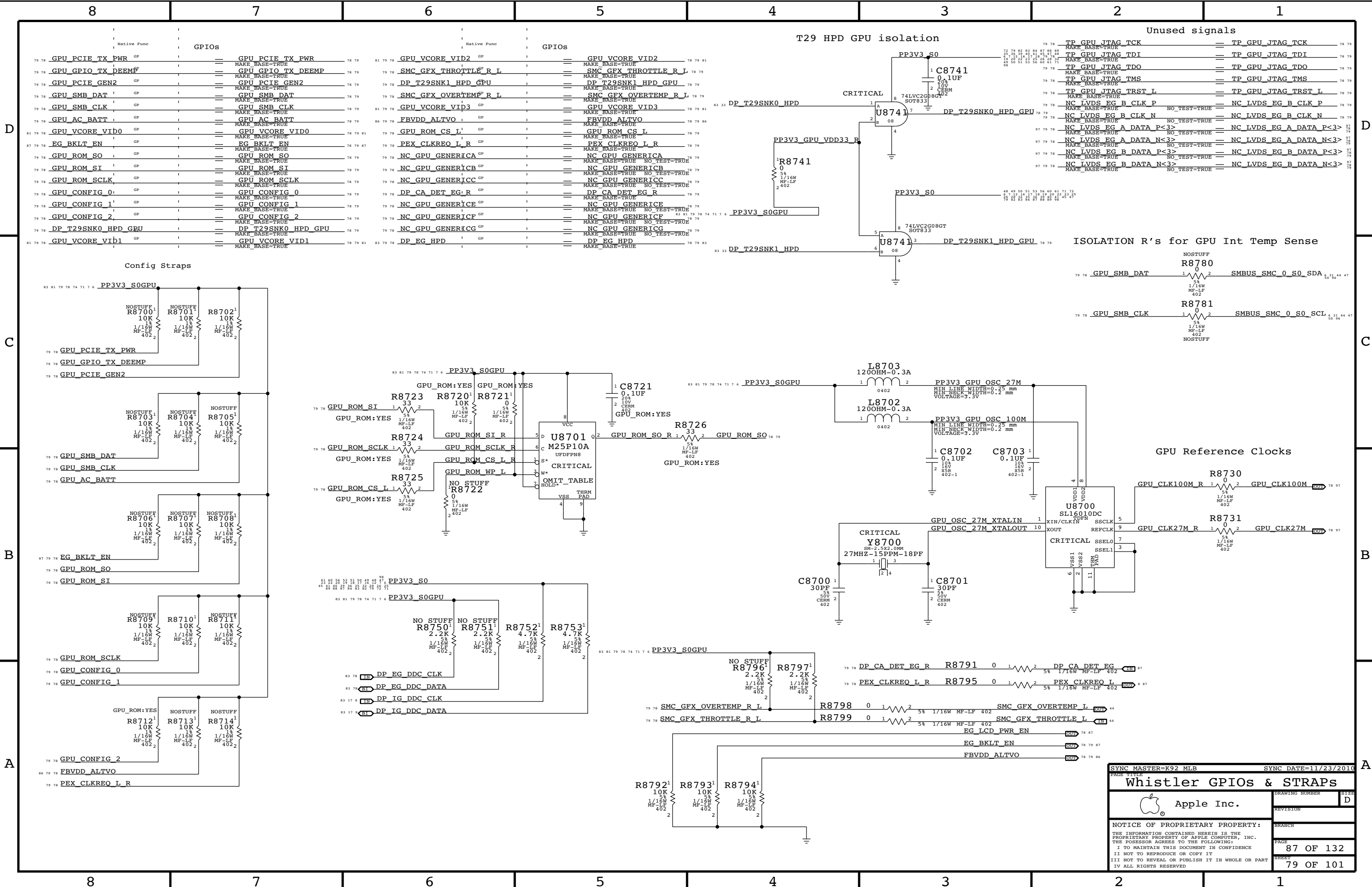
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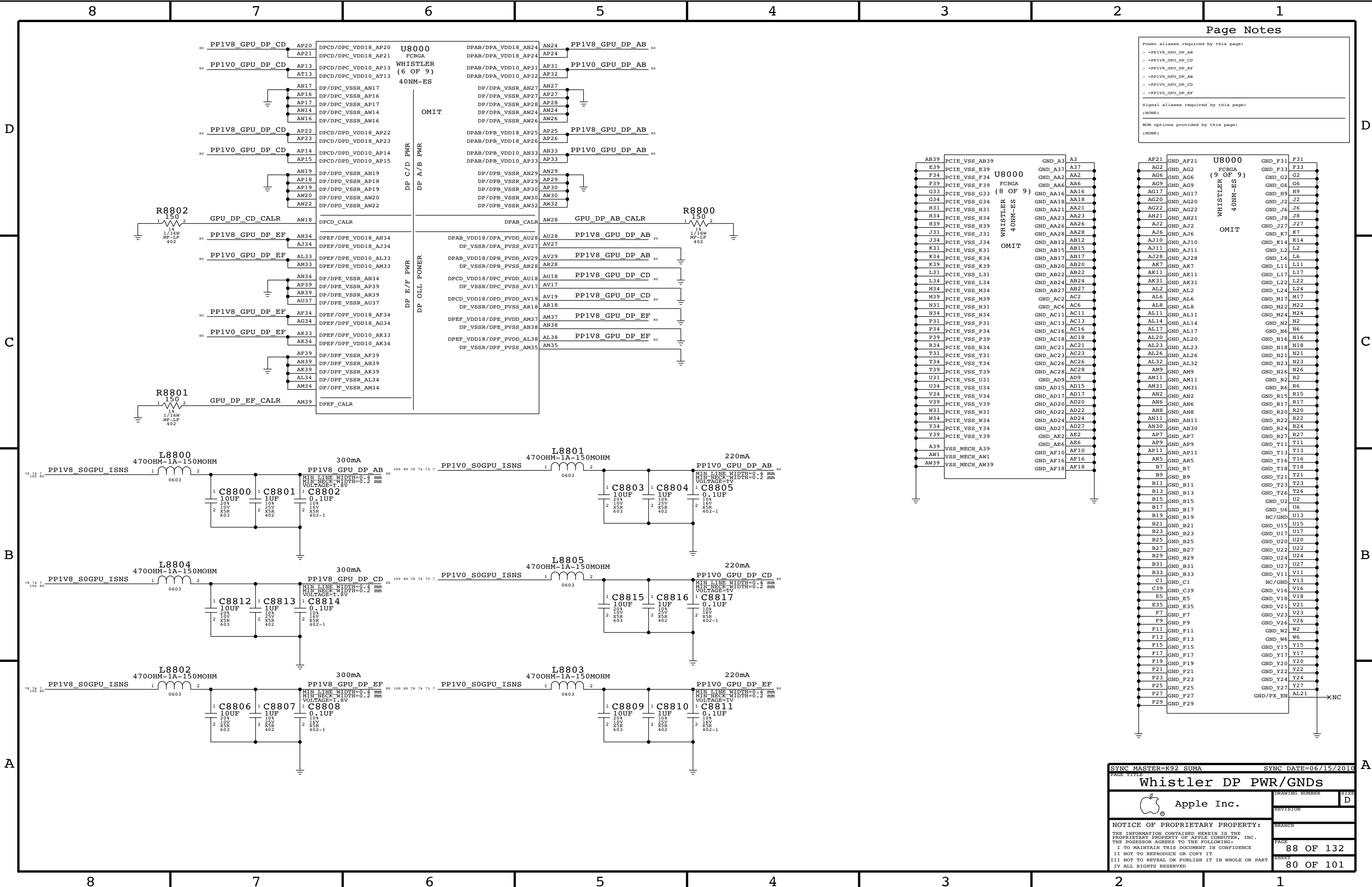
SIZE

D

86 OF 132

78 OF 101





Page Notes	
Power aliases required by this page:	
- ~PP1V8_GPU_DP_AB	
- ~PP1V8_GPU_DP_CD	
- ~PP1V8_GPU_DP_EF	
- ~PP1V0_GPU_DP_AB	
- ~PP1V0_GPU_DP_CD	
- ~PP1V0_GPU_DP_EF	
Signal aliases required by this page:	
(NONE)	
BOM options provided by this page:	
(NONE)	

AB39	PCIE_VSS_AB39	GND_A3	A3
E39	PCIE_VSS_E39	GND_A37	A37
F34	PCIE_VSS_F34	GND_AA2	AA2
F39	PCIE_VSS_F39	GND_AA6	AA6
G33	PCIE_VSS_G33	GND_AA16	AA16
G34	PCIE_VSS_G34	GND_AA18	AA18
H31	PCIE_VSS_H31	GND_AA21	AA21
H34	PCIE_VSS_H34	GND_AA23	AA23
H39	PCIE_VSS_H39	GND_AA26	AA26
J31	PCIE_VSS_J31	GND_AA28	AA28
J34	PCIE_VSS_J34	GND_AB12	AB12
K31	PCIE_VSS_K31	GND_AB15	AB15
K34	PCIE_VSS_K34	GND_AB17	AB17
K39	PCIE_VSS_K39	GND_AB20	AB20
L31	PCIE_VSS_L31	GND_AB22	AB22
L34	PCIE_VSS_L34	GND_AB24	AB24
M34	PCIE_VSS_M34	GND_AB27	AB27
M39	PCIE_VSS_M39	GND_AC2	AC2
N31	PCIE_VSS_N31	GND_AC6	AC6
N34	PCIE_VSS_N34	GND_AC11	AC11
P31	PCIE_VSS_P31	GND_AC13	AC13
P34	PCIE_VSS_P34	GND_AC16	AC16
P39	PCIE_VSS_P39	GND_AC18	AC18
R34	PCIE_VSS_R34	GND_AC21	AC21
T31	PCIE_VSS_T31	GND_AC23	AC23
T34	PCIE_VSS_T34	GND_AC26	AC26
T39	PCIE_VSS_T39	GND_AC28	AC28
U31	PCIE_VSS_U31	GND_AD9	AD9
U34	PCIE_VSS_U34	GND_AD15	AD15
V39	PCIE_VSS_V39	GND_AD17	AD17
W31	PCIE_VSS_W31	GND_AD20	AD20
W34	PCIE_VSS_W34	GND_AD22	AD22
Y34	PCIE_VSS_Y34	GND_AD24	AD24
Y39	PCIE_VSS_Y39	GND_AE2	AE2
A39	VSS_MECH_A39	GND_AE6	AE6
AW1	VSS_MECH_AW1	GND_AF10	AF10
AW39	VSS_MECH_AW39	GND_AF16	AF16
		GND_AF18	AF18

AF21	GND_AF21	U8000	GND_F31	F31
AG2	GND_AG2	(9 OF 9)	GND_F33	F33
AG6	GND_AG6	WHISTLER	GND_G2	G2
AG9	GND_AG9	40NM-ES	GND_G6	G6
AG17	GND_AG17	OMIT	GND_H9	H9
AG20	GND_AG20		GND_J2	J2
AG22	GND_AG22		GND_J6	J6
AH21	GND_AH21		GND_J8	J8
AJ2	GND_AJ2		GND_J27	J27
AJ6	GND_AJ6		GND_K7	K7
AJ10	GND_AJ10		GND_K14	K14
AJ11	GND_AJ11		GND_L2	L2
AJ28	GND_AJ28		GND_L6	L6
AK7	GND_AK7		GND_L11	L11
AK11	GND_AK11		GND_L17	L17
AK31	GND_AK31		GND_L22	L22
AL2	GND_AL2		GND_L24	L24
AL6	GND_AL6		GND_M17	M17
AL8	GND_AL8		GND_M22	M22
AL11	GND_AL11		GND_M24	M24
AL14	GND_AL14		GND_N2	N2
AL17	GND_AL17		GND_N6	N6
AL20	GND_AL20		GND_N16	N16
AL23	GND_AL23		GND_N18	N18
AL26	GND_AL26		GND_N21	N21
AL32	GND_AL32		GND_N23	N23
AM9	GND_AM9		GND_N26	N26
AM11	GND_AM11		GND_R2	R2
AM31	GND_AM31		GND_R6	R6
AN2	GND_AN2		GND_R15	R15
AN6	GND_AN6		GND_R17	R17
AN8	GND_AN8		GND_R20	R20
AN11	GND_AN11		GND_R22	R22
AN30	GND_AN30		GND_R24	R24
AP7	GND_AP7		GND_R27	R27
AP9	GND_AP9		GND_T11	T11
AP11	GND_AP11		GND_T13	T13
AR5	GND_AR5		GND_T16	T16
B7	GND_B7		GND_T18	T18
B9	GND_B9		GND_T21	T21
B11	GND_B11		GND_T23	T23
B13	GND_B13		GND_T26	T26
B15	GND_B15		GND_U2	U2
B17	GND_B17		GND_U6	U6
B19	GND_B19		NC/GND	U13
B21	GND_B21		GND_U15	U15
B23	GND_B23		GND_U17	U17
B25	GND_B25		GND_U20	U20
B27	GND_B27		GND_U22	U22
B29	GND_B29		GND_U24	U24
B31	GND_B31		GND_U27	U27
B33	GND_B33		GND_V11	V11
C1	GND_C1		NC/GND	V13
C39	GND_C39		GND_V16	V16
E5	GND_E5		GND_V18	V18
E35	GND_E35		GND_V21	V21
F7	GND_F7		GND_V23	V23
F9	GND_F9		GND_V26	V26
F11	GND_F11		GND_W2	W2
F13	GND_F13		GND_W6	W6
F15	GND_F15		GND_Y15	Y15
F17	GND_F17		GND_Y17	Y17
F19	GND_F19		GND_Y20	Y20
F21	GND_F21		GND_Y22	Y22
F23	GND_F23		GND_Y24	Y24
F25	GND_F25		GND_Y27	Y27
F27	GND_F27		GND/PX_EN	AL21
F29	GND_F29			

SYNC MASTER=K92 SUMA

SYNC DATE=06/15/2010

Whistler DP PWR/GNDs

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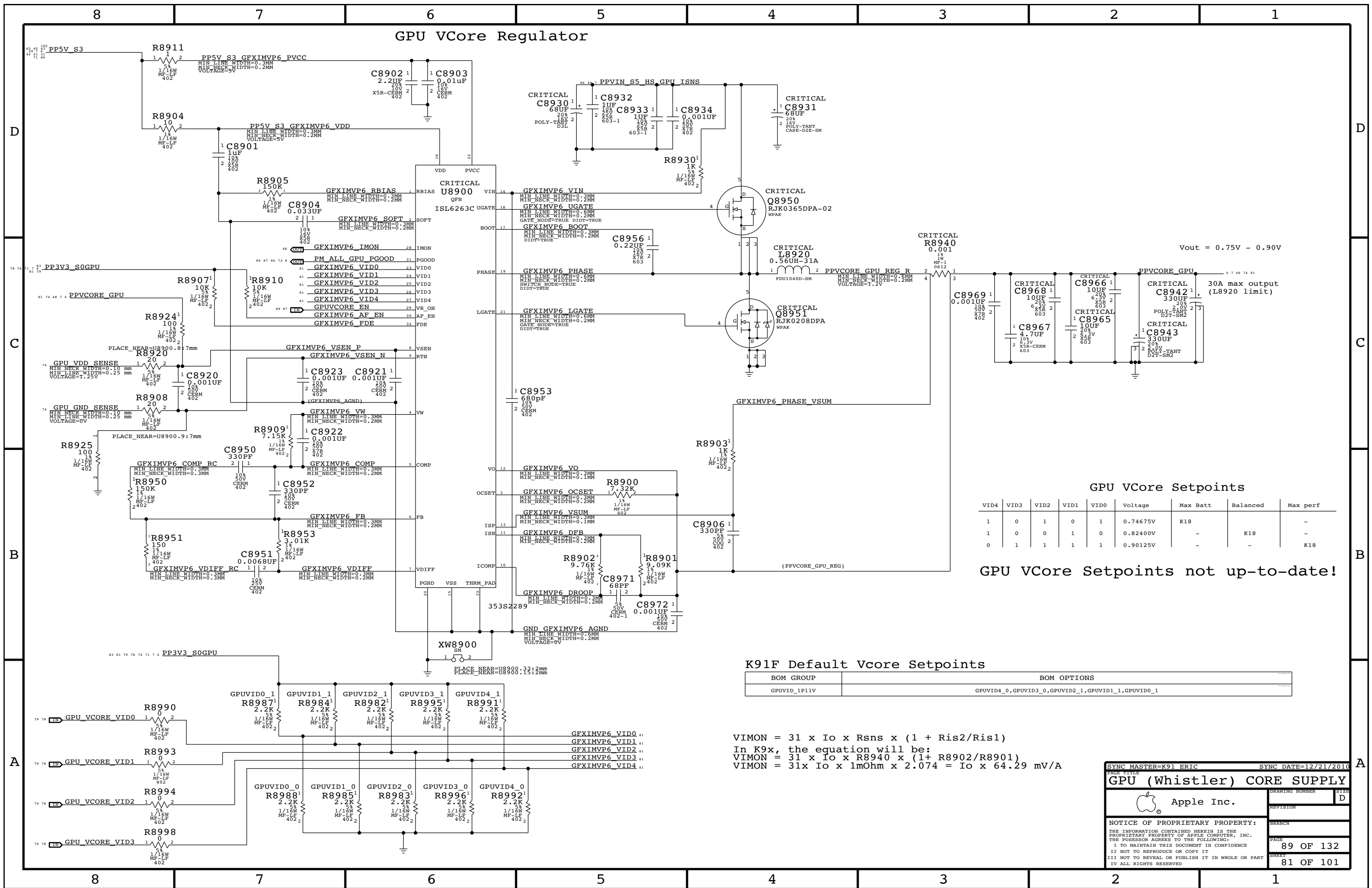
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88 OF 132


80 OF 101





GPU VCore Setpoints not up-to-date!

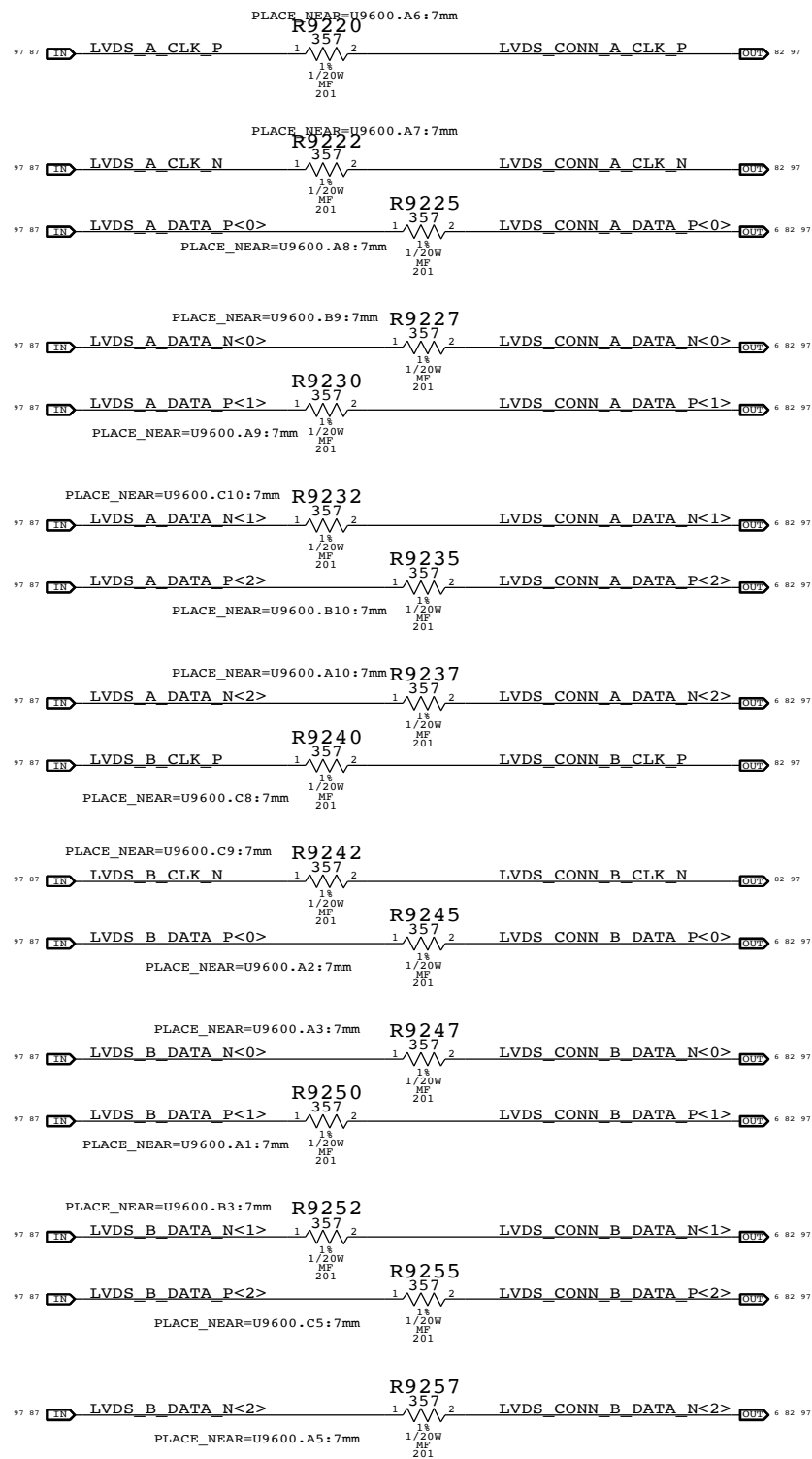
VIMON = 31 x Io x Rsns x (1 + Ris2/Ris1)  
In K9x, the equation will be:  
VIMON = 31 x Io x R8940 x (1+ R8902/R8901)  
VIMON = 31x Io x 1mOhm x 2.074 = Io x 64.29 mV/A

SYNCH MASTER=K91 ERIC		SYNCH DATE=12/21/2010	
PAGE TITLE			
GPU (Whistler)		CORE SUPPLY	
 Apple Inc.		DRAWING NUMBER	
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		PAGE	
		89 OF 132	
		SHEET	
		81 OF 101	

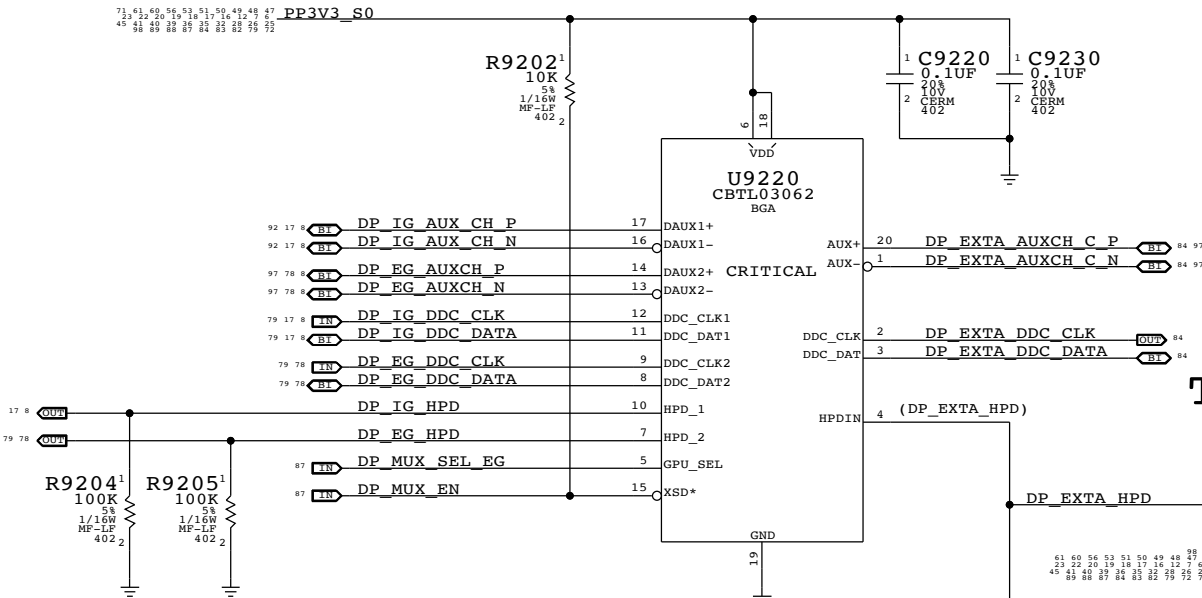


# LVDS Transmitter Termination

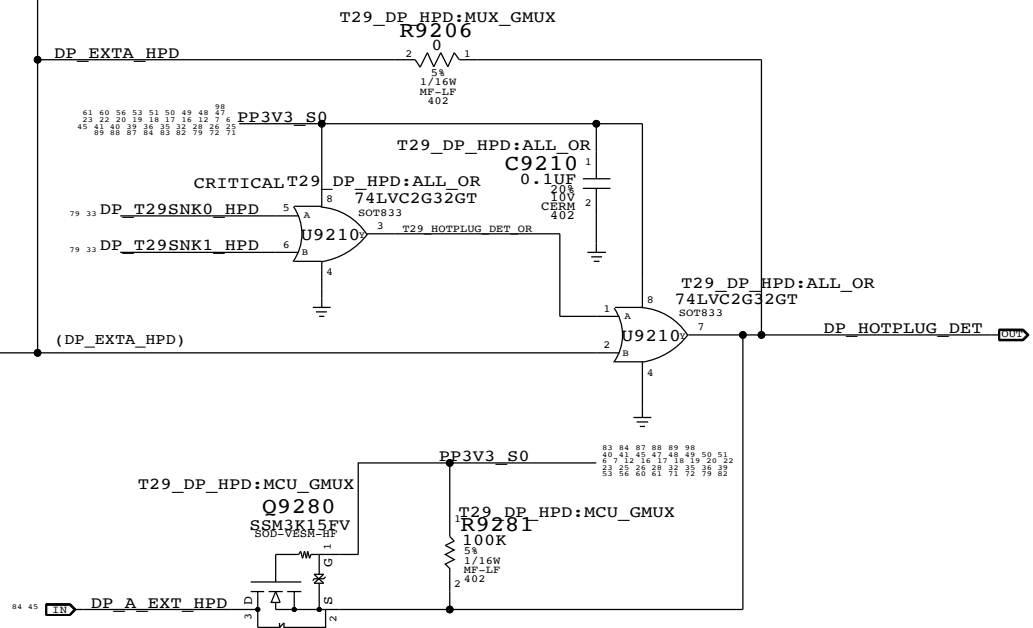
All emulated LVDS outputs require this termination



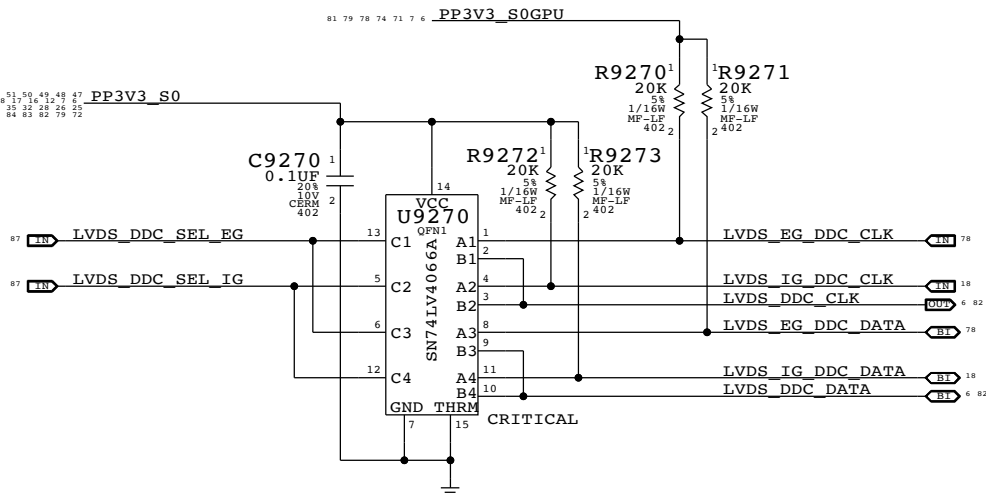
# DP AUX, DDC, & HPD muxing to IG/EG



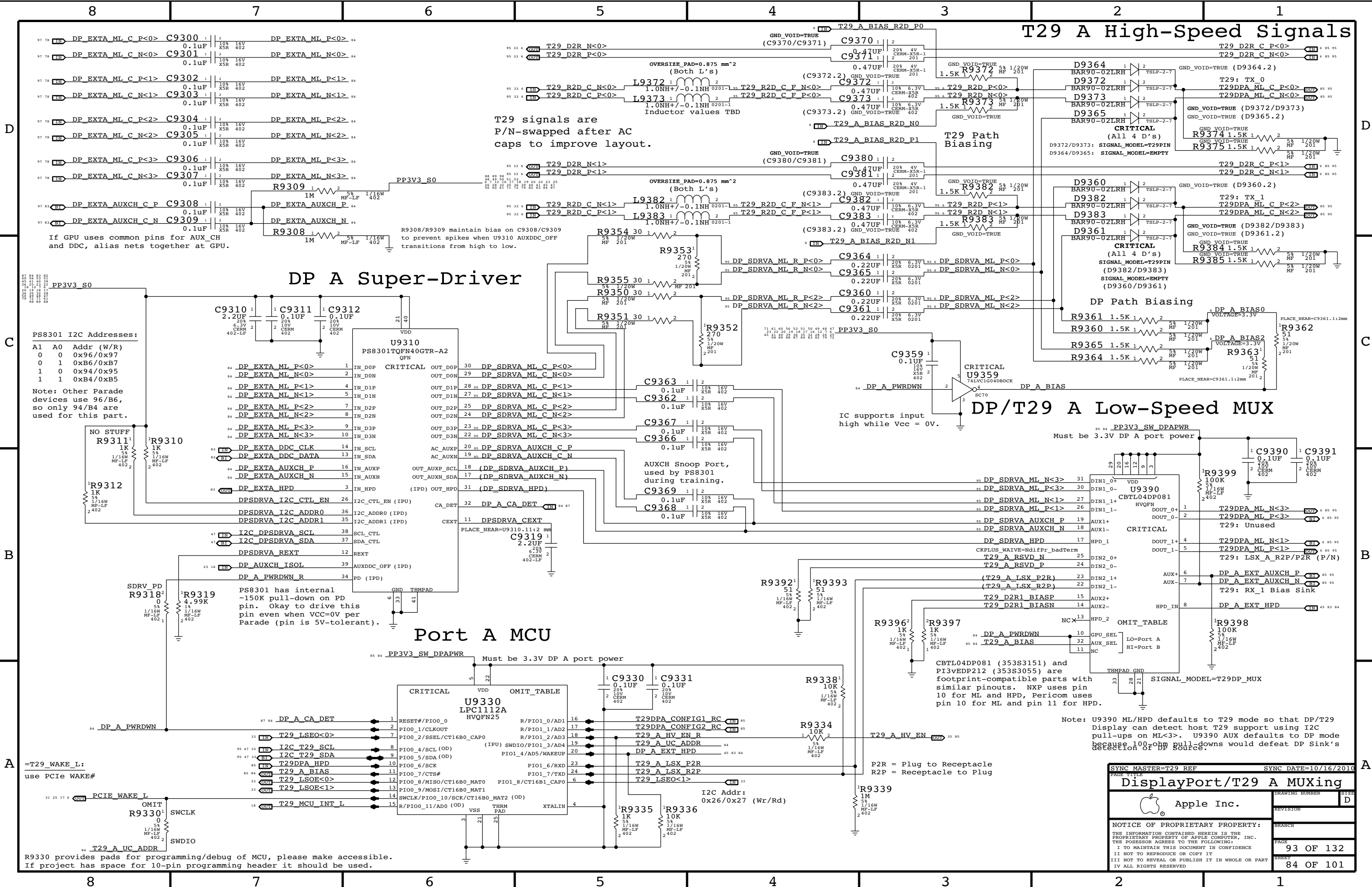
# T29/DP HOT PLUG IN

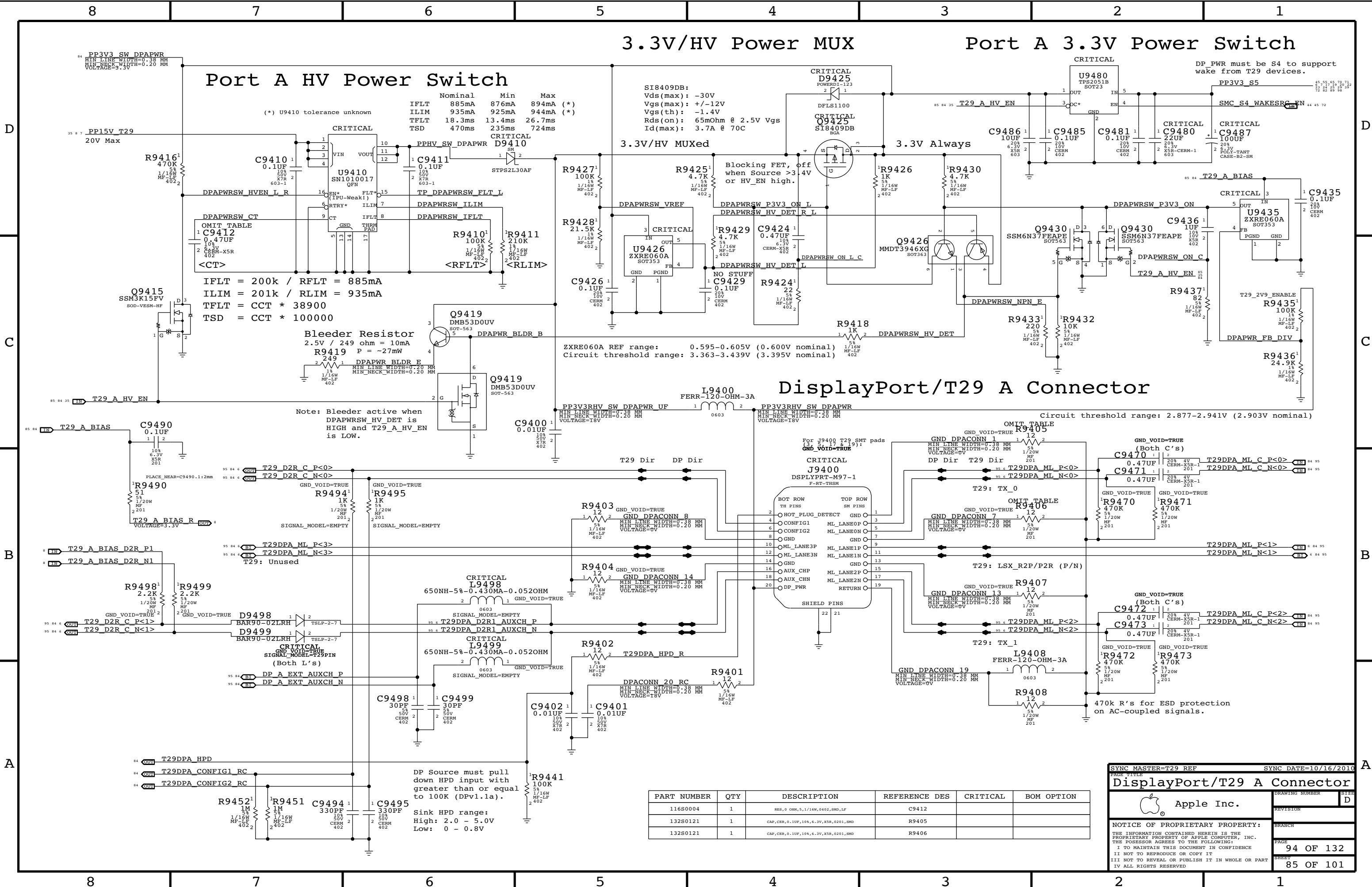


# LVDS DDC MUX



SYNC MASTER=K92 MLB		SYNC DATE=11/21/2010	
PAGE TITLE			
Muxed Graphics Support			
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3.3V/HV Power MUX

Port A 3.3V Power Switch

Port A HV Power Switch

DisplayPort/T29 A Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES, 0 OHM, 5, 1/16W, 0402, SMD, LF	C9412		
132S0121	1	CAP, CER, 0.1UF, 10%, 6.3V, X5R, 0201, SMD	R9405		
132S0121	1	CAP, CER, 0.1UF, 10%, 6.3V, X5R, 0201, SMD	R9406		

SYNC MASTER=T29 REF

SYNC DATE=10/16/2010

DisplayPort/T29 A Connector

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REVISION

BRANCH

PAGE

SHEET

SIZE

D

94 OF 132

85 OF 101

D

C

B

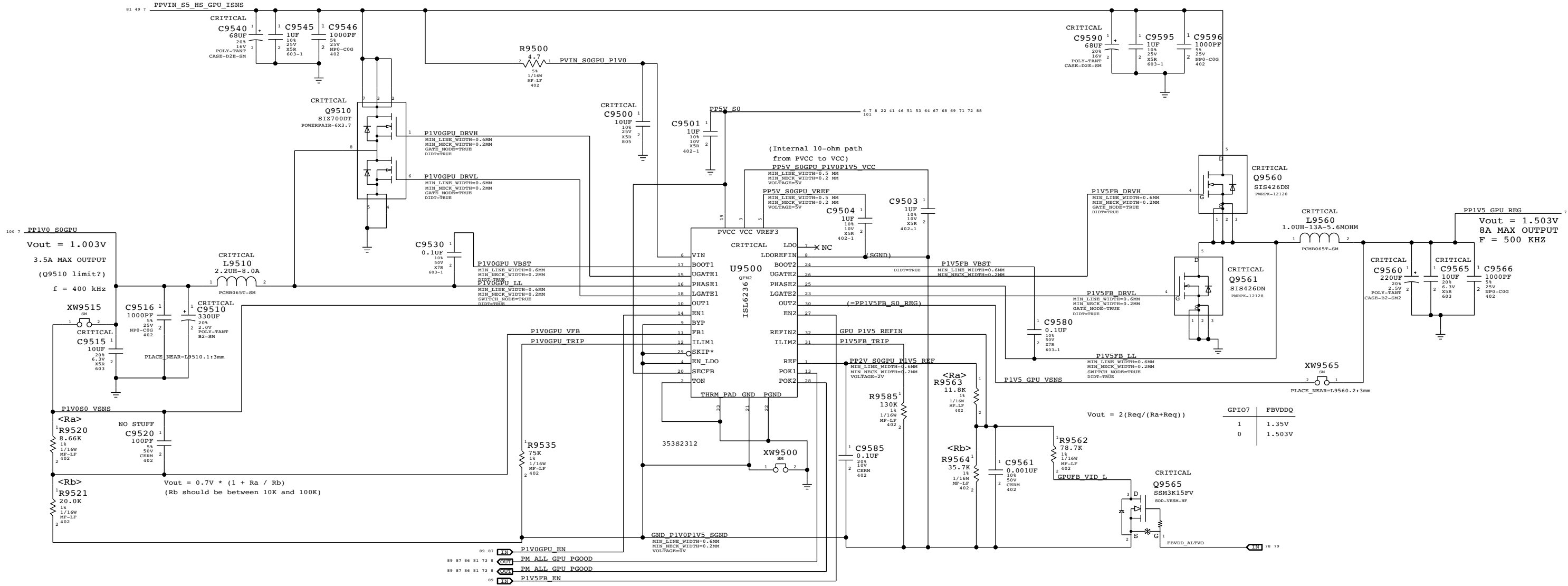
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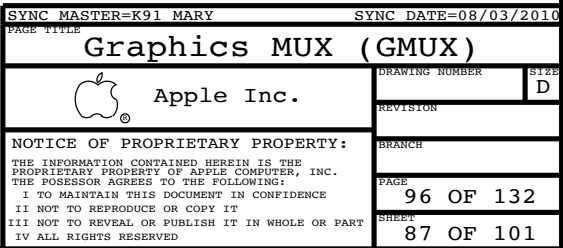
C

B

A



SYNC MASTER=K91 ERIC		SYNC DATE=10/08/2010	
PAGE TITLE			
1V0 GPU / 1V5 FB Power Supply			
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D

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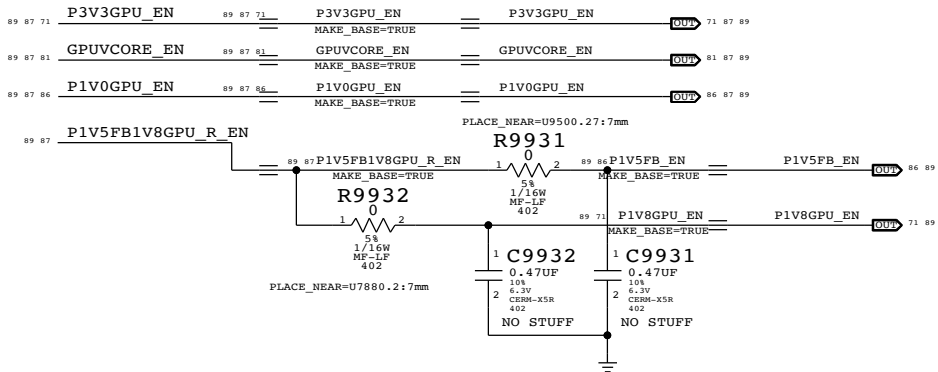
B

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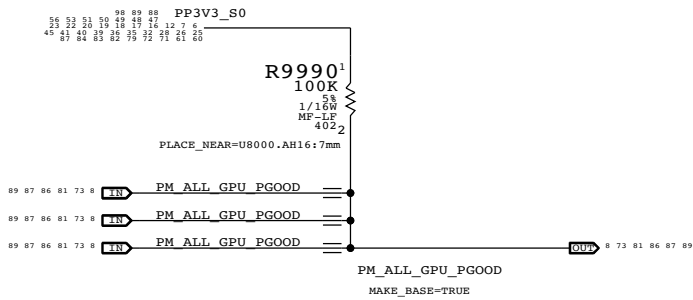
GPU Rail Sequencing

Whistler GPU requires rails to come up in the following order:

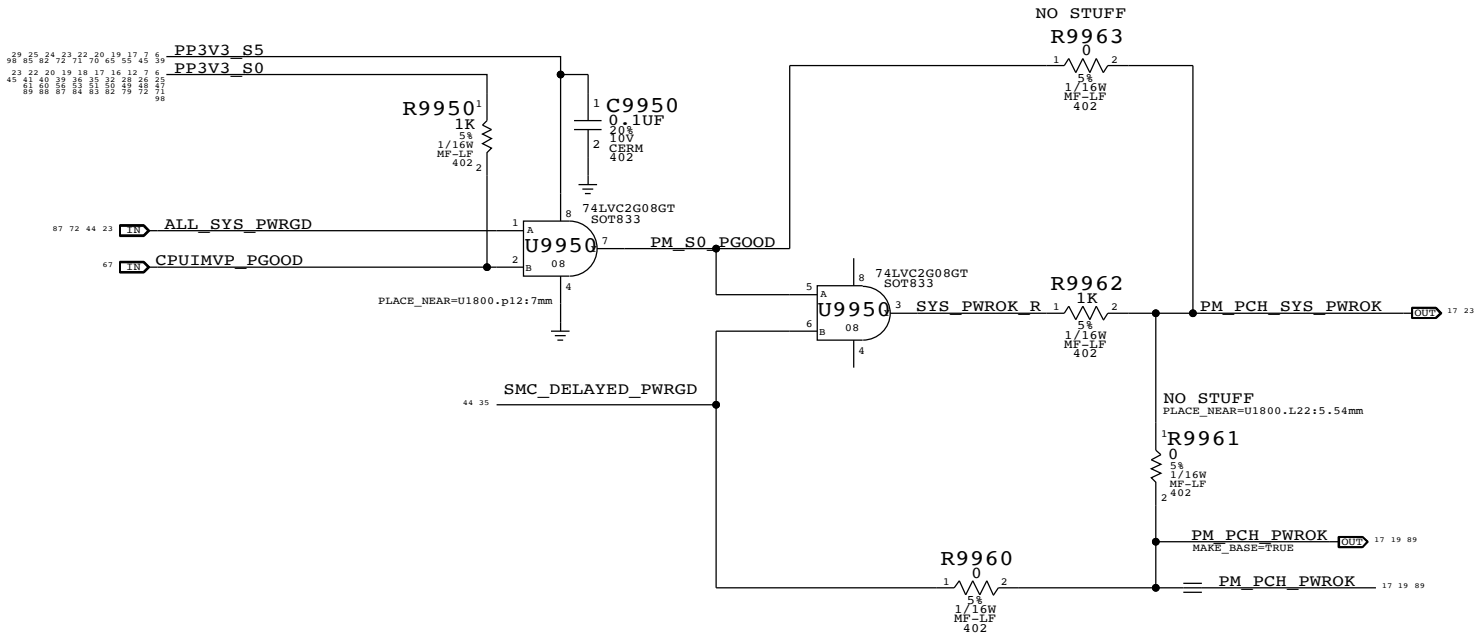
- 1) GPU\_3.3V
- 2) GPUVcore
- 3) GPU\_1.0V
- 4) GPU\_1.8V;GDDR5 1.5/1.35V



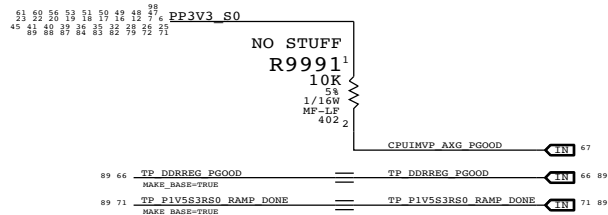
EXT GPU PWRGD Pullup



PCH S0 PWRGD



Unused PGOOD signal



SYNC MASTER=K91 MARY		SYNC DATE=08/03/2010	
PAGE TITLE		Power Sequencing EG/PCH S0	
		DRAWING NUMBER	SIZE
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		99 OF 132	89 OF 101



8

7

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1

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING\_RULE\_SET

LAYER

LINE-TO-LINE SPACING

WEIGHT

MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_QS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_QS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_QS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_QS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_QS	MEM_CLK	*	MEM_QS2MEM
MEM_QS	MEM_CTRL	*	MEM_QS2MEM
MEM_QS	MEM_CMD	*	MEM_QS2MEM
MEM_QS	MEM_DATA	*	MEM_QS2MEM
MEM_QS	MEM_QS	*	MEM_QS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20OTHER
MEM_CTRL	*	*	MEM_20OTHER
MEM_CMD	*	*	MEM_20OTHER
MEM_DATA	*	*	MEM_20OTHER
MEM_QS	*	*	MEM_20OTHER

Need to support MEM\_\*-style wildcards!

DDR3:

DQ/DM signals should be matched within 0.508mm of associated DQS pair.

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.

CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.

DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK P<5..0>	6 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK N<5..0>	6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	6 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	6 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	6 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	6 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	6 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	6 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	6 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	6 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	6 11 27
MEM_A_DQS0	MEM_85D	MEM_QS	MEM_A_DQS P<0>	6 11 27
MEM_A_DQS0	MEM_85D	MEM_QS	MEM_A_DQS N<0>	6 11 27
MEM_A_DQS1	MEM_85D	MEM_QS	MEM_A_DQS P<1>	6 11 27
MEM_A_DQS1	MEM_85D	MEM_QS	MEM_A_DQS N<1>	6 11 27
MEM_A_DQS2	MEM_85D	MEM_QS	MEM_A_DQS P<2>	6 11 27
MEM_A_DQS2	MEM_85D	MEM_QS	MEM_A_DQS N<2>	6 11 27
MEM_A_DQS3	MEM_85D	MEM_QS	MEM_A_DQS P<3>	6 11 27
MEM_A_DQS3	MEM_85D	MEM_QS	MEM_A_DQS N<3>	6 11 27
MEM_A_DQS4	MEM_85D	MEM_QS	MEM_A_DQS P<4>	6 11 27
MEM_A_DQS4	MEM_85D	MEM_QS	MEM_A_DQS N<4>	6 11 27
MEM_A_DQS5	MEM_85D	MEM_QS	MEM_A_DQS P<5>	6 11 27
MEM_A_DQS5	MEM_85D	MEM_QS	MEM_A_DQS N<5>	6 11 27
MEM_A_DQS6	MEM_85D	MEM_QS	MEM_A_DQS P<6>	6 11 26 27
MEM_A_DQS6	MEM_85D	MEM_QS	MEM_A_DQS N<6>	6 11 26 27
MEM_A_DQS7	MEM_85D	MEM_QS	MEM_A_DQS P<7>	6 11 27
MEM_A_DQS7	MEM_85D	MEM_QS	MEM_A_DQS N<7>	6 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK P<5..0>	6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK N<5..0>	6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	6 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	6 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	6 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	6 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	6 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	6 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	6 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	6 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	6 11 27
MEM_B_DQS0	MEM_85D	MEM_QS	MEM_B_DQS P<0>	6 11 27
MEM_B_DQS0	MEM_85D	MEM_QS	MEM_B_DQS N<0>	6 11 27
MEM_B_DQS1	MEM_85D	MEM_QS	MEM_B_DQS P<1>	6 11 27
MEM_B_DQS1	MEM_85D	MEM_QS	MEM_B_DQS N<1>	6 11 27
MEM_B_DQS2	MEM_85D	MEM_QS	MEM_B_DQS P<2>	6 11 27
MEM_B_DQS2	MEM_85D	MEM_QS	MEM_B_DQS N<2>	6 11 27
MEM_B_DQS3	MEM_85D	MEM_QS	MEM_B_DQS P<3>	6 11 27
MEM_B_DQS3	MEM_85D	MEM_QS	MEM_B_DQS N<3>	6 11 27
MEM_B_DQS4	MEM_85D	MEM_QS	MEM_B_DQS P<4>	6 11 27
MEM_B_DQS4	MEM_85D	MEM_QS	MEM_B_DQS N<4>	6 11 27
MEM_B_DQS5	MEM_85D	MEM_QS	MEM_B_DQS P<5>	6 11 27
MEM_B_DQS5	MEM_85D	MEM_QS	MEM_B_DQS N<5>	6 11 27
MEM_B_DQS6	MEM_85D	MEM_QS	MEM_B_DQS P<6>	6 11 27 28
MEM_B_DQS6	MEM_85D	MEM_QS	MEM_B_DQS N<6>	6 11 27 28
MEM_B_DQS7	MEM_85D	MEM_QS	MEM_B_DQS P<7>	6 11 27
MEM_B_DQS7	MEM_85D	MEM_QS	MEM_B_DQS N<7>	6 11 27

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Memory Constraints

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DRAWING NUMBER

REVISION

BRANCH

PAGE

SHEET

101 OF 132

91 OF 101

8

7

6

5

4

3

2

1



## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

## SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?


## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

## PCH Net Properties

ELECTRICAL-CONSTRAINT_SET		PHYSICAL		NET_TYPE	SPACING
	LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 44 46 87
	LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 44 46 87
	LPC_RESET_L	LPC_50S	LPC	LPCLPLUS RESET_L	6 25 46 87
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
		CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 44
		CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCLPLUS	6 25 46
	SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 23 26 28 30 41 47 61 88
	SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 23 26 28 30 41 47 61 88
	SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 47
	SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 47
	SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 47
	SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 47
	HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 56
		HDA_50S	HDA	HDA_BIT_CLK_R	16
	HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 56
		HDA_50S	HDA	HDA_SYNC_R	16
	HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
		HDA_50S	HDA	HDA_RST_L	16 56
	HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 56
		HDA_50S	HDA	AUD_SDI_R	56
	HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 56
		HDA_50S	HDA	HDA_SDOUT_R	16
	SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 46
		SPI_55S	SPI	SPI_CLK	46
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 46
		SPI_55S	SPI	SPI_MOSI	46
	SPI_MISO	SPI_55S	SPI	SPI_MISO	16 46
	SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 46
		SPI_55S	SPI	SPI_CS0_L	46
		PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
		PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
		PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
		PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
		PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
		PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
		PCIE_85D	PCIE	PCIE_AP_R2D_P	6 31
		PCIE_85D	PCIE	PCIE_AP_R2D_N	6 31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 31
		PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 31
		PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 31
		PCIE_85D	PCIE	PCIE_FW_R2D_P	38
		PCIE_85D	PCIE	PCIE_FW_R2D_N	38
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
		PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
		PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
		PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
		PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
1620		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
1630		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
1640	PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
1650		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33
1660		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
1670		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
1680		CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
1690		CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
1700		CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
1710		CPU_50S	CLK_PCIE	PCH_CLK33M_PCITIN	16 25
	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 73
		CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 73
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 31
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 31
	PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
	PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 16
		CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 16
1720	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 9 33
1730	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 9 33
1740	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	33
1750	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	33
1760	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 9 33
1770	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 9 33
1780	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
1790	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33

SYNC MASTER=K92 MLB		SYNC DATE=08/09/2010	
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PCH Constraints 2			
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		BRANCH	
		PAGE	103 OF 132
		SHEET	93 OF 101



## DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

## T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

## T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

## T29/DP Connector Signal Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?	T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

## T29 IC Net Properties


ELECTRICAL_CONSTRAINT_SET		NET TYPE		
		PHYSICAL	SPACING	
		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0> 6 33 78
		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0> 6 33 78
	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0> 6 33
	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0> 6 33
		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P 6 33
		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N 6 33 78
	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P 6 33
	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N 6 33
		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0> 6 33 78
		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0> 6 33 78
	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0> 6 33
	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0> 6 33
		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P 6 33 78
		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N 6 33 78
	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P 6 33
	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N 6 33
		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0> 6 33 78
		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0> 6 33 78
		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P 6 33
		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N 6 33
		T29_I2C_55S	T29_I2C	I2C_T29_SCL 33 47 84
		T29_I2C_55S	T29_I2C	I2C_T29_SDA 33 47 84
	T29_SPT_CLK	T29_SPT_55S	T29_SPT	T29_SPT_CLK 33
	T29_SPT_MOSI	T29_SPT_55S	T29_SPT	T29_SPT_MOSI 33
	T29_SPT_MISO	T29_SPT_55S	T29_SPT	T29_SPT_MISO 33
	T29_SPT_CS_L	T29_SPT_55S	T29_SPT	T29_SPT_CS_L 33
		T29DP_80D	T29DP	T29_R2D_C_P<3..0> 6 33 80
		T29DP_80D	T29DP	T29_R2D_C_N<3..0> 6 33 80
		T29DP_100D	T29DP	T29_D2R_P<3..0> 6 33 80
		T29DP_100D	T29DP	T29_D2R_N<3..0> 6 33 80

Only used on hosts supporting T29 video-in

## T29/DP Net Properties


ELECTRICAL CONSTRAINT_SET		NET TYPE		
		PHYSICAL	SPACING	
T29_R2D0	T29DP_80D	T29DP	T29_R2D P<0>	6 84
T29_R2D0	T29DP_80D	T29DP	T29_R2D N<0>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D P<1>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D N<1>	6 84
	T29DP_80D	T29DP	T29_R2D C F P<1..0>	84
	T29DP_80D	T29DP	T29_R2D C F N<1..0>	84
T29_D2R0	T29DP_100D	T29DP	T29_D2R C P<0>	6 84 85
T29_D2R0	T29DP_100D	T29DP	T29_D2R C N<0>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R C P<1>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R C N<1>	6 84 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	84
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 84 95
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 84 95
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	84
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	84
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	84 85
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	84 85
T29_R2D2	T29DP_80D	T29DP	T29_R2D P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D N<3>	
	T29DP_80D	T29DP	T29_R2D C F P<3..2>	
	T29DP_80D	T29DP	T29_R2D C F N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R C P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R C N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R C P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R C N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	95
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	95
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

SYNCH MASTER=T29 REF		SYNCH DATE=10/16/2010	
PAGE TITLE			
T29 Constraints			
 Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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		SHEET 95 OF 101	

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
□	SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 31 44 47 53 54
□	SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 31 44 47 53 54
□	SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 44 47 50
□	SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 44 47 50
□	SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 6 31 44 47 50 79
□	SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 6 31 44 47 50 79
□	SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 44 47 62 63
□	SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 44 47 62 63
□	SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 44 47 100
□	SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 44 47 100

SMBus Charger Net Properties			
		NET_TYPE	
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P
	1T01_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P
	1T01_DIFFPAIR		CHGR_CSO_N

SYNCH MASTER=K18 MLB		SYNCH DATE=04/27/2010	
PAGE TITLE			
SMC Constraints			
 Apple Inc.		DRAWING NUMBER	
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		106 OF 132	
		SHEET	
		96 OF 101	



## GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

## Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.  
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.  
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.  
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.  
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.





















## GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		PHYSICAL	SPACING	
	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P 75 76
	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N 75 76
	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P 75 76
	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0> 6 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0> 6 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L 6 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L 6 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L 75 76
	FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0> 6 75 76
1230	FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1> 6 75 76
1230	FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2> 6 75 76
1230	FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3> 6 75 76
1230	FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0> 6 75 76
1230	FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1> 6 75 76
1230	FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2> 6 75 76
1230	FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3> 6 75 76
1230	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0> 6 75 76
1230	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1> 6 75 76
1300	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2> 6 75 76
1300	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3> 6 75 76
1300	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0> 6 75 76
1300	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1> 6 75 76
1300	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2> 6 75 76
1300	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3> 6 75 76
	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0> 6 75 76
	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0> 6 75 76
	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1> 6 75 76
	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1> 6 75 76
	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0> 6 75 76
	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0> 6 75 76
	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1> 6 75 76
	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1> 6 75 76
	FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0> 6 75 76
	FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..8> 6 75 76
	FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16> 6 75 76
	FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24> 6 75 76
	FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0> 6 75 76
	FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..8> 6 75 76
	FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16> 6 75 76
	FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24> 6 75 76
	FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L 75 76 77

## GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		SPACING	
		PHYSICAL	SPACING		
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	75 77
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	75 77
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	75 77
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	6 75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	6 75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	6 75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	6 75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	75 77
	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	6 75 77
1810	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	6 75 77
1810	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	6 75 77
1810	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	6 75 77
1810	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	6 75 77
1810	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	6 75 77
1810	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	6 75 77
1810	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	6 75 77
1810	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	6 75 77
1810	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	6 75 77
1810	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	6 75 77
1810	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	6 75 77
1810	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	6 75 77
1810	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	6 75 77
1810	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	6 75 77
1810	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	6 75 77
1810	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	6 75 77
1810	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	6 75 77
1810	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	6 75 77
1810	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	6 75 77
1810	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	6 75 77
1810	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	6 75 77
1810	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	6 75 77
1810	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	6 75 77
1810	FB_B0_DO_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DO<7..0>	6 75 77
1810	FB_B0_DO_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DO<31..8>	6 75 77
1810	FB_B0_DO_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DO<23..16>	6 75 77
1810	FB_B0_DO_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DO<31..24>	6 75 77
1810	FB_B1_DO_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DO<7..0>	6 75 77
1810	FB_B1_DO_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DO<31..8>	6 75 77
1810	FB_B1_DO_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DO<23..16>	6 75 77
1810	FB_B1_DO_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DO<31..24>	6 75 77

## MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		PHYSICAL	SPACING	
	<u>LVDS_A_CLK</u>	<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_A_CLK_P</u> 83 87
	<u>LVDS_A_CLK</u>	<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_A_CLK_N</u> 83 87
	<u>LVDS_A_DATA</u>	<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_A_DATA_P&lt;2..0&gt;</u> 83 87
	<u>LVDS_A_DATA</u>	<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_A_DATA_N&lt;2..0&gt;</u> 83 87
	<u>LVDS_B_CLK</u>	<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_B_CLK_P</u> 83 87
	<u>LVDS_B_CLK</u>	<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_B_CLK_N</u> 83 87
	<u>LVDS_B_DATA</u>	<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_B_DATA_P&lt;2..0&gt;</u> 83 87
	<u>LVDS_B_DATA</u>	<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_B_DATA_N&lt;2..0&gt;</u> 83 87
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_A_CLK_F_P</u> 6 82
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_A_CLK_F_N</u> 6 82
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_B_CLK_F_P</u> 6 82
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_B_CLK_F_N</u> 6 82
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_A_CLK_P</u> 82 88
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_A_CLK_N</u> 82 88
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_A_DATA_P&lt;2..0&gt;</u> 6 82 88
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_A_DATA_N&lt;2..0&gt;</u> 6 82 88
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_B_CLK_P</u> 82 88
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_B_CLK_N</u> 82 88
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_B_DATA_P&lt;2..0&gt;</u> 6 82 88
		<u>LVDS_85D</u>	<u>LVDS</u>	<u>LVDS_CONN_B_DATA_N&lt;2..0&gt;</u> 6 82 88

## Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		PHYSICAL	SPACING	
<input type="checkbox"/>	GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 78 79
<input type="checkbox"/>	GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M 78 79
<input type="checkbox"/>	LVDS EG A_CLK	LVDS_85D	LVDS	LVDS EG A_CLK P 78 87
<input type="checkbox"/>	LVDS EG A_CLK	LVDS_85D	LVDS	LVDS EG A_CLK N 78 87
<input type="checkbox"/>	LVDS EG A_DATA	LVDS_85D	LVDS	LVDS EG A_DATA P<2..0> 78 87
<input type="checkbox"/>	LVDS EG A_DATA	LVDS_85D	LVDS	LVDS EG A_DATA N<2..0> 78 87
<input type="checkbox"/>	LVDS EG A_DATA3	LVDS_85D	LVDS	NC LVDS EG A_DATA P<3> 78 79
<input type="checkbox"/>	LVDS EG A_DATA3	LVDS_85D	LVDS	NC LVDS EG A_DATA N<3> 78 79
<input type="checkbox"/>	LVDS EG B_DATA	LVDS_85D	LVDS	LVDS EG B_DATA P<2..0> 78 87
<input type="checkbox"/>	LVDS EG B_DATA	LVDS_85D	LVDS	LVDS EG B_DATA N<2..0> 78 87
<input type="checkbox"/>	LVDS EG B_DATA3	LVDS_85D	LVDS	NC LVDS EG B_DATA P<3> 78 79
<input type="checkbox"/>	LVDS EG B_DATA3	LVDS_85D	LVDS	NC LVDS EG B_DATA N<3> 78 79
<input type="checkbox"/>	DP_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_C P<3..0> 78 84
<input type="checkbox"/>	DP_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_C N<3..0> 78 84
<input type="checkbox"/>	DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH_C P 83 84
<input type="checkbox"/>	DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH_C N 83 84
<input type="checkbox"/>	DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG_AUXCH_P 8 78 83
<input type="checkbox"/>	DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG_AUXCH_N 8 78 83

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1701_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1701_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

## Graphics , SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

## Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

## K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL	NET_TYPE		SPACING		
			ENET_10G0	ENETCONN			
		ENET_10G0	ENETCONN	ENETCONN P<3..0>			37
		ENET_10G0	ENETCONN	ENETCONN N<3..0>			37
		SENSE_DIFFPAIR	THERM_1701_558	THERM	CPUTHMSNS D2 P		50
			THERM_1701_558	THERM	CPUTHMSNS D2 N		50
6229	SENSE_DIFFPAIR	THERM_1701_558	THERM	CPU_THERMD_P			9 50
6230		THERM_1701_558	THERM	CPU_THERMD_N			9 50
	SENSE_DIFFPAIR	THERM_1701_558	THERM	GPU_THMSNS_D_P			50
		THERM_1701_558	THERM	GPU_THMSNS_D_N			50
	SENSE_DIFFPAIR	THERM_1701_558	THERM	GPU_TDIODE_P			50 78
		THERM_1701_558	THERM	GPU_TDIODE_N			50 78
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	VCCSA50 CS_P			48 64
		SENSE_1701_558	SENSE	VCCSA50 CS_N			48 64
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	VCCSAISNS_R_P			48
		SENSE_1701_558	SENSE	VCCSAISNS_R_N			48
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_1V5_S3_R_P			48
		SENSE_1701_558	SENSE	ISNS_1V5_S3_R_N			48
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	CPUVCCIOS0 CS_P			48 69
		SENSE_1701_558	SENSE	CPUVCCIOS0 CS_N			48 69
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	CPUVCCIOISNS_R_P			48
		SENSE_1701_558	SENSE	CPUVCCIOISNS_R_N			48
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	GPUISNS_N			48
		SENSE_1701_558	SENSE	GPUISNS_P			48
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_1V5_S3_N			48 66
		SENSE_1701_558	SENSE	ISNS_1V5_S3_P			48 66
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_AIRPORT_N			98
		SENSE_1701_558	SENSE	ISNS_AIRPORT_P			98
6240	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_AIRPORT_P			98
6241		SENSE_1701_558	SENSE	ISNS_AIRPORT_P			98
6242	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_AIRPORT_R_N			100
6243		SENSE_1701_558	SENSE	ISNS_AIRPORT_R_P			100
6244	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_HDD_N			
6245		SENSE_1701_558	SENSE	ISNS_HDD_P			
6246	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_HDD_R_N			100
6247		SENSE_1701_558	SENSE	ISNS_HDD_R_P			100
6248	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_LCDBKLT_N			
6249		SENSE_1701_558	SENSE	ISNS_LCDBKLT_P			
6250	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_ODD_N			
6251		SENSE_1701_558	SENSE	ISNS_ODD_P			
	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_ODD_R_N			100
		SENSE_1701_558	SENSE	ISNS_ODD_R_P			100
6252	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_PP1V0_S0GPU_P			
6253		SENSE_1701_558	SENSE	ISNS_PP1V0_S0GPU_N			
6254	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_PP1V0_S0GPU_R_P			100
6255		SENSE_1701_558	SENSE	ISNS_PP1V0_S0GPU_R_N			100
6256	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	PP1V8_S0GPU_P			
6257		SENSE_1701_558	SENSE	PP1V8_S0GPU_N			
6258	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	PP1V8_S0GPU_R_P			100
6259		SENSE_1701_558	SENSE	PP1V8_S0GPU_R_N			100
6260	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	PP1V5_S0GPU_P			
6261		SENSE_1701_558	SENSE	PP1V5_S0GPU_N			
6262	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	PP1V5_S0GPU_R_P			100
6263		SENSE_1701_558	SENSE	PP1V5_S0GPU_R_N			100
6264	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	CPUIMVP_ISNS1G_P			49 68
6265		SENSE_1701_558	SENSE	CPUIMVP_ISNS1G_N			49 68
6266	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	CPUIMVP_ISNS1G_R_P			49
6267		SENSE_1701_558	SENSE	CPUIMVP_ISNS1G_R_N			49
6268	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_HS_OTHER_P			49
6269		SENSE_1701_558	SENSE	ISNS_HS_OTHER_N			49
6270	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_HS_GPU_P			49
6271		SENSE_1701_558	SENSE	ISNS_HS_GPU_N			49
6272	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	ISNS_HS_COMPUTING_P			49
6273		SENSE_1701_558	SENSE	ISNS_HS_COMPUTING_N			49
6274	SENSE_DIFFPAIR	SENSE_1701_558	SENSE	CPUIMVP_ISNS_P			49
6275		SENSE_1701_558	SENSE	CPUIMVP_ISNS_N			49

## K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P 6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N 6 31
	1T01_DIEPPAIR		CHGR_CSI_R_P 63
	1T01_DIEPPAIR		CHGR_CSI_R_N 63
	1T01_DIEPPAIR		CHGR_CSO_R_P 49 63
	1T01_DIEPPAIR		CHGR_CSO_R_N 49 63
(USB_EXT_A)	USB_R50	USB	USB2_EXT_A_MUXED_P 42
(USB_EXT_A)	USB_R50	USB	USB2_EXT_A_MUXED_N 42
(USB_EXT_A)	USB_R50	USB	USB2_LT1_P 6 42
(USB_EXT_A)	USB_R50	USB	USB2_LT1_N 6 42
	USB_R50	USB	CONN_USB2_BT_P 6
	USB_R50	USB	CONN_USB2_BT_N 6
	USB_R50	USB	USB_LT2_P 6 42
	USB_R50	USB	USB_LT2_N 6 42
SSM2375L_P	AUDIODIEFPAIR	AUDIO	SSM2375L_P 59
	AUDIODIEFPAIR	AUDIO	SSM2375L_N 59
SSM2375R_P	AUDIODIEFPAIR	AUDIO	SSM2375R_P 59
	AUDIODIEFPAIR	AUDIO	SSM2375R_N 59
SSM2375S_P	AUDIODIEFPAIR	AUDIO	SSM2375S_P 59
	AUDIODIEFPAIR	AUDIO	SSM2375S_N 59
SPKRCONN_L_OUT_P	DIEFPAIR	AUDIO	SPKRCONN_L_OUT_P 4 59 60
	DIEFPAIR	AUDIO	SPKRCONN_L_OUT_N 4 59 60
SPKRCONN_R_OUT_P	DIEFPAIR	AUDIO	SPKRCONN_R_OUT_P 4 59 60
	DIEFPAIR	AUDIO	SPKRCONN_R_OUT_N 4 59 60
SPKRCONN_S_OUT_P	DIEFPAIR	AUDIO	SPKRCONN_S_OUT_P 4 59 60
	DIEFPAIR	AUDIO	SPKRCONN_S_OUT_N 4 59 60
	USB_R50	USB	USB_TPAD_R_P 52
	USB_R50	USB	USB_TPAD_R_N 52
	SB_POWER	PF3V3_S5	45 55 65 70 71 72 82 85 89 48 49 50 51 53 56 60 61 71 72 75 76 82 83 85 86 88 89 90 91 92 93 94 95 96 97 98 99
	SB_POWER	PF3V3_S0	
	SB_POWER	PP1V5_S3RS0	
	GND	GND	

	8	7	6	5	4	3	2	1	
	K91 Board-Specific Spacing & Physical Constraints								
	BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION	
	TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.5.1	
D	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM	
	STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM				
	55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM				
	50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	45_OHM_SE	TOP, BOTTOM	Y	0.13 MM	0.13 MM				
	45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM				
	40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	37_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.095 MM				
	37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
C	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM				
	27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.154 MM	0.154 MM	0.200 MM	0.200 MM	0.200 MM	
	72_OHM_DIFF	ISL2, ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM	
	72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM	0.120 MM	0.120 MM	0.120 MM	
	80_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM	
	80_OHM_DIFF	TOP, BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.110 MM	0.090 MM	0.180 MM	0.180 MM	0.180 MM	
	85_OHM_DIFF	ISL2, ISL11	Y	0.110 MM	0.090 MM	0.180 MM	0.180 MM	0.180 MM	
	85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.090 MM	0.190 MM	0.190 MM	0.190 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.102 MM	0.090 MM	0.220 MM	0.220 MM	0.220 MM	
	90_OHM_DIFF	ISL2, ISL11	Y	0.102 MM	0.090 MM	0.220 MM	0.220 MM	0.220 MM	
	90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.090 MM	0.230 MM	0.230 MM	0.230 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM	0.200 MM	0.200 MM	0.200 MM	
	100_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM	0.200 MM	0.200 MM	0.200 MM	
	100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM	0.220 MM	0.220 MM	0.220 MM	
A	PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.065 MM	0.065 MM	0.2 MM	0.2 MM	0.2 MM	
	110_OHM_DIFF	ISL2, ISL11	Y	0.065 MM	0.065 MM	0.2 MM	0.2 MM	0.2 MM	
	110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM	0.330 MM	0.330 MM	0.330 MM	
	8	7	6	5	4	3	2	1	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM


PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100\_DIFF\_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYNC MASTER=K18 MLB

SYNC DATE=04/27/2010

PCB Rule Definitions



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PAGE

SHEET

SIZE

D

109 OF 132

99 OF 101

