Boot Flash System Configuration Block
Version 2.5.15
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In order to reduce product cost, Core99/Core2001 hardware designs will consolidate the information normally stored in separate EEPROMs into the Boot ROM Flash device. Examples of such information include Ethernet hardware address and system bus clock. In these systems, this information will be stored in the "Sys-Config" section of the flash device. This area is an ideal location because, by design, it will never be changed after the machine leaves the factory floor— Firmware update software will only alter the boot image and Open Firmware sections.

The System Configuration Block contains two sections : The BootROM System Configuration (Sys-Config) section and the Configuration Test Data (Test-Data) Section. The Test-Data section is for manufacturing to store motherboard test information. The following tables describe the 136 bytes of the Sys-Config area required for the hardware initialization code. This information primarily addresses motherboard specific items such as the Ethernet Address, Bus Clock, etc. Additionally, for consumer platforms like P1 or C2, this section provides information about the soldered processor and DRAM. Reserved and unprogrammed bytes will be set to 0xFF (the erase value of the flash).

Table 1. Sys-Config (Boot ROM System Configuration)

Byte Offset	0	1	2	3
Header Section				
0x00-0x03	Signature = 0xC99C		Product ID	
0x04-0x07	Build Version (0x000436f1)			
0x08-0x0B	Build Date (0xYYYYMMDD)			
Motherboard Section				
0x0C-0x0F	Motherboard Revision (**Unused**)	Max Auxiliary Power Available(W) (Table 3)	Feature Flags (Table 4)	
0x10-0x13	Feature Flags(cont.)		Sound Architecture Extended (Table 4.1.1)	Config Block Version
0x14-0x17	Bus Clock(Hz)			
0x18-0x1B	PCI0 Clock(Hz)			
0x1C-0x1F	PCI1 Clock(Hz)			
0x20-0x23	PCI2 Clock(Hz)			
Processor Section				
0x24—0x4F	Processor Info (Table 5)			
Motherboard DRAM Section				
0x50-0x53	Memory Type	# of row addresses	# of column addresses	# of banks on SDRAM device
0x54-0x57	CAS Latency(tCL)	RAS to CAS Delay(tRCD)	Row(bank) precharge time(tRP)	Precharge time to RAS Latency(tRAS)
0x58-0x5B	CAS to CAS Delay(tCCD)	Data-in to precharge Latency(tDPL)	SDRAM Attributes: registered,buffered	Superset Tech. (ESDRAM = 0x01)
0x5C-0x5F	# of Soldered Memory Controller banks	SODIMM Bank Numbers(0,1)	Refresh Type	Reserved
0x60-0x63	Reduced Clock Frequency (Hz)			
0x64-0x67	RAM_ClockSignal_Map (Table 6)	DDR Clock Skew		
0x68-0x6B	Reserved			
0x6C-0x6F				
0x70-0x73				
Display Configuration Section				
0x74-0x77	Display Configuration Data			
0x78-0x7B				
Footer Section				
0x7C-0x7F	Checksum of system configuration			
Ethernet Section				
0x80-0x83	0xEA	Ethernet Address		
0x84-0x87	Ethernet Address cont.			Ethernet Address Checksum
Configuration Test Data Section				
0x88-FF	TBD			

The Product ID is a two byte field that represents a unique identifier for each platform. These two bytes are separated into 3 groups: 4bits for Product Family, 6 bits for Product Platform, and 6 bits for Product Version as described in Table 2.

Table 2. Product ID

Byte	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
0x00	Product Family (Table 2.1)				Product Platform			
0x01	Product Platform Cont.		Product Version					

The Product Family bits are described in the Table 2.1 below. It allows us to distinguish between the different classes(families) of products will have.

Table 2.1. Product Family

0	Consumer Desktop	5-15	Reserved
1	Consumer PowerBook		
2	Pro Desktop		
3	Pro PowerBook		
4	Rack		

The Product Platform and Product Version fields work similar to the two digits in the model property(i.e PowerMac4,4). The Product Platform gives the unique machine id for the product in the designated family and the Product Version field represents the release version for the given Product Platform. An example is for Kihei, Product Family will equal 0b0000 for Consumer Desktop(iMac), Product Platform will equal 0b000010) for the second platform in the iMac family and Product Version will equal 0b000001 for the first release of this platform. The two bytes will eqaul 0x0081. P1 will be the first consumer PowerBook and its machine id value will be 0x1081. Sawtooth(PowerMac3,1) will equal 0x20C1.

Max Auxiliary Power:
The Max Auxiliary Power byte in the Motherboard section allows us to indicate to software what the maximum auxiliary power available to PCI slots when the system is in sleep mode. This byte is the delta of the total auxiliary power provided by the system minus the auxiliary power needed by motherboard devices. Power Management software can then use this value to determine if it is safe to turn off power to PCI cards given the auxiliary power available and the auxiliary power needed by installed PCI cards. The table below indicates the layout of the byte:

Table 3. Max Auxiliary Power Available

Byte	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
	Auxiliary Power (Watts)						Scaling factory (Table 3.1)	

The Auxiliary Power represents the watts that are available for auxiliary power. The Scaling factory provides a scaling range for the Auxiliary Power. The Auxiliary Power has a range from 0-252(0xFC) with a granularity of 4(e.g. 4,8,…252). The Scaling Factory then determines the range that the Auxiliary Power value lies based on the table below:

Table 3.1. Scaling Factory Encoding

Bit Encoding	Scaling Factor	Range of Auxiliary Power
0b00	1.0 x	0 to 252 Watts
0b01	0.1 x	0 to 25.2 Watts
0b10	0.01 x	0 to 2.52 Watts
0b11	0.001	0 to .252 Watts

In order to distinguish the different machines, the system configuration information contains feature bits that can be set to describe product functionality. Below is the table which outlines the current bit settings:

Table 4. Feature Flags

Byte	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
0x00	Sound Architecture (Table 4.1)			On-Board Processor	IVAD Exists	Ultra66 Available	Registered CKE	Disable CKE
0x01	Reserved				USB Current Available (Table 4.2)			

0x02	White LED/flash rate	Power Step	AV Jack	C5003 Clock Driver	Ena Spread Spectrum Clock	Skip RAMBank 01	Video Mirror	VDR Power Step
0x03	Pangea MCLK Unused	Dynamic Speed Shift	Init DDR Clock	TBEN Enable	reserved			

The following tables describes the Sound Architecture field:

Table 4.1. Sound Architecture (3 bits)

0	No Sound	4	Screamer - Pismo
1	I2C	5	Screamer - Perigee
2	Screamer - Sawtooth	6	Reserved
3	Screamer - Kihei	7	Use Sound Architecture Extended (Table 4.1.1)

Table 4.1.1 Sound Architecture Extended (8 bits)

0	Not to be used	10	Snapper - Common
1	Tumbler - Tangent		
2	Tumbler - Inspire		
3	Tumbler - Marble		
4	Tumbler - Onyx		
5	Snapper - NLites		
6	Snapper - Mojave		
7	Snapper - Nector		
8	Snapper - Ivory		
9	Racks – light show		

The following table describes the USB current available field:

Table 4.2 USB Current Available Architecture

Standard USB = 0
4000ma = 1
All others reserved

The remaining bits in the feature flags are defined below:

- On-Board Processor – The processor is soldered to the motherboard
- IVAD Exists – Integrated Video and Deflection Processor for setting display timings
- Ultra66 Available – Ultra66 hardware and hard drives present in this configuration
- Registered CKE – MLB has a CKE SDRAM flip flop to run high bus frequency
- USB(0,1) Connected – USB is connected and available for use
- USB(0,1) Power Control – USB Port allows for power control
- White LED/flash rate – LED is controllable by PMU
  - 0= fast rate, original green LED
  - 1 = slow rate, white LED
- PowerStep- CPU can be run at different clock rate/voltage level
- AV Jack- headphone jack also provides video signal (Midway)
- C5003 Clock Driver - System uses an IMI 5003 clock driver chip
- Enable spread spectrum mode o f clock driver chip
- Skip RAMBank 01 – for high end PBs, RAM Bank 0/1 is not wired up so we need to skip probing it
- VDR Power Step- CPU can adjust RAM bus speed and then run PowerStep
- Pangea MClK Unused- The Memory Clocks in Pangea are not used
- Dynamic Speed Shift – Machine supports a fast speed/voltage shift
- Init DDR Clock – The Philips DDR Clock Chip(PCk2059A) needs to be initialized
- TBEN Enable – Enable TBEN support using an external clock for the timebase(Intrepid only)

P1/Kihei will have a soldered processor. P1 will have soldered DRAM as well. System configuration for both the processor and DRAM will be stored in the Boot ROM for these machines where necessary. The DRAM info is required data from the DIMM IIC ROMs to initialize the Uni-North Memoru Subsystem. The processor info is modified from the “WS IIC EEPROM Proposal” document. The following tables outline the processor information:

Table 5. Processor Info

Byte Offset	0	1	2	3
Header Section				
0x00-0x03	Signature = 0xC9	Bytes Used	Size of EEPROM = 2^n	EEPROM Version (0x01= this version)
0x04-0x07	CPU module Revision - 8 char ASCII Apple part number, including revision.			
0x08-0x0B	Examples: 820-1234-A = 8201234A, AP2240-01 = AP224001			
CPU Section				
0x0C-0x0F	# of Processors = n	Bus Mode (Table 5.1)	CPU Core Voltage(x 10mV)	CPU Temperature(°C)
0x10-0x13	Initial HID0 Register (**Pismo Only**)			
0x14-0x17	Boot HID0 Register (**Pismo Only**)			
0x18-0x1B	Default MSSCR0(Max/V'ger)			
Level Two Cache Section				
0x1C-0x1F	# of L2s	Size of L2 = 2^n	L2 Bus Width = 2^n	L2/Processor Ratio (Table 5.2)
0x20-0x23	L2 Mode (Table 5.3)	Reserved		
Level Three Cache Section				
0x24-0x27	# of L3s	Size of L3 = 2^n	L3 Bus Width = 2^n	L3/Processor Ratio (Table 5.2)
0x28-0x2B	L3 Mode (Table 5.3)	L3 Extended Mode (Table 5.4)	L3 PDET	Reserved

Table 5.1 Bus Mode Encoding

Bit 0	Bit 1	Bit 2-3	Bit 4-7
Parity	Reserved	Bus Mode	Bus Width
0 = Unsupported		00 = 60x Bus Mode	Actual Width of the System Bus = 2^n
1 = Supported		01 = MaxBus Mode	
		10 = Reserved	
		11 = Reserved	

Table 5.2. Bus, L2, and L3 to Processor Ratio Encoding

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Numerator				Denominator			
All ratios are with respect to processor speed. In order to calculate the actual bus/L2/L3 speed, the correct formula is (processor speed ÷ (numerator ÷ denominator)).							

Table 5.3. L2/L3 Mode Encoding

Bit 0	Bit 1	Bit 2-3	bit 4-7
Parity	Write Thru	L2 Output Hold	SRAM Type
0 = Not Supported,		00 = 0.5ns	0000 = Flow-Through
1 = Supported		01 = 1.0ns	0001 = Pipelined Burst
		10 = more OH	0010 = Late Write
		11 = even more OH	0011 = PC Double-Data-Rate SRAM
			0100 = Pipeline Burst 3(PB3)
			0101 = MSUG DDR SRAM
			all others = Reserved

Table 5.4. L3 Extended Mode Encoding

Bit 0	Bit 1	Bit 2-3	bit 4	Bit 5-7
L3 Sample Point Override	Additional PDET Shift	L3 Clock Sample Point	L3 No Echo Clock Delay(Apollo Only)	L3 P-Clock Sample Point
0 = No Extra Clk,	0 – No Shift	00 = 2 Clks		000 – 0 Clks
1 = 1 Clk to read latency	1 –Additional Shift	01 = 3 Clks		001 – 1 Clks

		10 = 4 Clks
		11 = 5 Clks

010 – 2 Clks
011 – 3 Clks
100 – 4 Clks
101 – 5 Clks

Table 6. RAM to Clock Signal Mapping Table

Config Block Value	Mapping Style	RAM/Clock Mapping
1	P62	Banks 0,1,6,7 – unused Bank 2 – connected to SDRAM7 and SDRAM 5 Bank 3 – connected to SDRAM6 and SDRAM2 Bank 4 – connected to SDRAM4 and SDRAM3 Bank 5 – connected to SDRAM0 and SDRAM1
255 (Default)	No Mapping Used.	No Mapping Used.

Revision History

2.0 6/28/99 Base System Configuration
2.1 7/6/99 Added back tCAS latency in the Motherboard DRAM info section.
2.2 8/20/99 Claimed reserved bit in L2/L3 Mode byte for setting L2/L3 in Write Thru mode.
2.3 1/3/00 Added Config Block Version to Header section and Refresh Type to DRAM section.
2.4 3/13/00 Added Extended L3 mode field and corresponding encoding table.
Updated current Sound Architecture values andupdated the L2/L3 SRAM types.
2.4.1 5/17/00 Changed the definition of the Sound Architecture value 0 from Burgandy to "No Sound".jdh
2.4.2 5/24/00 Added USB Current Available. jdh
2.4.3 6/5/00 Added Power LED. Hjr
2.4.5 9/21/00 Added sound value of 6 for Tumbler. Jdh
2.4.6 1/30/01 Added extended sound flag for Tumbler, removed the value 6 for Tumbler jdh for drf
2.4.7 2/21/01 Add bit to identify C5003 clock chip in system. Aek
2.4.8 3/7/01 Add Disable CKE feature flag. Aek
2.4.9 3/20/01 Add Onyx and Infinity sound value
2.4.10 3/30/01 Remove Infinity sound and correct description of
2.5 4/9/01 Add spread spectrum enable bit. Aek
2.5.1 6/11/01 Add video Mirroring bit
2.5.2 7/11/01 Add VDR PowerStep
2.5.3 9/27/01 Add Reduced Clock Frequency, Sound Architecture table jdh
2.5.4 10/25/01 Add Skip RAMBank 01 bit and description. Hy
2.5.5 11/19/01 Add PangeaMclk Unused and Dynamic Speed Shift flags. Dmc
2.5.6 1/21/02 Add RAM_ClockSignal_Map byte, indicates how the RAM and clock signals are connected. Cam
2.5.7 2/25/02 Add DDR Ckock Skew byte for setting up the DDR Clock delay on different motherboards. Dmc
2.5.8 3/4/02 Reuse the Rep.algorithm bit in L3 Extended Mode to represent the need for a PDET shift dmc
2.5.9 4/3/02 Reorganize and note unused areas jdh
2.5.10 5/7/02 Add Display Configuration Information that will be put in a property called “display-config-info” in the root node of the OF device tree to be used by the built in display device to describe the connection configuration to the display Fcode at Fcode load time (probe time).
2.5.11 5/20/02 Add Cpu Core Voltage and Cpu Temperature fields to Processor Info section. Also reuse L3 CYA bit to indicate whether we do not need a Echo Clock Delay on Apollo Node5 parts.
2.5.12 5/21/02 Initialize DDR Clock chip so that it clocks come up correctly
2.5.13 8/13/02 Added L3 PDET field to L3 section
2.5.14 11/5/02 Added feature flag for TBEN for Intrepid systems
2.5.15 12/19/02 Correct extended sound. Remove usb0 and 1 conn and PwrCtrl flag . They are completely unused and the the is now a usb2