.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
A	SIDE_ INS_DET_A		CP0_ QACK*		CP1_ QACK*	GND		OVDD		GND	TBEN	OVDD		GND	CHKSTOP*	OVDD	TOP_ INS_DET_B	GND		OVDD	CP0_ INT*	GND	CP1_ SRESET*	OVDD	CP0_ SRESET*	GND		CP1_ QREQ*	CP0_ QREQ*	TOP_ INS_DET_A
B					OVDD	ADIN 37	GND	ADIN 36	OVDD	ADIN 43	GND	ADIN 41	OVDD	ADIN 16	GND	ADOUT 29	OVDD	ADOUT 40	GND	ADOUT 24	OVDD	ADOUT 22	GND	ADOUT 20	OVDD	ADOUT 26	GND				
C			CP1_ INT*	GND	ADIN 23	OVDD	ADIN 33	GND	ADIN 38	OVDD	ADIN 39	GND	ADIN 19	OVDD	ADIN 5	GND	ADOUT 17	OVDD	ADOUT 34	GND	ADOUT 25	OVDD	CLKOUT*	GND	ADOUT 12	OVDD	ADOUT 10	GND			
D			OVDD	ADIN 24	GND	ADIN 31	OVDD	ADIN 32	GND	ADIN 27	OVDD	ADIN 26	GND	ADIN 40	OVDD	ADOUT 19	GND	ADOUT 38	OVDD	ADOUT 21	GND	ADOUT 37	OVDD	CLKOUT	GND	ADOUT 13	OVDD				
E			SYSCLK	OVDD	ADIN 20	GND	ADIN 2	OVDD	ADIN 21	GND	ADIN 34	OVDD	ADIN 29	GND	ADIN 15	OVDD	ADOUT 18	GND	ADOUT 42	OVDD	ADOUT 43	GND	ADOUT 11	OVDD	ADOUT 9	GND	ADOUT 8	OVDD			
F		SYSCLK*	GND	ADIN 12	OVDD	ADIN 7	GND	ADIN 0	OVDD	ADIN 22	GND	ADIN 42	OVDD	ADIN 28	GND	ADOUT 28	OVDD	ADOUT 14	GND	ADOUT 30	OVDD	ADOUT 31	GND	ADOUT 2	OVDD	SROUT1*	GND	ADOUT 1	OVDD	
G		OVDD	CLKIN*	GND	ADIN 8	OVDD	ADIN 3	GND	ADIN 1	OVDD	ADIN 25	GND	ADIN 35	OVDD	ADIN 4	GND	ADOUT 41	OVDD	ADOUT 35	GND	ADOUT 36	OVDD	ADOUT 5	GND	ADOUT 6	OVDD	SROUT1	GND		
H	GND	CLKIN	OVDD	ADIN 10	GND	SRIN0*	OVDD	ADIN 6	GND	ADIN 11	OVDD	ADIN 30	GND	ADIN 17	OVDD	ADOUT 15	GND	ADOUT 39	OVDD	ADOUT 33	GND	ADOUT 32	OVDD	SROUT0	GND	SROUT0*	OVDD	ADOUT 7	GND	
J		GND	ADIN 13	OVDD	SRIN0	GND	SRIN1*	OVDD	SRIN1	GND	ADIN 9	OVDD	ADIN 14	GND	ADIN 18	OVDD	ADOUT 16	GND	ADOUT 27	OVDD	ADOUT 23	GND	ADOUT 0	OVDD	ADOUT 4	GND	ADOUT 3	OVDD		GND
K	SIDE_ INS_DET_B		GND	CP0_ HRESET* ???	OVDD	CP1_ HRESET*	GND		OVDD		GND		OVDD	BOTTOM_ INS_DET_B	GND		OVDD		GND		OVDD		GND		OVDD		GND			BOTTOM_ INS_DET_A

NOTE: {SIGNAL}* means the inverse of {SIGNAL}
NOTE: Signal terminology is borrowed from PPC970MP datasheet & user manual

UNIDENTIFIED:
high resistance to/from ground & processor voltage (>200k)
low resistance to/from ground & processor voltage (<200k)

Processor Status/Control
Clock Control
Interrupts/Reset
Debug/Test Interface
Processor JTAG
Processor I2C
Processor Board Service Signals

Processor Interface Input (North Bridge to 970MP)
Processor Interface Output (970MP to North Bridge)

ACHTUNG: the ADIN29 and ADIN35 signals are swapped in the G5 Cypher version of the 300-pin connector compared to the G5 Omega; PI connections are otherwise identical. (*Dicks!*)

NOTE: while ADIN/ADOUT signals are 44-bit, they only carry 36 bits of data per clock edge; 8 out of 44 bits are used for the checksum, for more information on how the checksum is computed see 970FX User Manual