.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
A	TL_INSERT	SAT_TXD	CP0_QACK*	SAT_RXD	CP1_QACK*	GND	I2C_SAT_DAT	OVDD	I2C_SAT_CLK	GND	TBEN	OVDD	PROCID 1	GND	CHKSTOP*	OVDD	ML_INSERT	GND	PROCID 0	OVDD	CP0_INT*	GND	CP1_SRESET*	OVDD	CP0_SRESET*	GND	CORE_SLEWING*	CP1_QREQ*	CP0_QREQ*	BL_INSERT
B	PP3V3_RUN_MLB	VDNAP	OVERTEMP*	SAT_MRESET*	OVDD	ADIN 37	GND	ADIN 36	OVDD	ADIN 43	GND	ADIN 41	OVDD	ADIN 16	GND	ADOUT 29	OVDD	ADOUT 40	GND	ADOUT 24	OVDD	ADOUT 22	GND	ADOUT 20	OVDD	ADOUT 26	GND	POWERFAIL*	PP1V2_OVDD_RUN_MLB	PP1V2_OVDD_RUN_MLB
C	TRIGGER OUT	PP5V_RUN_MLB	CP1_INT*	GND	ADIN 23	OVDD	ADIN 33	GND	ADIN 38	OVDD	ADIN 39	GND	ADIN 19	OVDD	ADIN 5	GND	ADOUT 17	OVDD	ADOUT 34	GND	ADOUT 25	OVDD	CLKOUT*	GND	ADOUT 12	OVDD	ADOUT 10	GND	TDI	PP1V2_OVDD_RUN_MLB
D	PP3V3_PWRON_MLB	SAT_CLK	OVDD	ADIN 24	GND	ADIN 31	OVDD	ADIN 32	GND	ADIN 27	OVDD	ADIN 26	GND	ADIN 40	OVDD	ADOUT 19	GND	ADOUT 38	OVDD	ADOUT 21	GND	ADOUT 37	OVDD	CLKOUT	GND	ADOUT 13	OVDD	PSYNC	TMS	PP1V2_OVDD_RUN_MLB
E	OVDD_ENABLE	SV_PP12V	SYSCLK	OVDD	ADIN 20	GND	ADIN 2	OVDD	ADIN 21	GND	ADIN 34	OVDD	ADIN 29	GND	ADIN 15	OVDD	ADOUT 18	GND	ADOUT 42	OVDD	ADOUT 43	GND	ADOUT 11	OVDD	ADOUT 9	GND	ADOUT 8	OVDD	TCK	PP1V2_OVDD_RUN_MLB
F	SV_PROC_SENSE_I	SYSCLK*	GND	ADIN 12	OVDD	ADIN 7	GND	ADIN 0	OVDD	ADIN 22	GND	ADIN 42	OVDD	ADIN 28	GND	ADOUT 28	OVDD	ADOUT 14	GND	ADOUT 30	OVDD	ADOUT 31	GND	ADOUT 2	OVDD	SROUT1*	GND	ADOUT 1	OVDD	TDO
G	AGND_SAT	OVDD	CLKIN*	GND	ADIN 8	OVDD	ADIN 3	GND	ADIN 1	OVDD	ADIN 25	GND	ADIN 35	OVDD	ADIN 4	GND	ADOUT 41	OVDD	ADOUT 35	GND	ADOUT 36	OVDD	ADOUT 5	GND	ADOUT 6	OVDD	SROUT1	GND	NC	NC
H	GND	CLKIN	OVDD	ADIN 10	GND	SRIN0*	OVDD	ADIN 6	GND	ADIN 11	OVDD	ADIN 30	GND	ADIN 17	OVDD	ADOUT 15	GND	ADOUT 39	OVDD	ADOUT 33	GND	ADOUT 32	OVDD	SROUT0	GND	SROUT0*	OVDD	ADOUT 7	GND	SV_CORE_VSNS
J	CPU1_TEMP	GND	ADIN 13	OVDD	SRIN0	GND	SRIN1*	OVDD	SRIN1	GND	ADIN 9	OVDD	ADIN 14	GND	ADIN 18	OVDD	ADOUT 16	GND	ADOUT 27	OVDD	ADOUT 23	GND	ADOUT 0	OVDD	ADOUT 4	GND	ADOUT 3	OVDD	NC	AGND_VCORE
K	TR_INSERT	NC	GND	CP0_HRESET*	OVDD	CP1_HRESET*	GND	BYPASS*	OVDD	NC	GND	NC	OVDD	MR_INSERT	GND	NC	OVDD	NC	GND	NC	OVDD	NC	GND	NC	OVDD	NC	GND	NC	CPU0_TEMP	BR_INSERT

NOTE: {SIGNAL}* means the inverse of {SIGNAL}
NOTE: Signal terminology is borrowed from PPC970MP datasheet & user manual

Processor Board Power Signals
SMU Sat Signals
SMU Sat I2C
SMU Sat UART?
Insert Detect

Processor Status/Control
Clock Control
Interrupts/Reset
Debug/Test Interface
Processor JTAG

Processor Interface Input (North Bridge to 970MP)
Processor Interface Output (970MP to North Bridge)

ACHTUNG: the ADIN29 and ADIN35 signals are swapped in the G5 Cypher version of the 300-pin connector compared to the G5 Omega; PI connections are otherwise identical. (*Dicks!*)

NOTE: insert detect signals should be shorted on the board, which allows the motherboard to recognize that processor board is properly seated due to the change in resistance (resistor on MB vs dead short on PB): BL_INSERT to ML_INSERT, TL_INSERT to TR_INSERT, MR_INSERT to BR_INSERT.

NOTE: while ADIN/ADOUT signals are 44-bit, they only carry 36 bits of data per clock edge; 8 out of 44 bits are used for the checksum, for more information on how the checksum is computed see 970FX User Manual