IBM PowerPC 970FX RISC Microprocessor

Datasheet

Version 2.5

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Revision Log

Revision	Modification
March 26, 2007	Version 2.5 • Removed a note about disabling on-chip termination from *Figure 3-3 Block Diagram of an SSB for a Processor Interconnect Implementation* on page 30.
March 14, 2007	Version 2.4 • Removed part numbers IBM25PPC970FX6TB348ET and IBM25PPC970FX6TB348RT from the list of DD3.0x offerings in *Table 1-1 PowerPC 970FX Ordering and PVR for the Standard Lead Package Version* on page 16. • Removed part numbers IBM25PPC970FX6UB348RT, IBM25PPC970FX6UB428ET, and IBM25PPC970FX6UB429RT from the list of DD3.1 offerings in *Table 1-1 PowerPC 970FX Ordering and PVR for the Standard Lead Package Version* on page 16. • Removed part numbers IBM25PPC970FX6TB348ET and IBM25PPC970FX6TB348RT from the list of DD3.0x offerings in *Table 1-2 PowerPC 970FX Ordering and PVR for the Reduced-Lead Package Version* on page 17. • Removed part numbers IBM25PPC970FX6UR348RT, IBM25PPC970FX6UR428ET, and IBM25PPC970FX6UR429RT from the list of DD3.1 offerings in *Table 1-2 PowerPC 970FX Ordering and PVR for the Reduced-Lead Package Version* on page 17. • Changed the reliability grade from 3 to 2 in *Figure 1-2 Part Number Legend* on page 18. • Added the temperature range of the thermal diode into *Table 3-2 Recommended Operating Conditions* on page 21. • Removed old *Table 3-5* and *Table 3-6*, which contained power values for power-optimized parts. • Added 1.0, 1.2, 1.4, and 1.6 GHz frequency values to *Table 3-5 Power Consumption for Standard-Lead Packages* on page 24. • Created *Table 3-6 Power Consumption for Reduced-Lead Packages* on page 25. • Removed 2.2 GHz power dissipation figures from *Table 3-5 Power Consumption for Standard-Lead Packages* on page 24 and *Table 3-7 Power Consumption Throttle Back F/2* on page 26. • Corrected the recommended setting note for the $\overline{\text{TRST}}$ signal in *Table 5-8 Input/Output Signal Descriptions* on page 71. • Moved the revision log to after the front matter of the document.
June 4, 2006	Version 2.3 • Updated pin connection requirements in *Table 4-2. Pinout Listing for the CBGA Package, Table 5-7. PowerPC 970FX Pins for Manufacturing Test Only,* and *Table 5-8. Input/Output Signal Descriptions.* • Added note to Section 5.7.2.
April 11, 2006	Version 2.2 • Updated power-related values contained in *Table 3-2. Recommended Operating Conditions*, *Table 3-5. Power Consumption for Power-Optimized Parts*, *Table 3-7. Power Consumption for Standard Parts*, and *Table 5-2. PowerPC 970FX PLL Configuration.* • Updated power-related descriptions contained in *Section 4.1 ESD Considerations* and *Section 5.3 PLL Power Supply Filtering*.
October 14, 2005	Version 2.1 • Corrected F/2 values in *Table 3-5. Power Consumption for Power-Optimized Parts.* • Enhanced descriptions within *Section 4.2.2 Reduced-Lead Package Version.*
September 30, 2005	Version 2.0 • Added information that describes the distinctive specifications of the *leaded* package version and the *reduced-lead* package version: - Under *Section 1.4 Ordering and Processor Version Register*, added *Leaded Package Version* and *Reduced-Lead Package Version* subsections. - Reorganized *Section 3.1.5 Power Consumption*, to provide power consumption information for both standard and power-optimized parts in *Table 3-5*, *Table 3-6*, *Table 3-7* and *Table 3-8*. - Under *Section 4.2 Mechanical Packaging*, added *Leaded Package Version* and *Reduced-Lead Package Version* subsections. • Updated *Figure 5-1. PLL Power Supply Filter Circuit* with current information and clarified several of the figure callouts.

Revision	Modification
July 15, 2005	Version 1.0 • Updated features listing, *Table 1-1. PPC 970FX Ordering and PVR for the Leaded Package Version* and *Figure 1-2 Part Number Legend.* • Added errata list and application note documents to *Related Publications.* • Updated some of the specifications in *Table 3-2. Recommended Operating Conditions.* • Updated *Section 3.1.5 Power Consumption*, modifying the content and form of the specification tables. • Added a note to *Figure 3-3. Block Diagram of an SSB for a Processor Interconnect Implementation.* • Updated some of the specifications in *Section 3.5.1.2 Drive Side Characteristics.* • Extensively updated specifications in *Table 3-6. Power Consumption for Power-Optimized Parts* and *Table 3-7. Power Consumption for Standard Parts.* • Updated some of the specifications in *Table 3-11. Processor Interconnect SSB Driver Specifications* and *Table 3-13. Processor Interconnect SSB Receiver Specifications.* • Made major modifications to *Table 3-12. Processor Interconnect SSB PCB Trace Specifications*, *Table 3-14. Processor Interconnect SSB Timing Parameters for the Deskew and Clock Alignment* and *Section 3.5.1.4 Receive Side Characteristics.* • Added *Table 3-17. Input ac Timing Specifications for TBEN.* • Added a clarifying note to *Section 3.10.1 I^2C Bus Timing Information.* • Clarified text in *Section 3.10.3 I^2C and JTAG Considerations.* • Updated some of the specifications in *Figure 3-10. JTAG Clock Input Timing Diagram.* • Made major modifications to *Section 3.10.3 I2C and JTAG Considerations*, *Section 5.7.1 Thermal Management pins*, and *Section 5.7.2 Reading Thermal Diode Calibration Data Through JTAG.* • Updated *Section 4. PowerPC 970FX Microprocessor Dimension and Physical Signal Assignments* to describe both packaging types. • Changed the titles for *Figure 4-1. PPC 970FX Microprocessor for Mechanical Package, Leaded, for DD3.0x Parts (top and side)* and *Figure 4-2. PPC 970FX Microprocessor Mechanical Package, Leaded, for DD3.1x Parts (top and side)*. • Updated *Table 5-2. PowerPC 970FX PLL Configuration* and *Table 5-3. System Configuration - Typical Examples of Pin Settings.* • Added *Table 5-9. Thermal Diode Data Encoding.* • Updated some of the specifications in *Table 5-10. Allowable Forces on the PowerPC 970FX Package.*

About This Datasheet

This datasheet describes the IBM® PowerPC® 970FX RISC Microprocessor. This microprocessor, also called the PPC 970FX, is a 64-bit implementation of the IBM PowerPC family of reduced instruction set computer (RISC) microprocessors that are based on the PowerPC Architecture™.

Who Should Read This Datasheet

This datasheet is intended for designers who plan to develop products using the PPC 970FX.

Related Publications

Related IBM publications include the following documents:

- *PowerPC 970FX RISC Microprocessor Users Manual*
- *PowerPC 970FX Power-On Reset Application Note*
- *PowerPC 970FX DD3.x Errata List*

Other related publications include the following documents:

- *The* I^2*C-bus specification.* This document can be downloaded from the NXP web site at http://www.nxp.com/products/interface_control/i2c/.

Conventions and Notations Used in This Datasheet

The use of overbars, for example $\overline{\text{DDEL\_OUT}}$, designates signals that are active low or the complement of differential signals.

The following software documentation conventions are used in this manual:

1. Function names are written in **bold** type. For example, **np_npms_proc_register ()**.
2. Variables are written in italic type. For example, *enable_mode*.
3. Keywords and data types are shown by being written all in capitals with underlines between words. For example, OFF_DISABLED.

1. General Information

1.1 Description

The IBM PowerPC 970FX RISC microprocessor is a 64-bit implementation of the IBM PowerPC family of reduced instruction set computer (RISC) microprocessors that are based on the PowerPC Architecture. This microprocessor, also called the PowerPC 970FX, includes a vector single-instruction, multiple-data (SIMD) facility that supports high-bandwidth data processing and algorithmic-intensive computations. This microprocessor is also designed to support multiple system organizations, including desktop and low-end server applications, and uniprocessor up through 4-way symmetric multiprocessor configurations.

Note: The terms microprocessor and processor are used interchangeably in this document.

Figure 1-1 on page 15 is a block diagram of the PowerPC 970FX.

The PowerPC 970FX consists of three main components:

- PowerPC 970FX core, which includes vector/SIMD multimedia extension execution units
- PowerPC 970FX storage subsystem, which includes core interface logic, noncacheable unit, L2 cache and controls, and the bus interface unit
- PowerPC 970FX pervasive functions

This document also provides pertinent physical characteristics of the PowerPC 970FX single-chip modules.

1.2 Features

- 64-bit implementation of the PowerPC Architecture (version 2.01)
  - Binary compatibility for all PowerPC application level code (problem state)
  - Binary compatibility for all PowerPC application level code (problem state)
  - Support for the 32-bit operating system bridge facility
  - Vector/SIMD multimedia extension
- Layered implementation strategy for very high frequency operation
  - Deeply pipelined design
    - 16 stages for most fixed-point register-to-register operations
    - 18 stages for most load and store operations (assuming L1 data cache hit)
    - 21 stages for most floating-point operations
    - 19, 22, and 25 stages for fixed-point, complex-fixed, and floating-point operations, respectively in the vector arithmetic logic unit (VALU)
    - 19 stages for vector/SIMD multimedia extension permute operations
- Dynamic instruction cracking for some instructions allows for simpler inner core data flow
    - Dedicated data flow for cracking one instruction into two internal operations
    - Microcoded templates for longer emulation sequences
- Speculative superscalar inner core organization
  - Aggressive branch prediction
    - Prediction for up to two branches per cycle
    - Support for up to 16 predicted branches in flight
    - Prediction support for branch direction and branch addresses
  - Out-of-order issue of up to 10 operations into 10 execution pipelines

    - Two load or store operations
    - Two fixed-point register-to-register operations
    - Two floating-point operations
    - One branch operation
    - One condition register operation
    - One vector/SIMD multimedia extension permute operation
    - One vector/SIMD multimedia extension arithmetic logic unit (ALU) operation
  - In-order dispatch of up to five operations into a distributed issue queue structure
  - Register renaming on general purpose registers (GPRs), floating-point registers (FPRs), Vector Register Files (VRFs), condition register (CR) fields, Integer Exception Register (XER), Floating-Point Status and Control Register (FPSCR), Vector Status and Control Register (VSCR), Vector Register Save (VRSAVE), and Link and Count

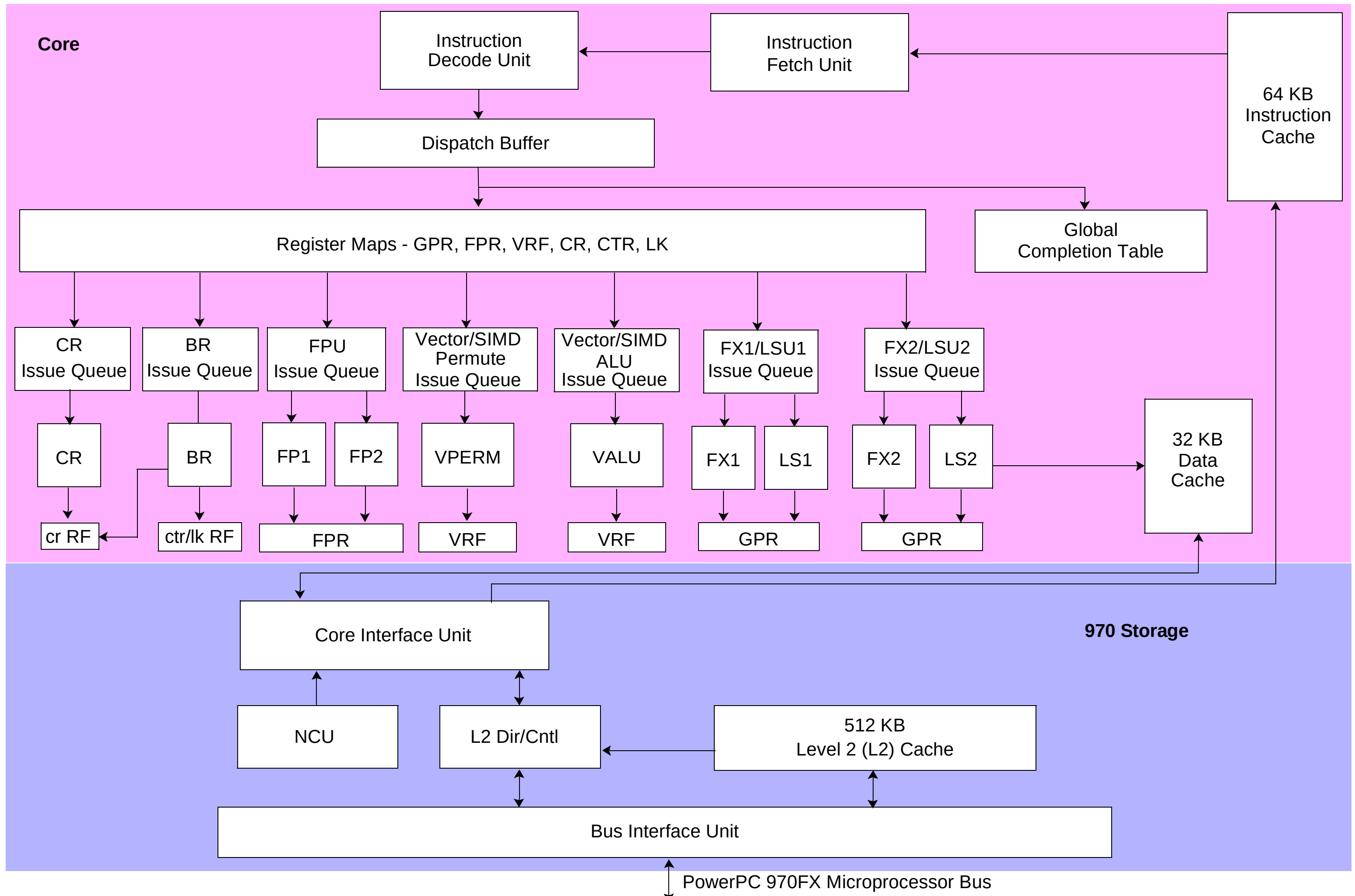
- Large number of instructions in flight (theoretical maximum of 215 instructions)
    - Up to 16 instructions in the instruction fetch unit (fetch buffer and overflow buffer)
    - Up to 32 instructions in the instruction fetch buffer in the instruction decode unit
    - Up to 35 instructions in three decode pipe stages and four dispatch buffers
    - Up to 100 instructions in the inner-core (after dispatch)
    - Up to 32 stores queued in the store queue (STQ) (available for forwarding)
  - Fast, selective flush of incorrect speculative instructions and results

- Specific focus on storage latency management
  - Out-of-order and speculative issue of load operations
  - Support for up to eight outstanding L1 cache line misses
  - Hardware-initiated instruction prefetching from the level 2 (L2) cache
  - Software-initiated data stream prefetching
    - Support for up to eight active streams
  - Critical word forwarding; critical sector first
  - New branch processing; prediction hints added to branch instructions

- Power management
  - Static power management
    - Software-initiated doze and nap
  - Dynamic power management
    - Parts of the design stop their (hardware-initiated) clocks when not in use
  - Power tuning engine
    - Software-initiated slow down of the processor; selectable to half of the nominal operating frequency

1.3 PowerPC 970FX RISC Microprocessor Block Diagram

Figure 1-1. PowerPC 970FX Block Diagram



ALU	Arithmetic logic unit	FPR	Floating point register	LSU	Local store unit	VPERM	Vector permute unit
BR	Branch	FPU	Floating point unit	NCU	Noncacheable unit	VRF	Vector register file
CR	Condition Register	FX	Fixed point	RF	Register file		
CTR	Counter Register	GPR	General purpose register	SIMD	Single-instruction, multiple-data		
FP	Floating point	LK	Link bit	VALU	Vector arithmetic logic unit		

1.4 Ordering and Processor Version Register

1.4.1 Standard Lead Package Version

Table 1-1 lists the PowerPC 970FX RISC Microprocessor part numbers and Processor Version Register (PVR) values for the respective design revision levels in a package that contains lead. See *Figure 1-2* on page 18 for the part number legend.

Table 1-1. PowerPC 970FX Ordering and PVR for the Standard Lead Package Version

Order Part Number	Frequency GHz	Revision Level	PVR	Note
IBM25PPC970FX6TB055RT	1.0	DD3.0x	x'003C0300'	See note
IBM25PPC970FX6TB075RT	1.2			
IBM25PPC970FX6TB186ET	1.6			
IBM25PPC970FX6TB267ET	1.8			
IBM25PPC970FX6UB055RT	1.0	DD3.1	x'003C0301'	
IBM25PPC970FX6UB075RT	1.2			
IBM25PPC970FX6UB105RT	1.4			
IBM25PPC970FX6UB185RT	1.6			
IBM25PPC970FX6UB186ET	1.6			
IBM25PPC970FX6UB267ET	1.8			
IBM25PPC970FX6UB348ET	2.0			

Note: See *Table 3-5* and *Table 3-7* on page 26 for power and voltage rating.

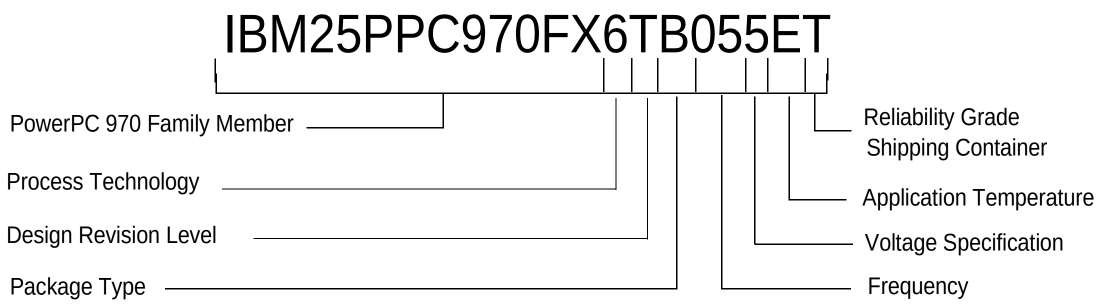
1.4.2 Reduced-Lead Package Version

Table 1-2 lists the PowerPC 970FX RISC Microprocessor part numbers and PVR values for the respective design revision levels in a package that contains less lead. See *Figure 1-2* on page 18 for the part number legend.

Table 1-2. PowerPC 970FX Ordering and PVR for the Reduced-Lead Package Version

Order Part Number	Frequency GHz	Revision Level	PVR	Note
IBM25PPC970FX6TR055RT	1.0	DD3.0x	x‘003C0300’	See note.
IBM25PPC970FX6TR075RT	1.2			
IBM25PPC970FX6TR186ET	1.6			
IBM25PPC970FX6TR267ET	1.8			
IBM25PPC970FX6UR055RT	1.0	DD3.1	x‘003C0301’	
IBM25PPC970FX6UR075RT	1.2			
IBM25PPC970FX6UR105RT	1.4			
IBM25PPC970FX6UR185RT	1.6			
IBM25PPC970FX6UR186ET	1.6			
IBM25PPC970FX6UR267ET	1.8			
IBM25PPC970FX6UR348ET	2.0			
Note: See *Table 3-5* on page 24 and *Table 3-7* on page 26 for power and voltage rating.				

Figure 1-2. Part Number Legend



Process Technology	6 = 10K0 (90 nm complementary metal oxide semiconductor [CMOS] silicon-on-insulator [SOI])
Design Revision Level	T = DD3.0x U = DD3.1
Package Type	B = 576 CBGA Ceramic Ball Grid Array (CBGA) R = 576 CBGA Pb reduced
Frequency	05 = 1.0 GHz 07 = 1.2 GHz 10 = 1.4 GHz 18 = 1.6 GHz 26 = 1.8 GHz 34 = 2.0 GHz
Voltage Specification	5 = V_{DD} is 1.00 V 6 = V_{DD} is 1.10 V 7 = V_{DD} is 1.15 V 8 = V_{DD} is 1.25 V 9 = V_{DD} is 1.20 V
Application Temperature	E = 105°C R = 105°C
Reliability Grade Shipping Container	T = Grade 2 Reliability, Tray **Note 1:** Automatic array recovery must be enabled as detailed in the *PowerPC 970FX RISC Microprocessor Power-On Reset Application Note*. **Note 2:** Grade 2 is 25 failures in time (FITs) (average failure rate) at 60°C for 40k and 100k power-on hours (POH).

2. General Parameters

Table 2-1 summarizes the general parameters of the PowerPC 970FX.

Table 2-1. General Parameters of the PowerPC 970FX

Item	Description	Notes
Die size	66.2 square mm	
Die dimensions	7.07 × 9.36 mm	
Transistor count	58 million	1
Package	576-pin ceramic ball grid array, 25 × 25 mm (1.0 mm pitch)	

1. For information only. The use of this value to calculate reliability is not valid.

3. Electrical and Thermal Characteristics

This section provides alternating current (ac) and direct current (dc) electrical specifications and thermal characteristics for the PowerPC 970FX.

3.1 dc Electrical Characteristics

The tables in this section describe the PowerPC 970FX RISC Microprocessor dc electrical characteristics.

3.1.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit	Notes
Core supply voltage	V_{DD}	-0.3 to 1.5	V	1, 3
I/O supply voltage	OV_{DD}	-0.3 to 1.7	V	1, 3
Phase-locked loop (PLL) supply voltage	AV_{DD}	-0.3 to 3.0	V	1, 3
Input voltage	V_{IN}	-0.3 to 1.7	V	1, 2
Storage temperature range	T_{STG}	-40 to 125	°C	1

1. Functional and tested operating conditions are given in *Table 3-2. Recommended Operating Conditions on page 21*. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed might affect device reliability or cause permanent damage to the device.
2. This is an implied dc voltage specification. Pending further evaluation, an allowance for ac overshoot or undershoot might be accommodated beyond this input voltage specification.
3. Power supply ramping recommendations:
   The order does not matter if the supplies reach their final destination in 50 ms.
   V_{DD} cannot exceed OV_{DD} by more than 0.8 V (except for 50 ms during power on or off, where it is allowed to be ≤ 1.35 V).
   OV_{DD} cannot exceed V_{DD} by more than 0.8 V (except for 50 ms during power on or off, where it is allowed to be ≤ 1.55 V).
   AV_{DD} cannot exceed V_{DD} by more than 2.5 V (except for 50 ms during power on or off, where it is allowed to be ≤ 2.75 V).

3.1.2 Recommended Operating Conditions

Table 3-2. Recommended Operating Conditions (Page 1 of 2)

Characteristic	Symbol	Value	Unit	Notes
Core supply voltage	V_{DD}	See *Table 3-5* and *Table 3-7* on page 26.	V	
PLL supply voltage	AV_{DD}	2.80±50 mV	V	1
PLL supply current, maximum	AI_{DD}	20	mA	
I/O supply voltage	OV_{DD}	1.5±50 mV	V	

Notes:

1. The PLL supply voltage has been adjusted to account for the maximum possible dc drop across the filter circuit. See *Section 5.3 PLL Power Supply Filtering* on page 66.
2. This is the maximum I/O current. As noted in *Table 3-7 Power Consumption Throttle Back F/2* on page 26, the actual I/O power varies between 1 - 3 watts based on the speed of the processor interface (PI) and whether the on-board termination is used. Typically it is active, but in cases of the slower parts and layouts with parts in very close proximity, signal analysis might show that the PI terminations can be turned off.

Table 3-2. Recommended Operating Conditions (Page 2 of 2)

Characteristic	Symbol	Value	Unit	Notes
I/O supply current, maximum	OI_{DD}	2	A	2
Input voltage	V_{IN}	GND to OV_{DD}	V	
Thermal diode temperature	T_{DIODE}	0 to 105	°C	

Notes:

1. The PLL supply voltage has been adjusted to account for the maximum possible dc drop across the filter circuit. See *Section 5.3 PLL Power Supply Filtering* on page 66.
2. This is the maximum I/O current. As noted in *Table 3-7 Power Consumption Throttle Back F/2* on page 26, the actual I/O power varies between 1 - 3 watts based on the speed of the processor interface (PI) and whether the on-board termination is used. Typically it is active, but in cases of the slower parts and layouts with parts in very close proximity, signal analysis might show that the PI terminations can be turned off.

3.1.3 Package Thermal Characteristics

Table 3-3. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
Ceramic ball grid array (CBGA) thermal conductance to back of die	θ_{JC}	0.1	°C/W
CBGA thermal conductance to system board	θ_{JB}	5.4	°C/W

3.1.4 dc Electrical Specifications

Table 3-4. dc Electrical Specifications

Characteristic	Symbol	Voltage		Unit	Notes
		Minimum	Maximum		
SYSCLK, $\overline{\text{SYSCLK}}$ input high voltage	—	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	1
SYSCLK, $\overline{\text{SYSCLK}}$ input low voltage	—	-0.3	$0.3 \times OV_{DD}$	V	1
Processor interface (PI) input high voltage	V_{IH}	$(0.5 \times OV_{DD}) + 0.2$	—	V	2
PI input low voltage	V_{IL}	—	$(0.5 \times OV_{DD}) - 0.2$	V	2
NonPI input high voltage	V_{IH}	$0.7 \times OV_{DD}$	—	V	3
NonPI input low voltage	V_{IL}	—	$0.3 \times OV_{DD}$	V	3
PI output high voltage	V_{OH}	$0.78 \times OV_{DD}$	—	V	4
PI output low voltage	V_{OL}	—	$0.22 \times OV_{DD}$	V	4
NonPI output high voltage, I_{OH} = -2 mA	V_{OH}	$OV_{DD} - 0.2$	—	V	—
NonPI output low voltage, I_{OL} = 2 mA	V_{OL}	—	0.2	V	—
Open drain (OD) output low, I_{OL} = 2 mA (CHKSTOP, I2CGO)	V_{OL}	—	0.2	V	5
OD output low, I_{OL} = 5 mA (I2C)	V_{OL}	—	0.2	V	
Input leakage current, $V_{IN} = OV_{DD}$, V_{IN} = 0 V	I_{IN}	—	60	µA	—
Hi-Z (off state) leakage current, $V_{OUT} = OV_{DD}$, V_{OUT} = 0 V	I_{TSO}	—	60	µA	—
Input capacitance, V_{IN} = 0 V, frequency = 1 MHz	C_{IN}	—	5.0	pF	6

Notes: See *Table 3-2* on page 21 for recommended operating conditions.

1. SYSCLK differential receiver requires high-speed transceiver logic (HSTL) differential signaling level. See the Joint Electron Device Engineering Council (JEDEC) HSTL standard.
2. See the electrical interface section of the *PowerPC 970FX RISC Microprocessor Users Manual*. The minimum input must meet the signal eye opening requirements of the link.
3. The Joint Test Action Group (JTAG) signals TDI, TMS, and $\overline{\text{TRST}}$ do not have internal pullups; therefore, pullups must be added to the system board. Pullups should be added and adjusted according to the system implementation. These input and outputs meet the dc specification in the JEDEC standard JESD8-11 for 1.5 V normal power supply range.
4. A 100 Ω split terminator is the test load. Note that a 40 Ω signal driver has an up level of $0.78 \times OV_{DD}$ for V_{OH} and $0.22 \times OV_{DD}$ at V_{OL}.
5. There are two open drain signals on this type of signal driver: CHKSTOP and I2CGO. The pullup for these nets depend on the T_{rise} time requirement, net load, and topology. The following examples are two bounding suggestions based on a point-to-point 50 Ω net with two lengths (5 cm and 61 cm). A 33 Ω series source terminator was added in both runs. A net of 61 cm is recommended.

   Examples:
   500 Ω pullup dc low level 0.18 V at the receiver
   T_{rise} 0.2 V - 0.8 V = 55 ns at 61 cm
   T_{rise} 0.2 V - 0.8 V = 10 ns at 5 cm

   1 kΩ pullup dc low level 0.13 V at the receiver
   T_{rise} 0.2 V - 0.8 V = 115 ns at 61 cm
   T_{rise} 0.2 V - 0.8 V = 20 ns at 5 cm
6. Capacitance values are guaranteed by design and characterization, and are not tested.

3.1.5 Power Consumption

For recommended operating conditions, see *Table 3-2* on page 21.

Table 3-5. Power Consumption for Standard-Lead Packages

			Full				F/2			
Frequency	Condition	Voltage (V)	Power (W)	Power (Integer Only)[1]	Doze Power	Nap Power	Power (W)	Doze Power	Nap Power	Notes
1.0 GHz	Typical Average at 65°C	1.00	11							2, 3, 4
	Maximum at 105°C		14							2, 3, 4
1.2 GHz	Typical Average at 65°C	1.00	13							2, 3, 4
	Maximum at 105°C		16							2, 3, 4
1.4 GHz	Typical Average at 65°C	1.00	15							2, 3, 4
	Maximum at 105°C		19							2, 3, 4
1.6 GHz	Typical Average at 65°C	1.00	17							2, 3, 4
	Maximum at 105°C		21							2, 3, 4
1.6 GHz	Typical Average at 65°C	1.10	23							2, 3, 4
	Maximum at 85°C		27	23.5	17	13	21	13	11	3, 4
	Maximum at 105°C		29	25.2						2, 3, 4
1.8 GHz	Typical Average at 65°C	1.15	30							2, 3, 4
	Maximum at 85°C		35	30.5	21	17	27	17	15	3, 4
	Maximum at 105°C		37	33.1						2, 3, 4
2.0 GHz	Typical Average at 65°C	1.25	48							2, 3, 4
	Maximum at 85°C		56	47.85	38	31	46	30	27	3, 4
	Maximum at 105°C		60	52.2						2, 3, 4

Note: Maximum power at 85°C is the *only* value that is guaranteed by manufacturing test. Values for typical at 65°C, maximum at 105°C, nap, and doze are not guaranteed by test. These values are to be used as characterization-based nominal values and are included for comparison purposes only.

1. Maximum power numbers are measured by tester code that includes floating-point (FP) and vector/SIMD multimedia extension instructions. Characterization results indicate that similar power test code that is integer only is an average of 13% less. The values in this column are not tested but based on the characterization information. The FP and vector/SIMD multimedia extension units are automatically clock gated when not in use.
2. Maximum power is projected at the nominal V_{DD} ,worst case I_{DDq}, and the maximum temperature as specified.
3. Voltage tolerance is ±50 mV.
4. These are core power only; OV_{DD} power of 1 - 3 watts is not included.

Table 3-6. Power Consumption for Reduced-Lead Packages

			Full				F/2			
Frequency	Condition	Voltage (V)	Power (W)	Power (Integer Only)[1]	Doze Power	Nap Power	Power (W)	Doze Power	Nap Power	Notes
1.0 GHz	Typical Average at 65°C	1.00	11							2, 3, 4
	Maximum at 105°C		14							2, 3, 4
1.2 GHz	Typical Average at 65°C	1.00	13							2, 3, 4
	Maximum at 105°C		16							2, 3, 4
1.4 GHz	Typical Average at 65°C	1.00	15							2, 3, 4
	Maximum at 105°C		19							2, 3, 4
1.6 GHz	Typical Average at 65°C	1.00	17							2, 3, 4
	Maximum at 105°C		21							2, 3, 4
1.6 GHz	Typical Average at 65°C	1.10	23							2, 3, 4
	Maximum at 85°C		27	23.5	17	13	21	13	11	3, 4
	Maximum at 105°C		29	25.2						2, 3, 4
1.8 GHz	Typical Average at 65°C	1.15	30							2, 3, 4
	Maximum at 85°C		35	30.5	21	17	27	17	15	3, 4
	Maximum at 105°C		38	33.1						2, 3, 4
2.0 GHz	Typical Average at 65°C	1.25	48							2, 3, 4
	Maximum at 85°C		56	47.85	38	31	46	30	27	3, 4
	Maximum at 105°C		60	52.2						2, 3, 4

Note: Maximum power at 85°C is the *only* value that is guaranteed by manufacturing test. Values for typical at 65°C, maximum at 105°C, nap, and doze are not guaranteed by test. These values are to be used as characterization-based nominal values and are included for comparison purposes only.

1. Maximum power numbers are measured by tester code that includes floating-point (FP) and vector/SIMD multimedia extension instructions. Characterization results indicate that similar power test code that is integer only is an average of 13% less. The values in this column are not tested but based on the characterization information. The FP and vector/SIMD multimedia extension units are automatically clock gated when not in use.
2. Maximum power is projected at the nominal V_{DD} ,worst case I_{DDq}, and the maximum temperature as specified.
3. Voltage tolerance is ±50 mV.
4. These are core power only; OV_{DD} power of 1 - 3 watts is not included.

Table 3-7. Power Consumption Throttle Back F/2

Frequency	Condition	Voltage (V)	Power (W)	Doze Power	Nap Power	Notes
1.6 GHz	Maximum at 65°C	1.00	15	8	7	1, 2, 3
1.8 GHz	Maximum at 65°C	1.10	22	13	11	1, 2, 3
2.0 GHz	Maximum at 65°C	1.10	29	16	13	1, 2, 3

Note: Maximum power at 85°C is the *only* value that is guaranteed by manufacturing test. Values for typical at 65°C, nap, and doze are not guaranteed by test. These values are to be used as characterization-based nominal values and are included for comparison purposes only.

1. Maximum power is projected at the nominal V_{DD} worst case I_{DDq}, and the maximum temperature as specified.
2. Voltage tolerance is ±50 mV.
3. These are core power only; OV_{DD} power of 1 - 3 watts is not included.

3.2 ac Electrical Characteristics

This section provides the ac electrical characteristics for the PowerPC 970FX. After fabrication, parts are sorted by maximum processor core frequency as shown in *Section 3.3* on page 26 and tested for conformance to the ac specifications for that frequency. The processor core frequency is determined by the SYSCLK and the settings of the PLL_MULT signal.

This section describes only asynchronous and mode-select inputs and outputs. For bus timing information, see the *PowerPC 970FX RISC Microprocessor Users Manual*.

3.3 Clock ac Specifications

Table 3-8 provides the clock ac timing specifications as defined in *Figure 3-1 Clock Differential HSTL Signal* on page 27.

Table 3-8. Clock ac Timing Specifications (Page 1 of 2)

Callout Number	Characteristic	Value		Unit	Notes
		Minimum	Maximum		
—	SYSCLK frequency	100	300	MHz	1, 2, 4
—	SYSCLK input jitter (cycle to cycle)	—	±75	ps	4
1	SYSCLK rise and fall time	—	500	ps	3, 4
2	SYSCLK and $\overline{\text{SYSCLK}}$ input high voltage	—	OV_{DD} + 0.3	V	4

Notes:

1. **Important:** Processor frequency is determined by the PLL_MULT and SYSCLK input frequencies. PLL_RANGE(1:0) must be set to the correct values for the expected processor frequency. Consult *Table 5-2. PowerPC 970FX RISC Microprocessor PLL Configuration on page 64* for the allowable frequency range for these pins.
2. PowerPC 970FX minimum processor frequency will be determined by characterization. The minimum frequency is an estimation.
3. The rise and fall times for the SYSCLK inputs are measured from 0.4 to 1.0 V.
4. **Important:** The data in this table is based on simulation and might be revised after hardware characterization.
5. For a timing diagram, see *Figure 3-1* on page 27.
6. Guaranteed by design and not tested.
7. The differential voltage is the minimum peak-to-peak voltage on both the SYSCLK and $\overline{\text{SYSCLK}}$ pins (similar to what is measured with single-ended oscilloscope probes).

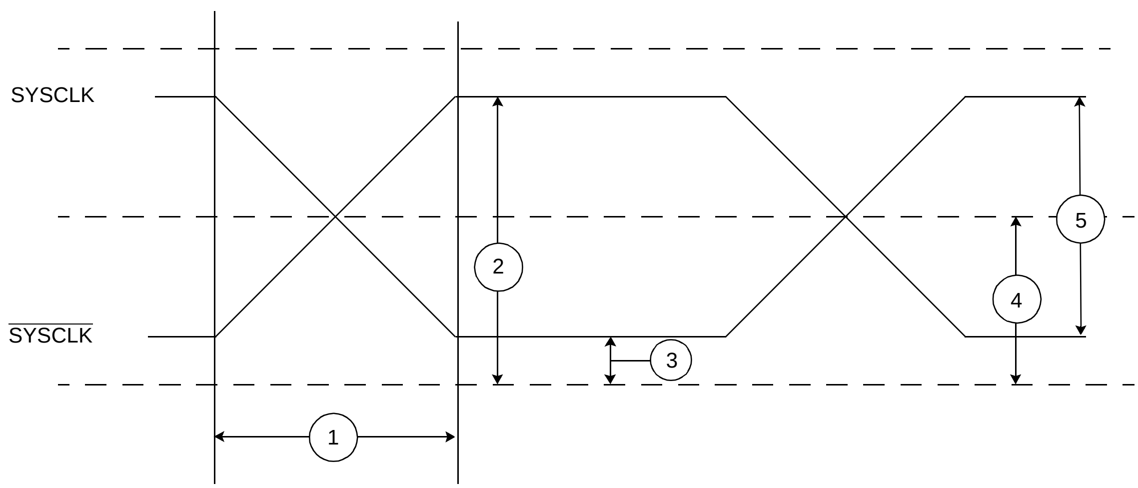
Table 3-8. Clock ac Timing Specifications (Page 2 of 2)

Callout Number	Characteristic	Value		Unit	Notes
		Minimum	Maximum		
3	SYSCLK and $\overline{\text{SYSCLK}}$ input low voltage	-0.3	—	V	4
4	Differential crossing-point voltage	$0.4 \times OV_{DD}$	$0.6 \times OV_{DD}$	V	4
5	Differential voltage	0.385	1.6	V	4, 7
—	PLL lock time	—	800	µSec	4, 7
—	Duty cycle	40%	60%	—	—

Notes:

1. **Important:** Processor frequency is determined by the PLL_MULT and SYSCLK input frequencies. PLL_RANGE(1:0) must be set to the correct values for the expected processor frequency. Consult *Table 5-2. PowerPC 970FX RISC Microprocessor PLL Configuration on page 64* for the allowable frequency range for these pins.
2. PowerPC 970FX minimum processor frequency will be determined by characterization. The minimum frequency is an estimation.
3. The rise and fall times for the SYSCLK inputs are measured from 0.4 to 1.0 V.
4. **Important:** The data in this table is based on simulation and might be revised after hardware characterization.
5. For a timing diagram, see *Figure 3-1* on page 27.
6. Guaranteed by design and not tested.
7. The differential voltage is the minimum peak-to-peak voltage on both the SYSCLK and $\overline{\text{SYSCLK}}$ pins (similar to what is measured with single-ended oscilloscope probes).

Figure 3-1. Clock Differential HSTL Signal



Notes:

The legend for this figure is provided by callout number in *Table 3-8* on page 26.

To determine the processor clock, multiply the SYSCLK frequency by one of the following values:

- 12 for PLL_MULT = ‘0’
- 8 for PLL_MULT = ‘1’

For more information about the PLL configuration, see *Table 5-2 PowerPC 970FX RISC Microprocessor PLL Configuration* on page 64.

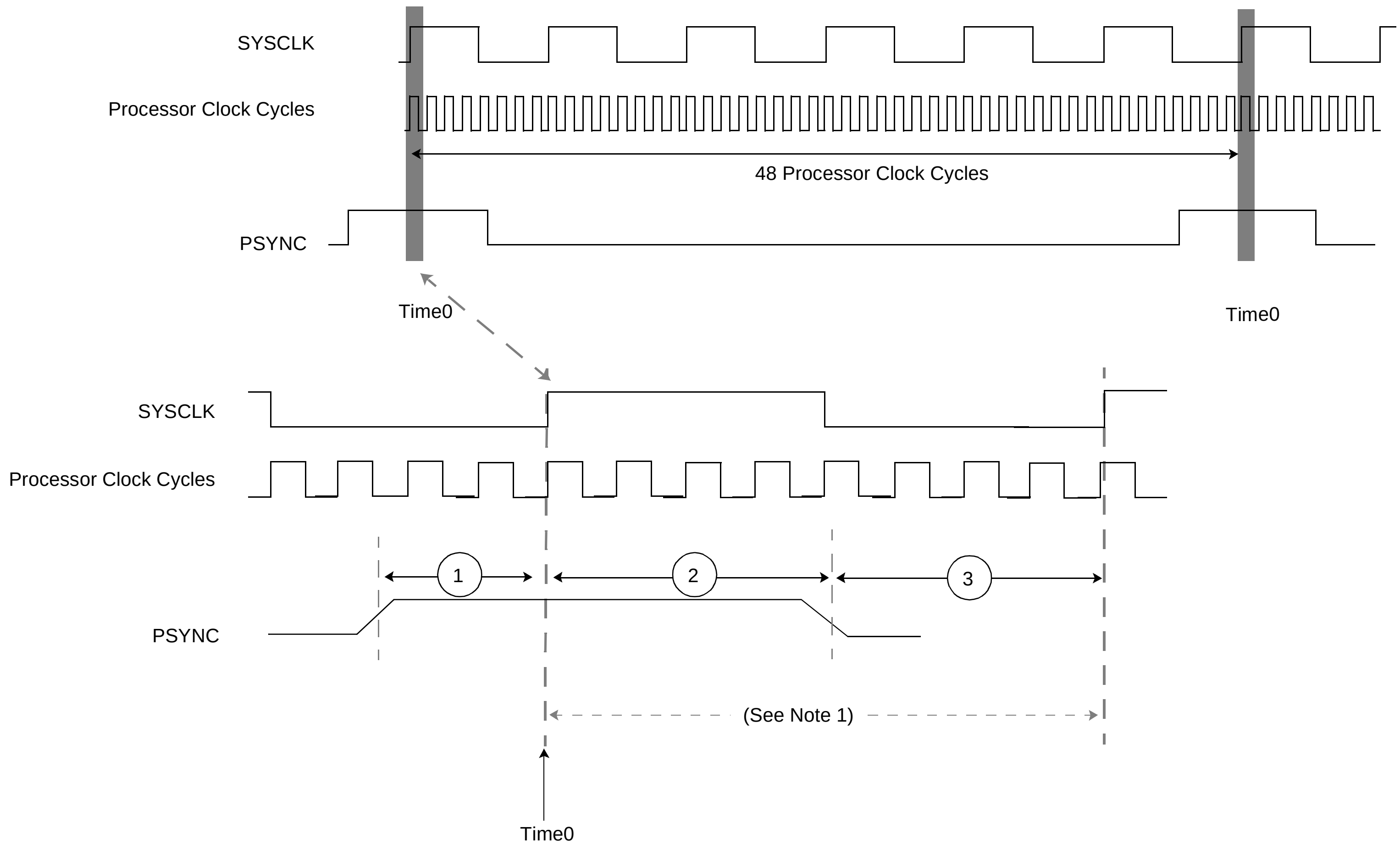
3.4 Processor-Clock Timing Relationship between PSYNC and SYSCLK

Table 3-9 and *Figure 3-2* on page 29 describes the processor-clock timing relationship between PSYNC and SYSCLK.

Table 3-9. Processor-Clock Timing Relationship Between PSYNC and SYSCLK

Callout Number	Characteristic		Value		Unit
			Minimum	Maximum	
1	Setup time	t_{SETUP}	0.8	—	ns
2	Hold time	t_{HOLD}	0.8	—	ns
3	Guard time	t_{GUARD}	0.8	—	ns
Note: For a timing diagram, see *Figure 3-2* on page 29.					

Figure 3-2. Processor-Clock Timing Relationship between PSYNC and SYSCLK



Notes:

1. The maximum rate of occurrence between PSYNCs is 48 processor clock cycles independent of the PLL multiplier (12 or 8). One pulse per 24 SYSCLKS is suggested.
2. The legend for this figure is provided by callout numbers in *Table 3-9* on page 28.

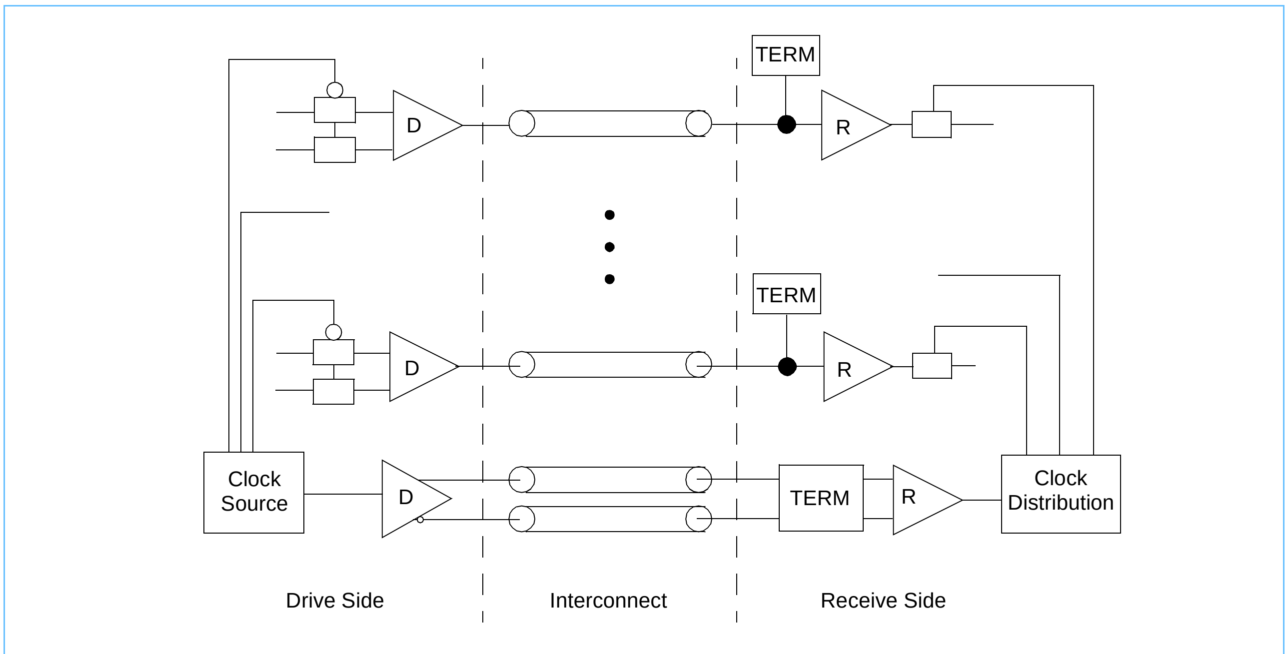
3.5 Processor Interconnect Specifications

3.5.1 Electrical and Physical Specifications

3.5.1.1 Source Synchronous Bus

Figure 3-3 provides a representative block diagram of a source synchronous bus (SSB) for a PowerPC 970FX RISC Microprocessor processor interconnect implementation. Each SSB consists of three major subsections: the drive side, the module-to-module interconnect, and the receive side. First, data is either balance-coding-method encoded or checksummed, then clock-phase multiplexed, and finally launched from the drive side onto the module interconnect. The receive side includes far-end termination and circuitry to demultiplex, deskew data, align clocks, and synchronize the received data.

Figure 3-3. Block Diagram of an SSB for a Processor Interconnect Implementation



3.5.1.2 Drive Side Characteristics

Figure 3-4 shows a typical implementation for a single-ended line. The drivers are of the push-pull type with a nominal impedance (R0 of 20 Ω) that overdrives the line impedance. The nominal swing at the receiver, terminated with resistance (TR0 of 110 Ω) to each rail, is 13% OV_{DD} to 87% OV_{DD}. R0 is 20 Ω when the signal driver is in the low output impedance mode. The 20 Ω setting is suitable for all bus speeds. The PowerPC 970FX has a 40 Ω nominal output impedance mode that is suitable for bus speeds less than 800 megatransfers per second in some applications.

The maximum skew between any of the outputs is 150 ps at the ball grid array pin. The maximum interconnect skew on the system board between any two outputs must be less than 150 ps. The interconnect skew on the system board between any two inputs must be less than 300 ps.

Figure 3-4. Typical Implementation for a Single-Ended Line

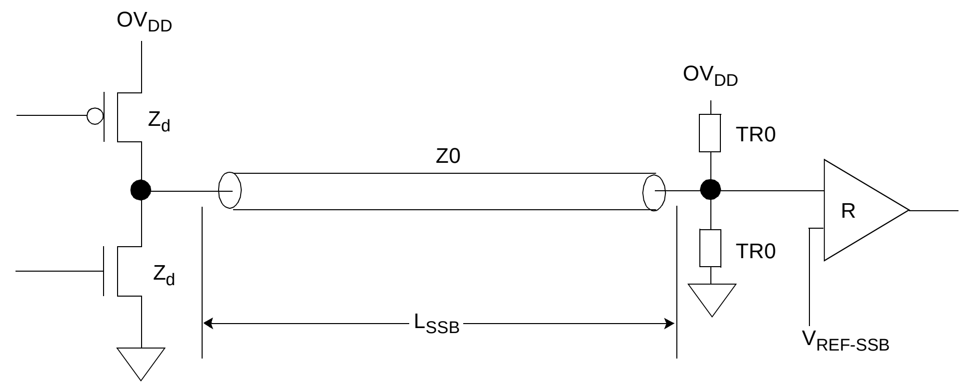


Table 3-10. Processor Interconnect SSB Driver Specifications

Symbol	Description	Minimum	Typical	Maximum	Units	Notes
$V_{OH}DC$	High output level at dc		0.87 OV_{DD}		mV	
$V_{OL}DC$	Low output level at dc		0.13 OV_{DD}		mV	
T_{DR}	Signal driver rise time	70	133	171	ps	20% to 80% of swing
T_{DF}	Signal driver fall time	81	155	162	ps	20% to 80% of swing
Z_D	Signal driver output impedance	15	20	25	Ω	Low-Ω mode
Z_D	Signal driver output impedance	30	40	50	Ω	High-Ω mode

3.5.1.3 Module-to-Module Interconnect Characteristics

All traces are to be routed as striplines or microstrip. The tolerance on trace impedance is 10%. Care must be taken when mixing transmission line styles to manage propagation delay differences. The clock delay should be longer than the longest data delay for bus speeds at or higher than 1.1 Gbps or on lines longer than 13 cm.

Table 3-11. Processor Interconnect SSB Printed Circuit Board Trace Specifications

Symbol	Description	Minimum	Typical	Maximum	Units	Notes
L_{SSB}	Trace length			18	cm	For transfer speeds of 1.5 Gps.
				22.5	cm	For transfer speeds of 1.0 Gps.
Z_0	Trace impedance	45	50	55	Ω	
S_{DPCB}	Printed circuit board data trace skew			150	ps	

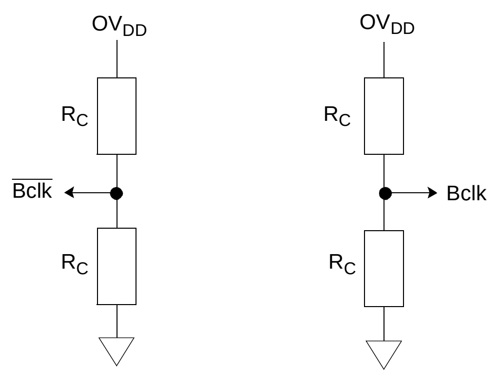
3.5.1.4 Receive Side Characteristics

The receive side contains far-end termination circuitry as shown in *Figure 3-4* on page 31 for the single-ended lines. The total skew from the drive side to the module input pins on the receive side is 350 ps (S_{DS} + S_{PCB}) between any two signals (clocks or data). The differential clock termination scheme is shown in *Figure 3-5* on page 32. All receivers are pseudo-differential with reference to $V_{REF\text{-}SSB}$ and with common-mode rejection of at least $0.5 \times V_{DD}$. $V_{REF\text{-}SSB}$ can be generated internally by the receive-side circuitry or can be derived from the supply voltage.

Table 3-12. Processor Interconnect SSB Receiver Specifications

Symbol	Description	Minimum	Typical	Maximum	Units	Notes
$V_{REF\text{-}SSB}$	SSB reference voltage		$0.5 \times OV_{DD}$		mV	$(V_{OH}DC + V_{OL}DC)/2$
$Bclk_{DC}$	Bus clock duty cycle	48	50	52	%	
TR0	Single-ended terminator	83	110	137	Ω	110±25%

Figure 3-5. Differential Clock Termination Circuitry

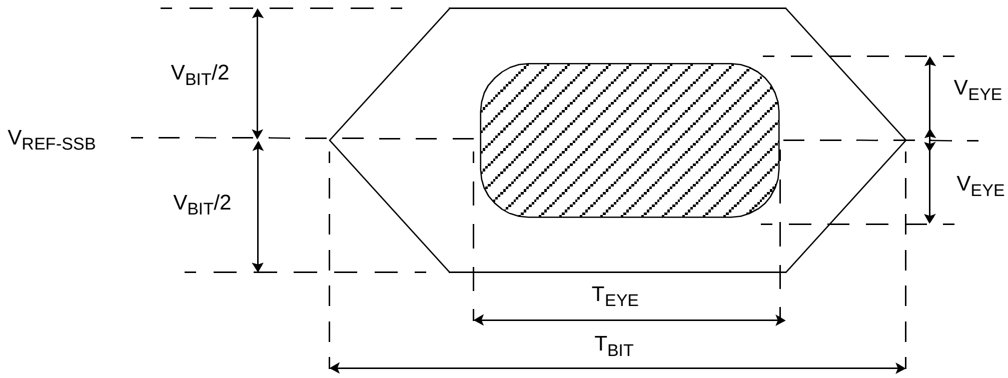


For high-performance operation, the PI supports the inclusion and operation of receive-side circuitry for clock alignment and individual bit-level deskew. An initialization alignment procedure (IAP) is activated at power-on reset for bit-level deskew and clock alignment. The IAP uses delay elements in the receive-side circuitry to first equalize the delay of the incoming data signals and then center the clock transition in the timing window. The timing parameters for the delay elements and flip-flops that register the data signals are summarized in *Table 3-13* on page 32.

Table 3-13. Processor Interconnect SSB Timing Parameters for the Deskew and Clock Alignment

Symbol	Description	Minimum	Typical	Maximum	Units	Notes
T_{BIT}	Bit time		$1/(2 \times Bclk)$		ns	
T_{DED}	Delay element time increment	18	25	35	ps	Thirty-one delay elements for data
T_{DEC}	Delay element time increment	18	25	35	ps	Sixty-four delay elements for clock

Figure 3-6. Post-IAP Eye Opening



The reference level for V_{EYE} is $V_{REF-SSB}$. The horizontal (T_{EYE}) eye opening is a function of the bit time (T_{BIT}) and the earliness of the bus clock transition relative to the slowest data signal.

Table 3-14. Eye-Size Requirements

Bit Rate (Mbps)	Processor to Bus Ratio	Processor Core (MHz)	Step Time (ps)	Eye Requirement (ps)	Bit Time (ps)	Eye/Bit Time	V_{EYE} (Minimum)
400	3	1200	31.9	863	2500	34.5%	150 mV
450	3	1350	31.9	797	2222.2	34.5%	150 mV
500	3	1500	31.9	744	2000	37.2%	150 mV
500	2	1000	31.9	744	2000	37.2%	150 mV
666	3	1998	27.8	605	1501.5	40.3%	150 mV
666	2	1332	31.9	625	1501.5	41.6%	150 mV
866	2	1732	31.9	544	1154.7	47.1%	150 mV
1066	2	2132	26.0	465	938.1	49.6%	150 mV

3.6 Input ac Specifications

This section provides specifications for pins: $\overline{\text{INT}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, TBEN, $\overline{\text{THERM\_INT}}$, and TRIGGERIN.

Table 3-15, *Table 3-16*, and *Table 3-17* provide the input ac timing specifications as defined in *Figure 3-7* on page 35.

Table 3-15. Input ac Timing Specifications

Callout Number	Characteristic	Value		Unit
		Minimum	Maximum	
1	Rise time	—	< 1	ns
2	Pulse width	10	—	ns
3	Fall time	—	< 1	ns

Table 3-16. Input ac Timing Specifications for TBEN

Callout Number	Characteristic	Value		Unit
		Minimum	Maximum	
1	Rise time	—	< 1	ns
2	Pulse width	$8 \times T_{full}$[1]	—	ns
3	Fall time	—	< 1	ns

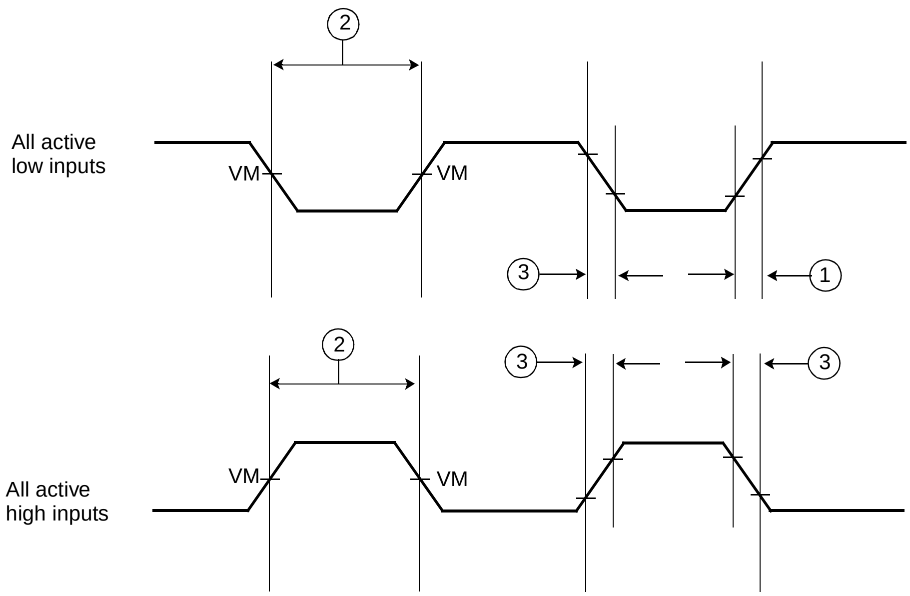
1. T_{full} is the clock period of the full frequency processor clock.

Table 3-17. Input ac Timing Specifications for $\overline{\textit{HRESET}}$

Callout Number	Characteristic	Value		Unit
		Minimum	Maximum	
1	Rise time	—	< 1.5	ns
2	Pulse width	50	—	ns
3	Fall time	—	< 1.5	ns

Note: For bus timing information, see *Section 3.5* of the *PowerPC 970FX RISC Microprocessor Users Manual*.

Figure 3-7. Asynchronous Input Timing



Notes:

1. There is no reference to SYSCLK because these inputs are sampled using the internal processor clock.
2. Define maximum rise and fall time as < 1 ns.
3. Define minimal pulse length > 10 ns.
4. The midpoint voltage (VM) is (OV_{DD}/2).
5. These timings refer to the following pins: $\overline{\text{INT}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$, $\overline{\text{HRESET}}$,$\overline{\text{SRESET}}$, TBEN, $\overline{\text{THERM\_INT}}$, and TRIGGERIN.
6. The legend for this figure is provided by callout number in *Table 3-15* on page 34.

3.6.1 TBEN Input Pin

The TBEN input pin can be used as either an enable for the internal timebase/decrementer or as an external clock input. The mode is controlled by the setting of HID0 bit 19. When this bit is ‘0’, the timebase and decrementer update at 1/8th the processor core frequency whenever TBEN is high (traditional enable mode). When HID0 bit 19 is ‘1’, the timebase and decrementer are clocked by the rising edge of TBEN (external clock input mode). When the external clock input mode is used, the TBEN input frequency must not exceed 1/16th of the core processor maximum frequency.

3.7 Asynchronous Output Specifications

This section describes the asynchronous outputs and bidirectional signals. Timing information is not provided because these signals are launched by the internal processor clock.

Table 3-18, *Table 3-19*, and *Table 3-20* list the asynchronous outputs and bidirectionals (BiDi) signals.

Table 3-18. Asynchronous Type Output Signals

Pin	Description	Comment	Pin
ATTENTION	Attention	To service processor	AD12
$\overline{\text{QREQ}}$	Quiesce request	Power management	AB12
TRIGGEROUT		Debug only	N19
Note: There is no reference to SYSCLK because this output is launched by the (internal) processor clock.			

Table 3-19. Asynchronous Open Drain Output Signals

Pin	Description	Comment	Pin
I2CGO	I^2C interface go	Arbitration I^2C and JTAG	N22
Notes: The rise and fall times are measured between the 20% to 80% points of the input signal swing. There is no reference to SYSCLK because this output is launched by the (internal) processor clock. Pull-up resistor = 10 kΩ			

Table 3-20. Asynchronous Open-Drain Bidirectional Signals

Pin	Description	Comment	Pin
$\overline{\text{CHKSTOP}}$	Checkstop signal input/output		R20
Notes: There is no reference to SYSCLK because this output is launched by the (internal) processor clock. Pull-up resistor = 10 kΩ			

3.8 Mode Select Input Timing Specifications

This section provides timing specifications for the mode-select pins. These pins are sampled by $\overline{\text{HRESET}}$.

Table 3-21 provides the input ac timing specifications as defined in *Figure 3-8* on page 38. The mode-select signals and debug pins are listed in *Table 3-22* on page 39 and *Table 3-23* on page 39.

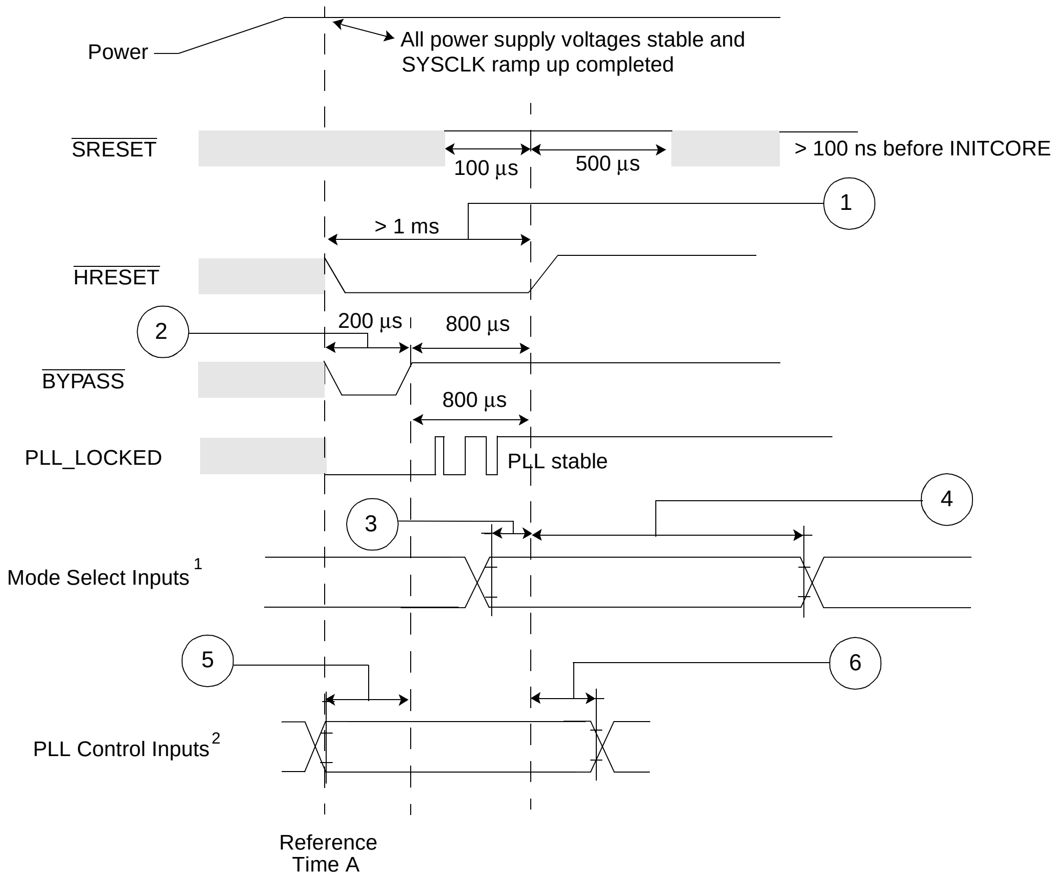
Table 3-21. Input ac Timing Specifications

Callout Number	Characteristic	Value		Unit	Notes
		Minimum	Maximum		
1	$\overline{\text{HRESET}}$ width	>1	—	ms	4
2	$\overline{\text{BYPASS}}$ width	200	—	µs	4
3	Mode select signal setup	20	—	Processor clocks	1, 5
4	Mode select inputs hold time	1000	—	Processor clocks	1
5	PLL control signal setup	20	—	Processor clocks	2, 3
6	PLL control inputs hold time	20	—	Processor clocks	2, 3

Notes:

1. Mode select pins must not change level sooner than 20 processor clocks before the falling edge of $\overline{\text{HRESET}}$ and must be held for a minimum of 1000 processor clocks after the rising edge of $\overline{\text{HRESET}}$.
2. PLL control pins must not change level earlier than 20 processor clocks before the rising edge of $\overline{\text{BYPASS}}$ and must be held for a minimum of 20 processor clocks after the rising edge of $\overline{\text{HRESET}}$.
3. PLL control inputs must not change while $\overline{\text{HRESET}}$ is low.
4. For timing diagrams, see *Figure 3-8* on page 38 and *Figure 3-9* on page 40.
5. Guaranteed by design and not tested.

Figure 3-8. $\overline{\text{HRESET}}$ *and* $\overline{\text{BYPASS}}$ *Timing Diagram*



Notes:

1. These timings refer to the following pins: BUS_CFG(0:2), PROCID(0:2).
2. These timings refer to the following pins: CKTERM_DIS, PLL_MULT, and PLL_RANGE(1:0). These pins can only be changed by driving $\overline{\text{HRESET}}$ and $\overline{\text{BYBASS}}$ low.
3. $\overline{\text{HRESET}}$ and $\overline{\text{BYPASS}}$ can be low during initial program load stages and need not change during powerup before reference time A.
4. PLL control inputs must not change while $\overline{\text{HRESET}}$ is low.
5. The legend for this figure is provided by callout number in *Table 3-21* on page 37.

Table 3-22. Mode Select Type Input Signals

Pin	Description	Comment	Pin
BUS_CFG(0:2)	Bus configuration	Select processor clock to bus clock ratio.	AA19, AC19, AB16
CKTERM_DIS	Clock receiver termination	Disable internal clock receiver terminator.	AA14
PLL_MULT	Select between multiplier 8 or 12		AA8
PLL_RANGE(1:0)	PLL range select		AA9, AB7
PROCID(0:2)	Processor identifier (ID)	For a multiprocessor environment.	L19, M19, M18

Table 3-23. Debug Pins

Pin	Description	Comment	Pin
$\overline{\text{AVP\_RESET}}$		For manufacturing test only.	W23
EI_DISABLE		Disables use of initial alignment procedure (IAP) to adjust clock skew on the processor interface.	P20
GPULDBG	PPC 970FX debug	Pull up to OV_{DD} for debug mode, JTAG - I^2C interaction	AA22

3.9 Spread Spectrum Clock Generator

3.9.1 Design Considerations

When designing with the spread spectrum clock generator (SSCG), there are several design issues that must be considered as described in this section. SSCG creates a controlled amount of long-term jitter. For a receiving PLL in the PowerPC 970FX to operate in this environment, it must be able to accurately track the SSCG clock jitter.

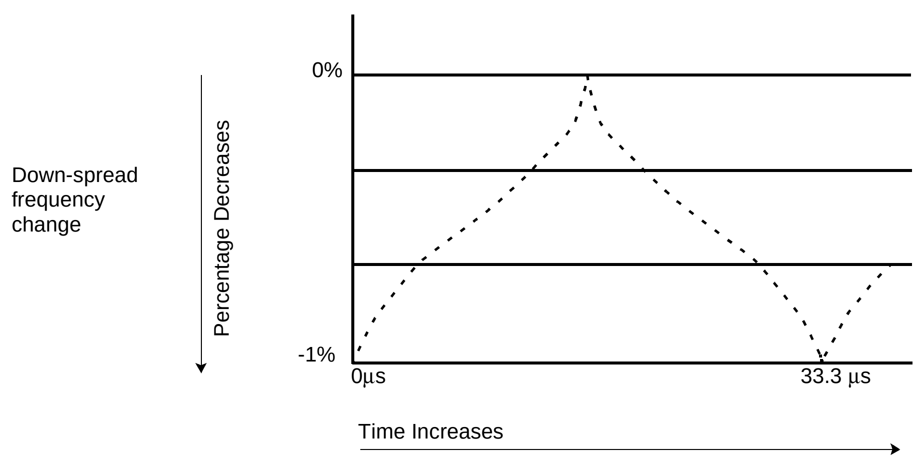
Note: The accuracy to which the PowerPC 970FX PLL can track the SSCG clock is called the *tracking skew*.

The following SSCG configuration is recommended:

- Down spread mode, less than or equal to 1% of the maximum frequency
- A modulation frequency of 30 kHz
- A cubic sweep profile, also called a *Hershey Kiss* profile (as in a Lexmark[1] profile), as described in *Figure 3-9*.

In this configuration the tracking skew is less than 100 ps.

Figure 3-9. Spread Spectrum Clock Generator Modulation Profile



1. See patent 5,631,920.

3.10 I^2C and JTAG

3.10.1 I^2C Bus Timing Information

The I^2C-bus specification can be downloaded from the NXP Web site at http://www.nxp.com/products/interface_control/i2c/.

The PowerPC 970FX I^2C bus is limited to a speed of 50 kHz for the standard-mode timing specification and does not support the high-speed (Hs-mode) or fast-mode timing.

The PowerPC 970FX I^2C pins are limited to OV_{DD} voltages. Level shifting or pullups or both might be required to interface to higher voltage devices. See *The I^2C-bus specification* for recommendations on level shifting and pullups.

Note: To avoid problems in determining the correct pull-up resistor value, wiring level-shifted PowerPC 970FX I^2C bus pins together with non-PowerPC 970FX parts in a system is discouraged. Each PowerPC 970FX should have its own private level shifter.

3.10.2 IEEE 1149.1 ac Timing Specifications

Table 3-24 provides the IEEE 1149.1 JTAG ac timing specifications as defined in *Figure 3-10* on page 42 and *Figure 3-11* on page 43. The five JTAG signals are listed here:

- TDI (test data in)
- TDO (test data out)
- TMS (test mode select)
- TCK (test clock)
- TRST (test reset)

Note: The following recommendations address some of the PowerPC 970FX's nonstandard IEEE ac timing implementations:

- See *Section 3.10.3 I^2C and JTAG Considerations* on page 43 to determine pullups and pulldowns for configuration of TCK, TDI, and TMS.
- JTAG scan chains should not be daisy chained in systems using multiple PowerPC 970FX's in multiprocessor configurations if I^2C is supported. The JTAG scan chains should be connected in parallel (all TCKs tied together, all TDIs tied together, and so forth) and use separate TMS inputs to select each 970 processor for JTAG access.
- JTAG operations require that the core clock be operating normally with the PLL in bypass mode. CLKIN and $\overline{\text{CLKIN}}$ must receive at least 16 pulses for TCK down level and 16 pulses for TCK up level.

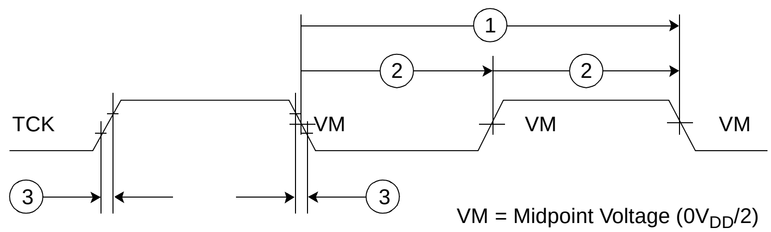
Table 3-24. JTAG ac Timing Specifications (Dependent on SYSCLK)

Callout Number	Characteristic	Minimum	Maximum	Unit	Notes
—	TCK frequency of operation	—	1/16	Core processor frequency	1, 5
1	TCK cycle time	32	—	Processor clocks	2, 5
2	TCK clock pulse width	15	—	Processor clocks	2, 5
3	TCK rise and fall times	0	2	ns	3, 5
4	TMS, TDI data setup time	0	—	ns	5
5	TMS, TDI data hold time	15	—	ns	5
6	TCK to TDO data valid	2.5	12	ns	4, 5
7	TCK to TDO high impedance	3	9	ns	3, 5
8	TCK to output data not valid (output hold)	0	—	ns	5

Notes:

1. TCK frequency is limited by the core processor frequency.
2. Processor clock cycles.
3. Guaranteed by characterization and not tested.
4. The minimum specification is guaranteed by characterization and not tested.
5. The JTAG timings are dependent on an active SYSCLK.
6. For a timing diagram, see *Figure 3-10* and *Figure 3-11* on page 43.

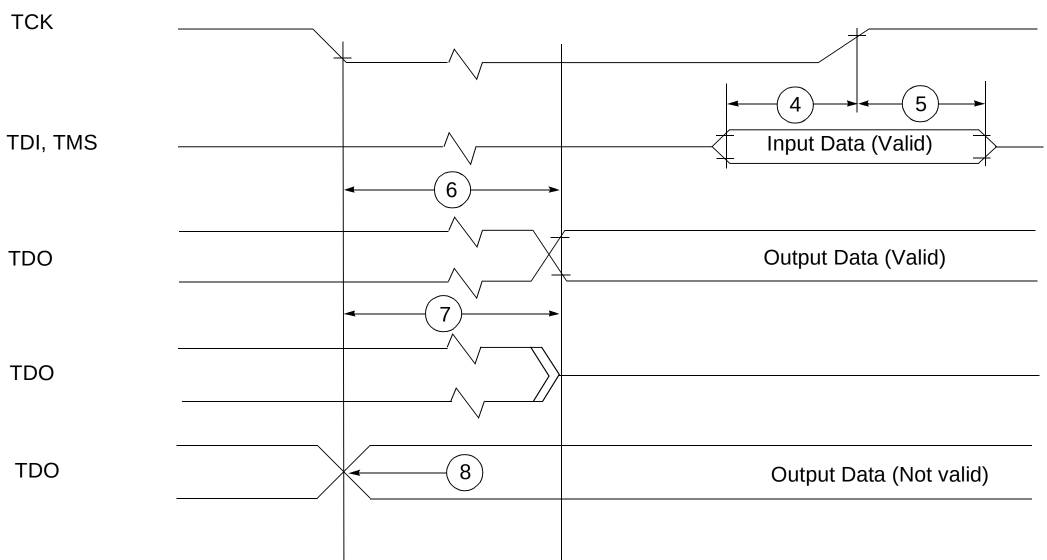
Figure 3-10. JTAG Clock Input Timing Diagram



Note: The legend for this figure is provided by callout number in *Table 3-24*.

Figure 3-11 provides the test access port timing diagram.

Figure 3-11. Test Access Port Timing Diagram



Note: The legend for this figure is provided in *Table 3-24 JTAG ac Timing Specifications (Dependent on SYSCLK)* on page 42.

3.10.3 I²C and JTAG Considerations

For systems using only JTAG, TDO should be pulled up (tied to OV_{DD}), and the I^2C data and clock pins should also be tied to OV_{DD}. For systems using only I^2C, the signals TCK, TMS, TDO, and TDI should be pulled down. If the system needs to support both JTAG and I^2C access, pull-down resistors must be connected to the JTAG pins. These resistors maintain the correct state on the JTAG pins when I^2C access is active. These pull-down resistors must be able to be overdriven for JTAG operation. Additionally, the JTAG driver hardware connected to the 970FX should drive its outputs low (on TCK, TMS, TDI) when JTAG is idle.

Note: $\overline{\text{TRST}}$ should always be pulled up to OV_{DD} on the PowerPC 970FX.

3.10.4 Boundary Scan Considerations

The PowerPC 970FX does not support the boundary scan description language (BSDL) standard for implementing boundary scan testing. The IBM technical library contains an application note titled *PowerPC 970FX Boundary Scan* that describes a method of producing the equivalent function.

4. Dimensions and Physical Signal Assignments

The IBM PowerPC 970FX uses a ceramic ball grid array (CBGA) that supports 576 balls. Two different substrates are used for the PowerPC 970FX. Both packages are shown in *Figure 4-1*, *Figure 4-2*, and *Figure 4-3*. Note that they are identically dimensioned.

4.1 Electrostatic Discharge Considerations

Appropriate electrostatic discharge (ESD) handling procedures should be implemented and maintained for any facilities handling this component.

This product has been ESD tested to meet or exceed the Joint Electron Device Engineering Council (JEDEC) specifications JESD22-A114C.01, JESD22-C101C, and JESD22-A115-A for the following models:

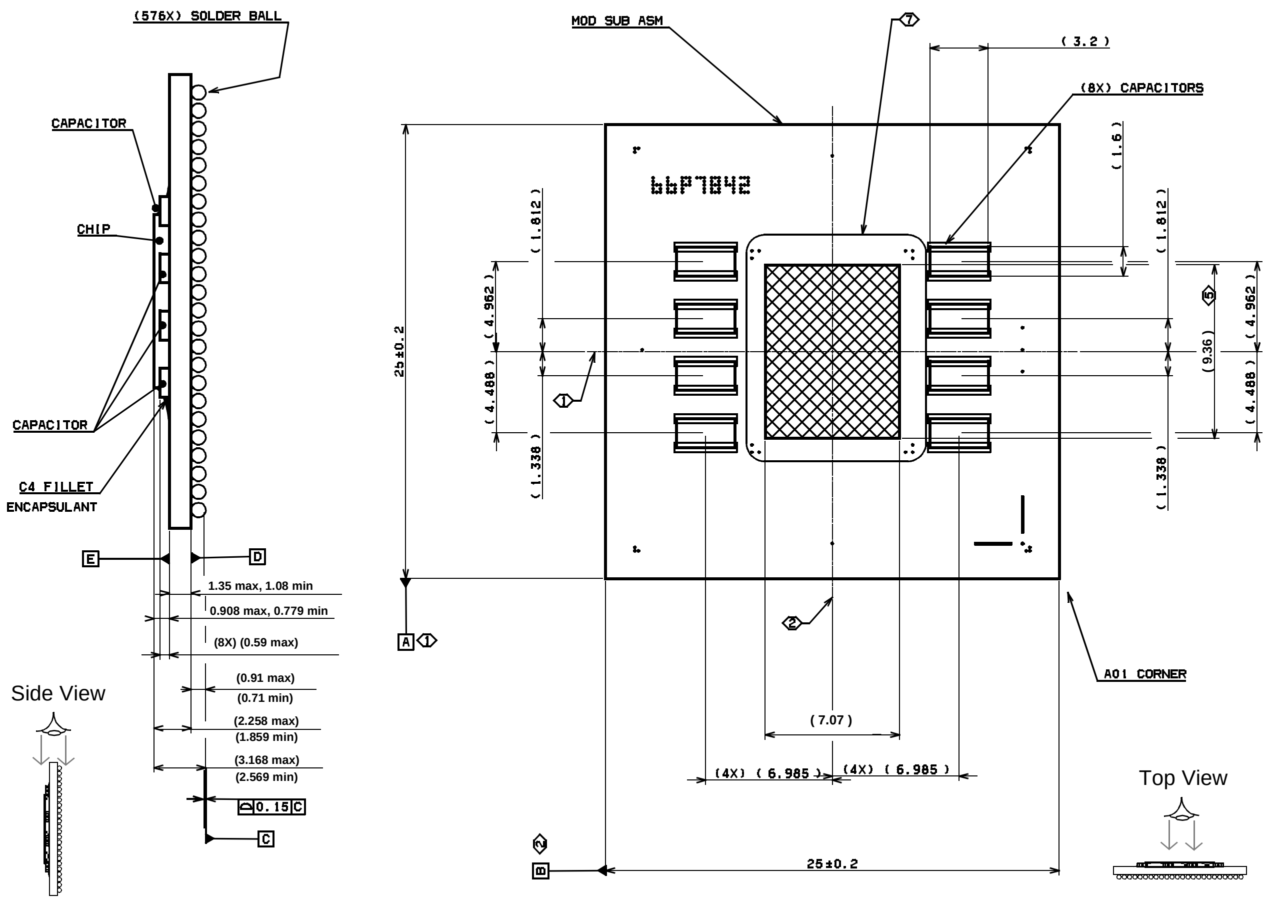
- Human body model (HBM) - Class 1B
- Field-induced charged device model (CDM) - Class II
- Machine model (MM) - Class A.

4.2 Mechanical Packaging

4.2.1 Standard Lead Package Version

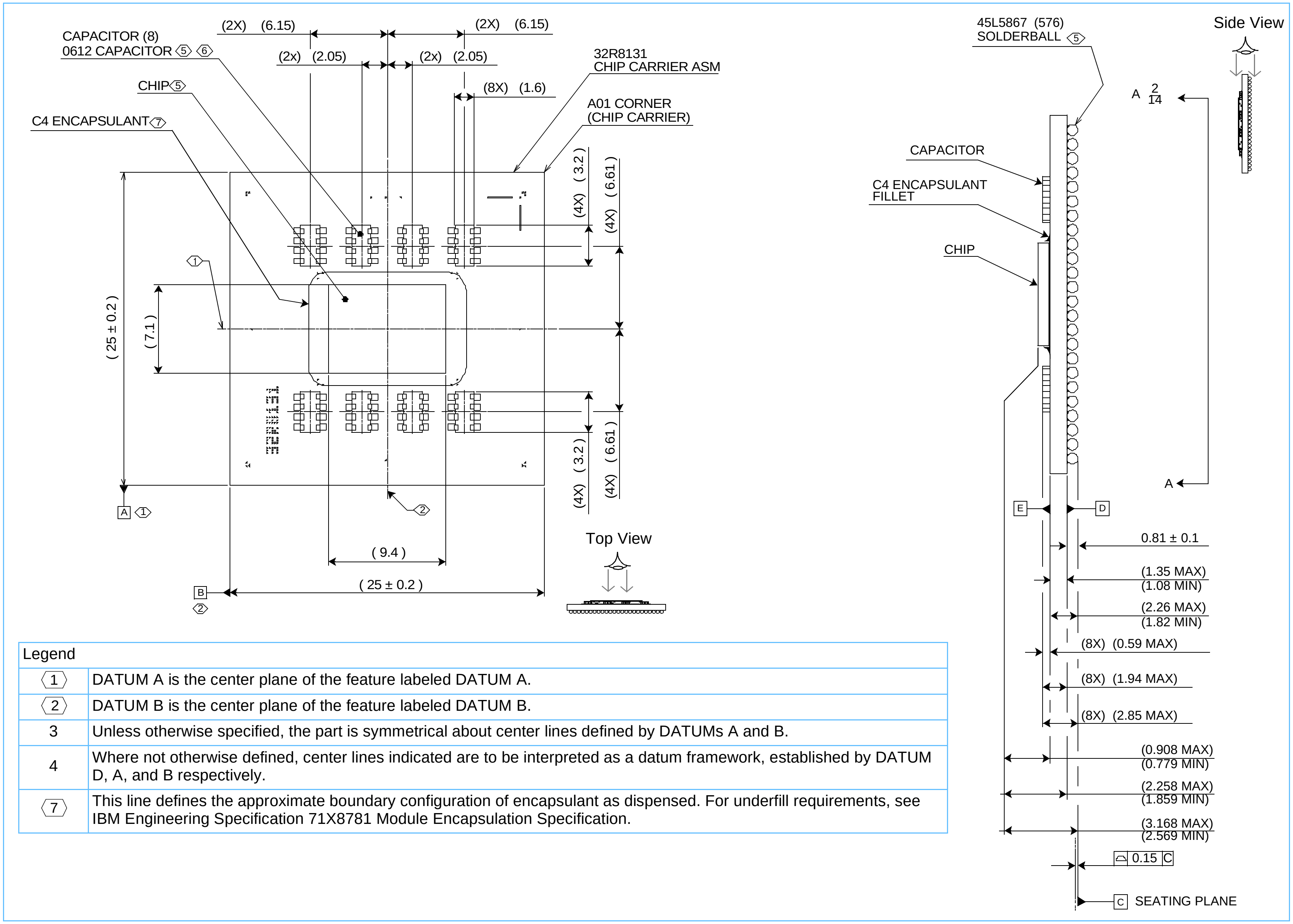
Figure 4-1 on page 46 and *Figure 4-2* on page 47 show the side and top views of the packages including the height from the top of the die to the bottom of the solder balls. *Figure 4-3* on page 48 shows a bottom view of the PowerPC 970FX.

Figure 4-1. PowerPC 970FX Microprocessor Mechanical Package for Standard Lead DD3.0x Parts (top and side)



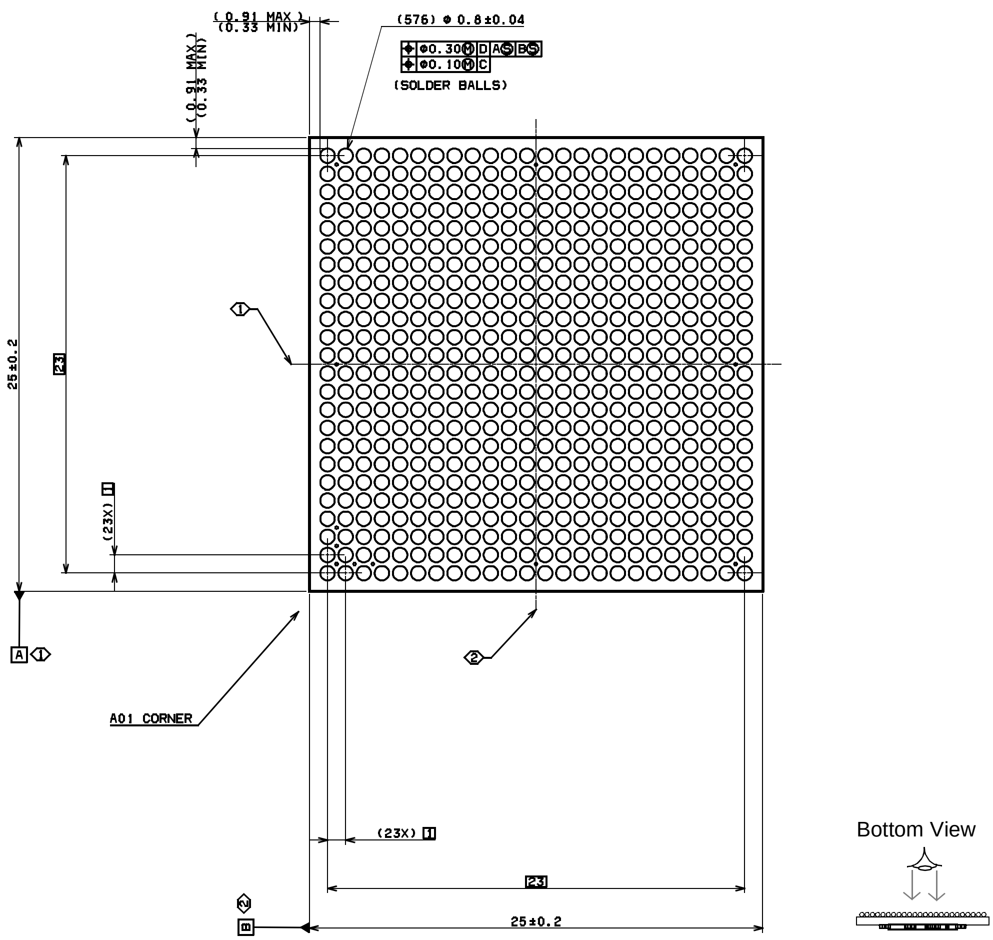
Legend	
1	DATUM A is the center plane of the feature labeled DATUM A.
2	DATUM B is the center plane of the feature labeled DATUM B.
3	Unless otherwise specified, the part is symmetrical about center lines defined by DATUMs A and B.
4	Where not otherwise defined, center lines indicated are to be interpreted as a datum framework, established by DATUM D, A, and B respectively.
7	This line defines the approximate boundary configuration of encapsulant as dispensed.

Figure 4-2. PowerPC 970FX Microprocessor Mechanical Package for Standard Lead, DD3.1x Parts (top and side)



Legend	
1	DATUM A is the center plane of the feature labeled DATUM A.
2	DATUM B is the center plane of the feature labeled DATUM B.
3	Unless otherwise specified, the part is symmetrical about center lines defined by DATUMs A and B.
4	Where not otherwise defined, center lines indicated are to be interpreted as a datum framework, established by DATUM D, A, and B respectively.
7	This line defines the approximate boundary configuration of encapsulant as dispensed. For underfill requirements, see IBM Engineering Specification 71X8781 Module Encapsulation Specification.

Figure 4-3. PowerPC 970FX Microprocessor Bottom Dimensions for Standard Lead CBGA Package



Legend	
1	DATUM A is the center plane of the feature labeled DATUM A.
2	DATUM B is the center plane of the feature labeled DATUM B.
3	Unless otherwise specified, the part is symmetrical about center lines defined by DATUMs A and B.

4.2.2 Reduced-Lead Package Version

This section describes the reduced-lead package, as indicated by the ‘R’ in the package code field of the part number. For the reduced-lead package, lead-free solder is used for the substrate capacitors and the ball grid array (BGA) balls on the bottom of the package. Standard high-melting-point 97% Pb and 3% Sn solder (exempted by European Union restriction of hazardous substances [RoHS] legislation) is used for the C4 balls that interconnect the die to the substrate. The resulting module is RoHS compatible.

All datasheet electrical specifications apply equally to standard and reduced-lead parts.

4.2.2.1 Mechanical Specifications

The solder balls on the bottom of the reduced-lead package are slightly smaller, which will decrease the overall module height when assembled onto a system board. Heatsink solutions should be modified accordingly

Table 4-1. Standard-Lead and Reduced-Lead Package, Layout, and Assembly Differences

Package	JEDEC Moisture Sensitivity Level (MSL)	Solder Ball Composition	Solder Ball Diameter mm (inch)	CBGA Substrate I/O Pad Diameter mm (inch)	Card Solder Mask Opening Diameter mm (inch)	Card Solder Screen Diameter	Card Pad Diameter mm (inch)
Standard Lead	1	Sn 10% Pb 90%	0.80 (0.0315)	0.80 (0.0315)	0.80 (0.0315)	26.5 mil opening in 7.5 mil thick stencil, 2500-4600 cubic mils	0.70 (0.0275)
Reduced Lead	3	Sn 95.5% Ag 3.8% Cu 0.7%	0.635 (0.025)	0.80 (0.0315)	0.72 (0.028)	23 mil opening in 4 mil thick stencil, 1400-2000 cubic mils	0.61 (0.024)
Note: All dimensions in mm unless noted. Dimensions in parenthesis are in inches.							

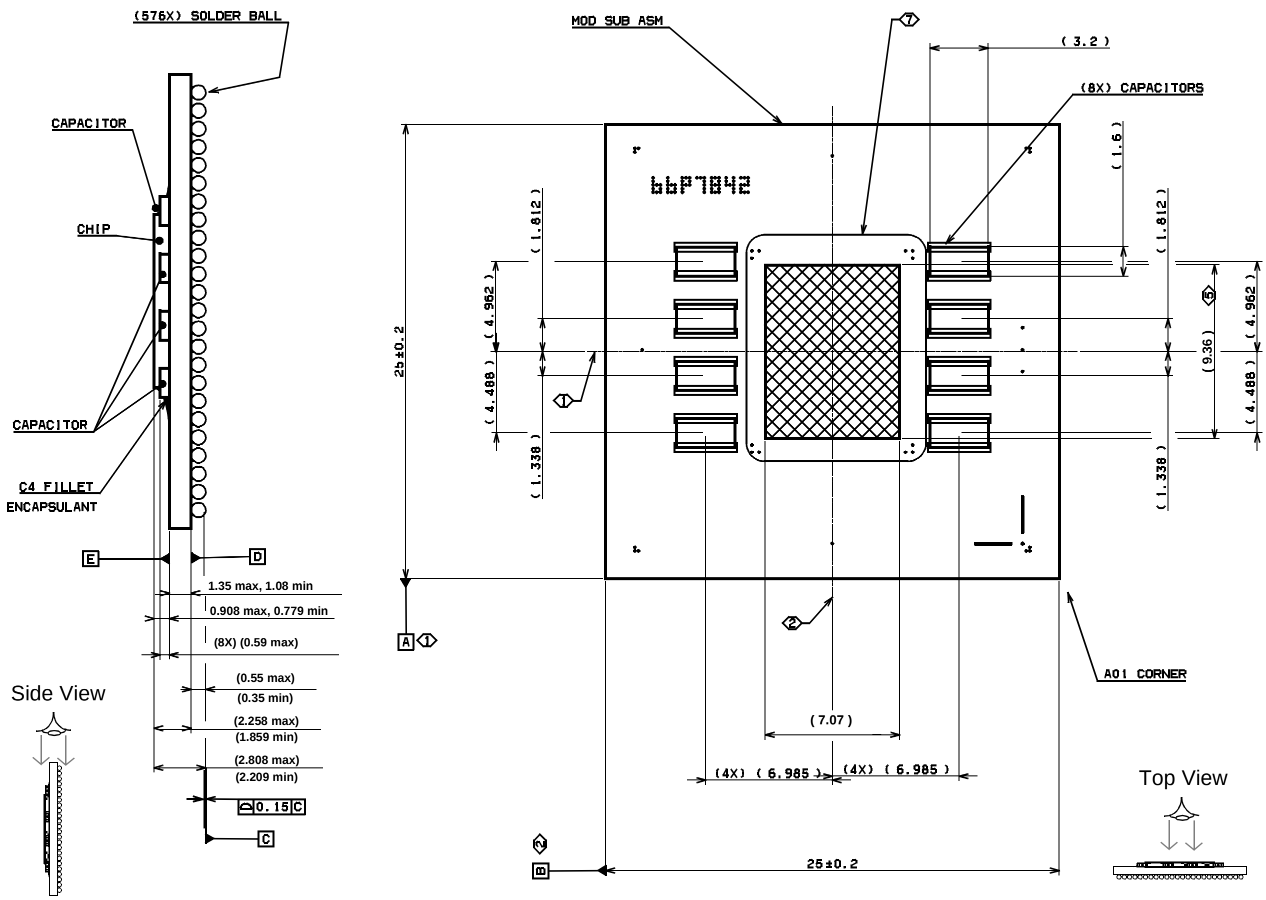
4.2.2.2 Assembly Considerations

The reduced-lead package is compatible with a 260°C lead-free card assembly reflow profile. See the International Electronics Manufacturing Initiative (iNEMI) Consortium, www.inemi.org, for industry-standard assembly and rework information. The coplanarity specification for the reduced-lead CBGA, like other single melt BGA packages, is 0.20 mm (8 mil). The qualification testing included a lead-free, water-soluble solder paste with type 3 mesh size (-325±500). The solder alloy is 95.5% Sn, 4.0% Ag, and 0.5% Cu, with a 90% metal loading. The paste viscosity range is 600 to 800 thousands of centipoises (kcps). The thickness of the stencil is 4 mils and the aperture diameter is 23 mils. The target solder paste volume range is between 1400 to 2000 cubic mils. Achieving the correct paste volume is necessary to eliminate solder shorts and produce high reliability solder joints. The actual solder paste volume from the qualification build ranged from 1750 to 2000 cubic mils.

The JEDEC moisture sensitivity level is MSL 3 for the reduced-lead package. Storage and assembly protocols should be modified accordingly.

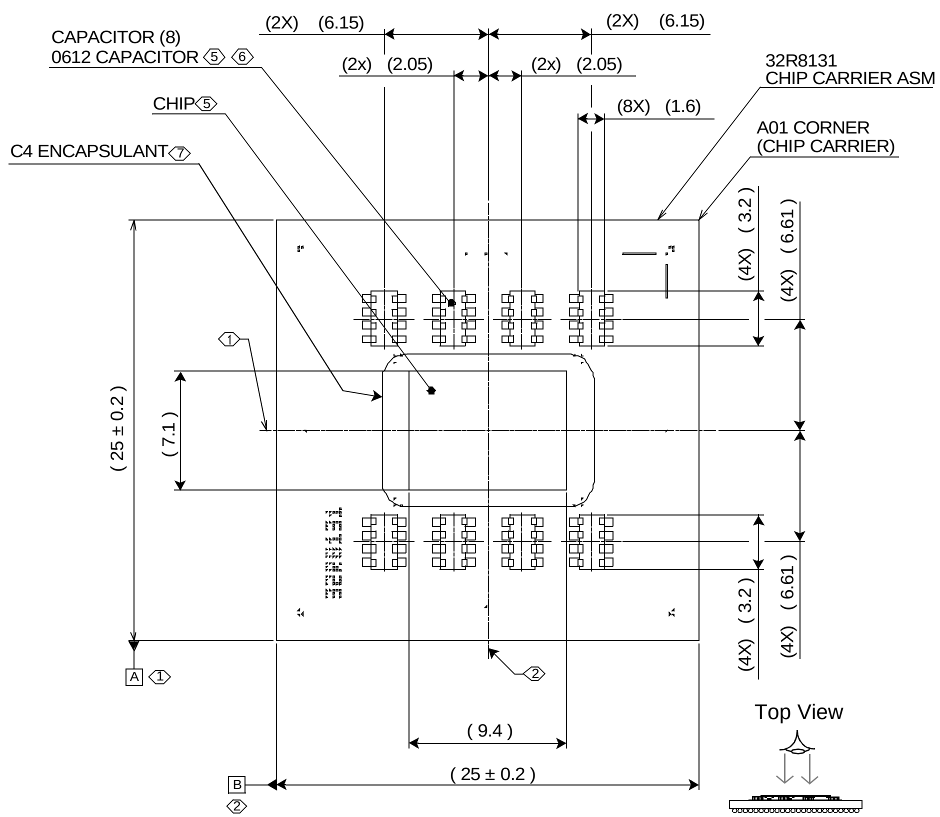
Figure 4-4 on page 50 and *Figure 4-5* on page 51 show the side and top views of the packages including the height from the top of the die to the bottom of the solder balls. *Figure 4-6* on page 52 shows a bottom view of the PowerPC 970FX.

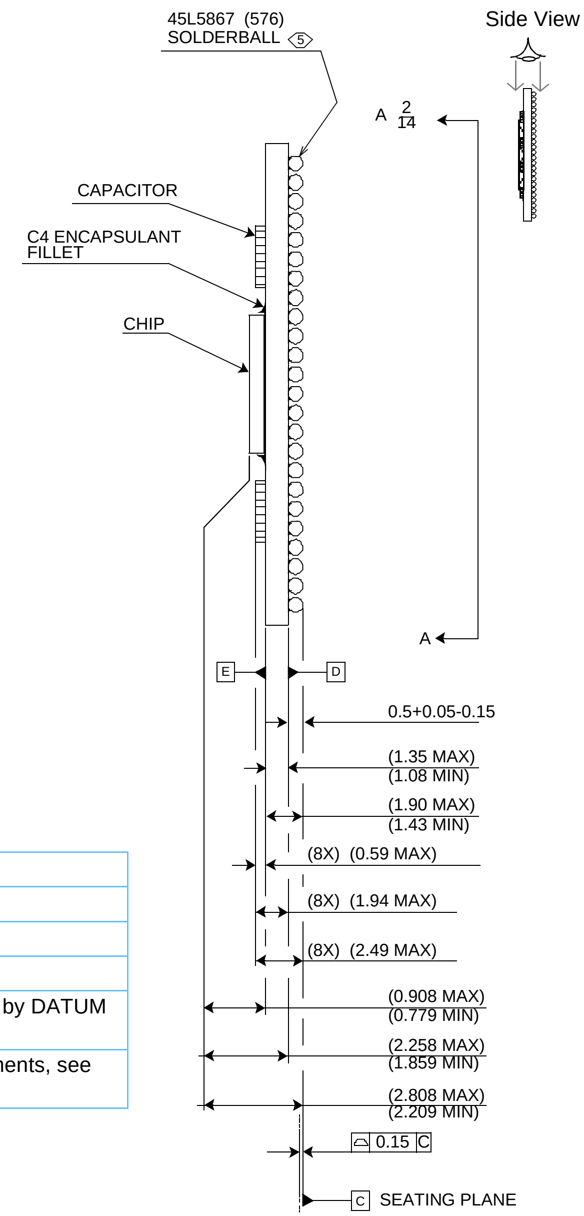
Figure 4-4. PowerPC 970FX Microprocessor Mechanical Package for Reduced-Lead DD3.0x Parts (top and side)



Legend	
1	DATUM A is the center plane of the feature labeled DATUM A.
2	DATUM B is the center plane of the feature labeled DATUM B.
3	Unless otherwise specified, the part is symmetrical about center lines defined by DATUMs A and B.
4	Where not otherwise defined, center lines indicated are to be interpreted as a datum framework, established by DATUM D, A, and B respectively.
7	This line defines the approximate boundary configuration of encapsulant as dispensed.

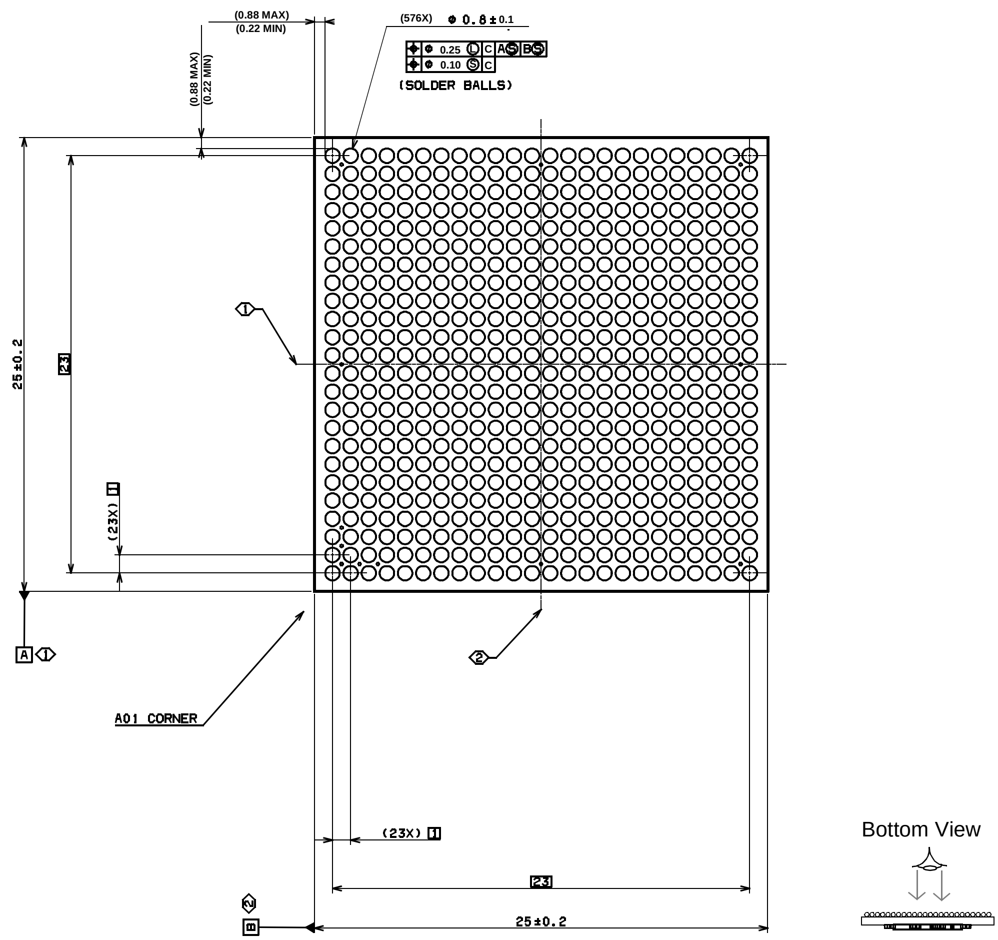
Figure 4-5. PowerPC 970FX Microprocessor Mechanical Package for Reduced-Lead DD3.1 Parts (top and side)





Legend	
1	DATUM A is the center plane of feature labeled DATUM A.
2	DATUM B is the center plane of feature labeled DATUM B.
3	Unless otherwise specified, the part is symmetrical about center lines defined by DATUMs A and B.
4	Where not otherwise defined, center lines indicated are to be interpreted as a datum framework, established by DATUM D, A, and B respectively.
7	This line defines the approximate boundary configuration of encapsulant as dispensed. For underfill requirements, see IBM Engineering Specification 71X8781 Module Encapsulation Specification.

Figure 4-6. PowerPC 970FX Microprocessor Bottom Dimensions for Reduced-Lead CBGA Package



Legend	
1	DATUM A is the center plane of feature labeled DATUM A.
2	DATUM B is the center plane of feature labeled DATUM B.
3	Unless otherwise specified, the part is symmetrical about center lines defined by DATUMs A and B.

Figure 4-7. PowerPC 970FX Ball Placement (Top View)

AD24 GND	AD23 OV_{DD}	AD22 TMS	AD21 TCK	AD20 GND	AD19 OV_{DD}	AD18 $\overline{\text{MCP}}$	AD17 TBEN	AD16 GND	AD15 OV_{DD}	AD14 PSYNC_OUT	AD13 TDO	AD12 ATTENTION	AD11 LSSD_STOP_ENABLE	AD10 GND	AD9 OV_{DD}	AD8 LSSD_STOPC2_ENABLE	AD7 LSSD_STOPC2STAR_ENABLE	AD6 GND	AD5 V_{DD}	AD4 GND	AD3 V_{DD}	AD2 GND	AD1 OV_{DD}	AD
AC24 $\overline{\text{BI\_MODE}}$	AC23 GND	AC22 V_{DD}	AC21 GND	AC20 V_{DD}	AC19 BUS_CFG1	AC18 V_{DD}	AC17 GND	AC16 C1_UND_GLOBAL	AC15 C2_UND_GLOBAL	AC14 V_{DD}	AC13 GND	AC12 V_{DD}	AC11 GND	AC10 PULSE_SEL2	AC9 PULSE_SEL0	AC8 V_{DD}	AC7 GND	AC6 V_{DD}	AC5 GND	AC4 V_{DD}	AC3 GND	AC2 V_{DD}	AC1 GND	AC
AB24 SYNC_ENABLE	AB23 V_{DD}	AB22 GND	AB21 TDI	AB20 GND	AB19 $\overline{\text{INT}}$	AB18 GND	AB17 V_{DD}	AB16 BUS_CFG2	AB15 V_{DD}	AB14 GND	AB13 V_{DD}	AB12 $\overline{\text{QREQ}}$	AB11 PULSE_SEL1	AB10 GND	AB9 V_{DD}	AB8 GND	AB7 PLL_RANGE0	AB6 RAMSTOP_ENABLE	AB5 LSSDMODE	AB4 $\overline{\text{SRESET}}$	AB3 V_{DD}	AB2 GND	AB1 V_{DD}	AB
AA24 OV_{DD}	AA23 GND	AA22 GPULDBG	AA21 GND	AA20 $\overline{\text{I2CCK}}$	AA19 BUS_CFG0	AA18 V_{DD}	AA17 GND	AA16 V_{DD}	AA15 GND	AA14 CKTERM_DIS	AA13 SPARE	AA12 AFN	AA11 GND	AA10 PSYNC	AA9 PLL_RANGE1	AA8 PLL_MULT	AA7 GND	AA6 OV_{DD}	AA5 $\overline{\text{RI}}$	AA4 V_{DD}	AA3 GND	AA2 V_{DD}	AA1 DIODENEG	AA
Y24 GND	Y23 V_{DD}	Y22 V_{DD}	Y21 $\overline{\text{I2CDT}}$	Y20 GND	Y19 V_{DD}	Y18 GND	Y17 OV_{DD}	Y16 GND	Y15 V_{DD}	Y14 GND	Y13 OV_{DD}	Y12 GND	Y11 V_{DD}	Y10 GND	Y9 V_{DD}	Y8 GND	Y7 V_{DD}	Y6 GND	Y5 V_{DD}	Y4 GND	Y3 V_{DD}	Y2 GND	Y1 DIODEPOS	Y
W24 OV_{DD}	W23 $\overline{\text{AVP\_RESET}}$	W22 PLLTEST	W21 GND	W20 $\overline{\text{TRST}}$	W19 GND	W18 V_{DD}	W17 GND	W16 V_{DD}	W15 GND	W14 V_{DD}	W13 GND	W12 V_{DD}	W11 GND	W10 V_{DD}	W9 GND	W8 V_{DD}	W7 GND	W6 V_{DD}	W5 GND	W4	W3 GND	W2 V_{DD}	W1 GND	W
V24 BYPASS	V23 PSRO0	V22 $\overline{\text{THERM\_INT}}$	V21 $\overline{\text{QACK}}$	V20 $\overline{\text{HRESET}}$	V19 V_{DD}	V18 GND	V17 V_{DD}	V16 GND	V15 V_{DD}	V14 GND	V13 V_{DD}	V12 GND	V11 V_{DD}	V10 GND	V9 V_{DD}	V8 GND	V7 V_{DD}	V6 GND	V5 PSRO_Enable	V4 GND	V3 V_{DD}	V2 GND	V1 V_{DD}	V
U24 $\overline{\text{DI2}}$	U23 GND	U22 V_{DD}	U21 GND	U20 V_{DD}	U19 LSSD_SCAN_ENABLE	U18 V_{DD}	U17 GND	U16 V_{DD}	U15 GND	U14 V_{DD}	U13 GND	U12 V_{DD}	U11 GND	U10 V_{DD}	U9 GND	U8 V_{DD}	U7 GND	U6 V_{DD}	U5 GND	U4 V_{DD}	U3 GND	U2 V_{DD}	U1 GND	U
T24 GND	T23 V_{DD}	T22 $\overline{\text{SYSCLK}}$	T21 OV_{DD}	T20 PLL_LOCK	T19 PLLTESTOUT	T18 GND	T17 V_{DD}	T16 GND	T15 OV_{DD}	T14 GND	T13 V_{DD}	T12 GND	T11 OV_{DD}	T10 GND	T9 V_{DD}	T8 GND	T7 V_{DD}	T6 GND	T5 V_{DD}	T4 GND	T3 V_{DD}	T2 KVPRBGND	T1 V_{DD}	T
R24 ANALOG_GND	R23 GND	R22 SYSCLK	R21 GND	R20 $\overline{\text{CHKSTOP}}$	R19 GND	R18 V_{DD}	R17 GND	R16 V_{DD}	R15 GND	R14 V_{DD}	R13 GND	R12 V_{DD}	R11 GND	R10 V_{DD}	R9 GND	R8 V_{DD}	R7 GND	R6 V_{DD}	R5 GND	R4 V_{DD}	R3 GND	R2 KVPRBVDD	R1 Z_SENSE	R
P24 AVDD	P23 V_{DD}	P22 GND	P21 V_{DD}	P20 EI_DISABLE	P19 V_{DD}	P18 GND	P17 OV_{DD}	P16 GND	P15 V_{DD}	P14 GND	P13 V_{DD}	P12 GND	P11 V_{DD}	P10 GND	P9 V_{DD}	P8 GND	P7 V_{DD}	P6 GND	P5 V_{DD}	P4 GND	P3 V_{DD}	P2 Z_OUT	P1 V_{DD}	P
N24 OV_{DD}	N23 GND	N22 I2CGO	N21 TRIGGERIN	N20 V_{DD}	N19 TRIGGEROUT	N18 V_{DD}	N17 GND	N16 V_{DD}	N15 GND	N14 V_{DD}	N13 GND	N12 V_{DD}	N11 GND	N10 V_{DD}	N9 GND	N8 V_{DD}	N7 GND	N6 V_{DD}	N5 GND	N4 V_{DD}	N3 ADOUT0	N2 V_{DD}	N1 SPARE_GND	N
M24 GND	M23 V_{DD}	M22 GND	M21 V_{DD}	M20 GND	M19 PROCID1	M18 PROCID2	M17 V_{DD}	M16 GND	M15 V_{DD}	M14 GND	M13 V_{DD}	M12 GND	M11 V_{DD}	M10 GND	M9 OV_{DD}	M8 GND	M7 V_{DD}	M6 GND	M5 V_{DD}	M4 GND	M3 ADOUT4	M2 GND	M1 OV_{DD}	M
L24 SRIN0	L23 GND	L22 $\overline{\text{SRIN1}}$	L21 SRIN1	L20 V_{DD}	L19 PROCID0	L18 V_{DD}	L17 GND	L16 OV_{DD}	L15 GND	L14 V_{DD}	L13 GND	L12 V_{DD}	L11 GND	L10 OV_{DD}	L9 GND	L8 V_{DD}	L7 GND	L6 V_{DD}	L5 GND	L4 V_{DD}	L3 SROUT0	L2 $\overline{\text{SROUT0}}$	L1 ADOUT3	L
K24 $\overline{\text{SRIN0}}$	K23 V_{DD}	K22 ADIN6	K21 OV_{DD}	K20 GND	K19 V_{DD}	K18 GND	K17 OV_{DD}	K16 GND	K15 V_{DD}	K14 GND	K13 V_{DD}	K12 GND	K11 V_{DD}	K10 GND	K9 V_{DD}	K8 GND	K7 V_{DD}	K6 GND	K5 OV_{DD}	K4 ADOUT5	K3 ADOUT2	K2 ADOUT6	K1 GND	K
J24 ADIN8	J23 GND	J22 ADIN3	J21 ADIN1	J20 V_{DD}	J19 GND	J18 OV_{DD}	J17 GND	J16 V_{DD}	J15 GND	J14 OV_{DD}	J13 GND	J12 V_{DD}	J11 GND	J10 OV_{DD}	J9 GND	J8 OV_{DD}	J7 GND	J6 V_{DD}	J5 GND	J4 V_{DD}	J3 GND	J2 V_{DD}	J1 OV_{DD}	J
H24 OV_{DD}	H23 ADIN7	H22 ADIN2	H21 ADIN0	H20 GND	H19 V_{DD}	H18 GND	H17 V_{DD}	H16 GND	H15 V_{DD}	H14 GND	H13 V_{DD}	H12 GND	H11 V_{DD}	H10 GND	H9 V_{DD}	H8 GND	H7 V_{DD}	H6 GND	H5 V_{DD}	H4 GND	H3 ADOUT7	H2 ADOUT1	H1 ADOUT8	H
G24 ADIN13	G23 GND	G22 V_{DD}	G21 ADIN11	G20 ADIN9	G19 ADIN14	G18 V_{DD}	G17 GND	G16 V_{DD}	G15 GND	G14 V_{DD}	G13 GND	G12 V_{DD}	G11 GND	G10 V_{DD}	G9 GND	G8 V_{DD}	G7 GND	G6 V_{DD}	G5 GND	G4 ADOUT9	G3 ADOUT13	G2 GND	G1 SROUT1	G
F24 GND	F23 ADIN10	F22 GND	F21 ADIN25	F20 GND	F19 OV_{DD}	F18 GND	F17 V_{DD}	F16 GND	F15 V_{DD}	F14 GND	F13 V_{DD}	F12 GND	F11 V_{DD}	F10 GND	F9 V_{DD}	F8 GND	F7 OV_{DD}	F6 GND	F5 V_{DD}	F4 ADOUT11	F3 OV_{DD}	F2 ADOUT10	F1 $\overline{\text{SROUT1}}$	F
E24 CLKIN	E23 GND	E22 V_{DD}	E21 ADIN22	E20 ADIN21	E19 GND	E18 V_{DD}	E17 GND	E16 V_{DD}	E15 GND	E14 V_{DD}	E13 GND	E12 ADOUT16	E11 GND	E10 V_{DD}	E9 GND	E8 V_{DD}	E7 GND	E6 V_{DD}	E5 GND	E4 V_{DD}	E3 $\overline{\text{CLKOUT}}$	E2 ADOUT12	E1 OV_{DD}	E
D24 $\overline{\text{CLKIN}}$	D23 V_{DD}	D22 ADIN12	D21 V_{DD}	D20 ADIN32	D19 V_{DD}	D18 ADIN30	D17 V_{DD}	D16 GND	D15 ADIN18	D14 GND	D13 V_{DD}	D12 GND	D11 ADOUT15	D10 GND	D9 OV_{DD}	D8 ADOUT27	D7 V_{DD}	D6 ADOUT23	D5 V_{DD}	D4 GND	D3 CLKOUT	D2 ADOUT26	D1 GND	D
C24 OV_{DD}	C23 GND	C22 ADIN20	C21 GND	C20 V_{DD}	C19 ADIN34	C18 ADIN35	C17 ADIN29	C16 ADIN42	C15 ADIN17	C14 ADIN28	C13 ADIN4	C12 ADOUT28	C11 ADOUT19	C10 ADOUT41	C9 ADOUT39	C8 ADOUT35	C7 ADOUT33	C6 ADOUT36	C5 ADOUT21	C4 ADOUT32	C3 GND	C2 OV_{DD}	C1 ADOUT20	C
B24 ADIN24	B23 ADIN23	B22 GND	B21 ADIN31	B20 OV_{DD}	B19 ADIN27	B18 GND	B17 ADIN26	B16 OV_{DD}	B15 ADIN15	B14 GND	B13 V_{DD}	B12 GND	B11 OV_{DD}	B10 ADOUT18	B9 GND	B8 ADOUT14	B7 OV_{DD}	B6 ADOUT30	B5 GND	B4 ADOUT31	B3 V_{DD}	B2 ADOUT22	B1 GND	B
A24 OV_{DD}	A23 ADIN37	A22 ADIN33	A21 ADIN36	A20 ADIN38	A19 ADIN43	A18 ADIN39	A17 ADIN41	A16 ADIN19	A15 ADIN40	A14 ADIN16	A13 ADIN5	A12 ADOUT29	A11 ADOUT17	A10 ADOUT40	A9 ADOUT38	A8 ADOUT42	A7 ADOUT34	A6 ADOUT43	A5 ADOUT24	A4 ADOUT37	A3 GND	A2 ADOUT25	A1 OV_{DD}	A
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

Note: This diagram is oriented as if looking down through the PowerPC 970FX with it placed and soldered on the system board - a top view.

Figure 4-8. PowerPC 970FX Ball Placement (Bottom View)

AD	AD1 OV$_{DD}$	AD2 GND	AD3 V$_{DD}$	AD4 GND	AD5 V$_{DD}$	AD6 GND	AD7 LSSD_STOPC2STAR_ENABLE	AD8 LSSD_STOPC2_ENABLE	AD9 OV$_{DD}$	AD10 GND	AD11 LSSD_STOP_ENABLE	AD12 ATTENTION	AD13 TDO	AD14 PSYNC_OUT	AD15 OV$_{DD}$	AD16 GND	AD17 TBEN	AD18 $\overline{\text{MCP}}$	AD19 OV$_{DD}$	AD20 GND	AD21 TCK	AD22 TMS	AD23 OV$_{DD}$	AD24 GND
AC	AC1 GND	AC2 V$_{DD}$	AC3 GND	AC4 V$_{DD}$	AC5 GND	AC6 V$_{DD}$	AC7 GND	AC8 V$_{DD}$	AC9 PULSE_SEL0	AC10 PULSE_SEL2	AC11 GND	AC12 V$_{DD}$	AC13 GND	AC14 V$_{DD}$	AC15 C2_UND_GLOBAL	AC16 C1_UND_GLOBAL	AC17 GND	AC18 V$_{DD}$	AC19 BUS_CFG1	AC20 V$_{DD}$	AC21 GND	AC22 V$_{DD}$	AC23 GND	AC24 $\overline{\text{BI\_MODE}}$
AB	AB1 V$_{DD}$	AB2 GND	AB3 V$_{DD}$	AB4 $\overline{\text{SRESET}}$	AB5 LSSDMODE	AB6 RAMSTOP_ENABLE	AB7 PLL_RANGE0	AB8 GND	AB9 V$_{DD}$	AB10 GND	AB11 PULSE_SEL1	AB12 $\overline{\text{QREQ}}$	AB13 V$_{DD}$	AB14 GND	AB15 V$_{DD}$	AB16 BUS_CFG2	AB17 V$_{DD}$	AB18 GND	AB19 $\overline{\text{INT}}$	AB20 GND	AB21 TDI	AB22 GND	AB23 V$_{DD}$	AB24 SYNC_ENABLE
AA	AA1 DIODENEG	AA2 V$_{DD}$	AA3 GND	AA4 V$_{DD}$	AA5 $\overline{\text{RI}}$	AA6 OV$_{DD}$	AA7 GND	AA8 PLL_MULT	AA9 PLL_RANGE1	AA10 PSYNC	AA11 GND	AA12 AFN	AA13 SPARE	AA14 CKTERM_DIS	AA15 GND	AA16 V$_{DD}$	AA17 GND	AA18 V$_{DD}$	AA19 BUS_CFG0	AA20 $\overline{\text{I2CCK}}$	AA21 GND	AA22 GPULDBG	AA23 GND	AA24 OV$_{DD}$
Y	Y1 DIODEPOS	Y2 GND	Y3 V$_{DD}$	Y4 GND	Y5 V$_{DD}$	Y6 GND	Y7 V$_{DD}$	Y8 GND	Y9 V$_{DD}$	Y10 GND	Y11 V$_{DD}$	Y12 GND	Y13 OV$_{DD}$	Y14 GND	Y15 V$_{DD}$	Y16 GND	Y17 OV$_{DD}$	Y18 GND	Y19 V$_{DD}$	Y20 GND	Y21 $\overline{\text{I2CDT}}$	Y22 V$_{DD}$	Y23 V$_{DD}$	Y24 GND
W	W1 GND	W2 V$_{DD}$	W3 GND	W4 SPARE2	W5 GND	W6 V$_{DD}$	W7 GND	W8 V$_{DD}$	W9 GND	W10 V$_{DD}$	W11 GND	W12 V$_{DD}$	W13 GND	W14 V$_{DD}$	W15 GND	W16 V$_{DD}$	W17 GND	W18 V$_{DD}$	W19 GND	W20 $\overline{\text{TRST}}$	W21 GND	W22 PLLTEST	W23 $\overline{\text{AVP\_RESET}}$	W24 OV$_{DD}$
V	V1 V$_{DD}$	V2 GND	V3 V$_{DD}$	V4 GND	V5 PSRO_Enable	V6 GND	V7 V$_{DD}$	V8 GND	V9 V$_{DD}$	V10 GND	V11 V$_{DD}$	V12 GND	V13 V$_{DD}$	V14 GND	V15 V$_{DD}$	V16 GND	V17 V$_{DD}$	V18 GND	V19 V$_{DD}$	V20 $\overline{\text{HRESET}}$	V21 $\overline{\text{QACK}}$	V22 $\overline{\text{THERM\_INT}}$	V23 PSRO0	V24 BYPASS
U	U1 GND	U2 V$_{DD}$	U3 GND	U4 V$_{DD}$	U5 GND	U6 V$_{DD}$	U7 GND	U8 V$_{DD}$	U9 GND	U10 V$_{DD}$	U11 GND	U12 V$_{DD}$	U13 GND	U14 V$_{DD}$	U15 GND	U16 V$_{DD}$	U17 GND	U18 V$_{DD}$	U19 LSSD_SCAN_ENABLE	U20 V$_{DD}$	U21 GND	U22 V$_{DD}$	U23 GND	U24 $\overline{\text{DI2}}$
T	T1 V$_{DD}$	T2 KVPRBGND	T3 V$_{DD}$	T4 GND	T5 V$_{DD}$	T6 GND	T7 V$_{DD}$	T8 GND	T9 V$_{DD}$	T10 GND	T11 OV$_{DD}$	T12 GND	T13 V$_{DD}$	T14 GND	T15 OV$_{DD}$	T16 GND	T17 V$_{DD}$	T18 GND	T19 PLLTESTOUT	T20 PLL_LOCK	T21 OV$_{DD}$	T22 $\overline{\text{SYSCLK}}$	T23 V$_{DD}$	T24 GND
R	R1 Z_SENSE	R2 KVPRBVDD	R3 GND	R4 V$_{DD}$	R5 GND	R6 V$_{DD}$	R7 GND	R8 V$_{DD}$	R9 GND	R10 V$_{DD}$	R11 GND	R12 V$_{DD}$	R13 GND	R14 V$_{DD}$	R15 GND	R16 V$_{DD}$	R17 GND	R18 V$_{DD}$	R19 GND	R20 $\overline{\text{CHKSTOP}}$	R21 GND	R22 SYSCLK	R23 GND	R24 ANALOG_GND
P	P1 V$_{DD}$	P2 Z_OUT	P3 V$_{DD}$	P4 GND	P5 V$_{DD}$	P6 GND	P7 V$_{DD}$	P8 GND	P9 V$_{DD}$	P10 GND	P11 V$_{DD}$	P12 GND	P13 V$_{DD}$	P14 GND	P15 V$_{DD}$	P16 GND	P17 OV$_{DD}$	P18 GND	P19 V$_{DD}$	P20 EI_DISABLE	P21 V$_{DD}$	P22 GND	P23 V$_{DD}$	P24 AVDD
N	N1 SPARE_GND	N2 V$_{DD}$	N3 ADOUT0	N4 V$_{DD}$	N5 GND	N6 V$_{DD}$	N7 GND	N8 V$_{DD}$	N9 GND	N10 V$_{DD}$	N11 GND	N12 V$_{DD}$	N13 GND	N14 V$_{DD}$	N15 GND	N16 V$_{DD}$	N17 GND	N18 V$_{DD}$	N19 TRIGGEROUT	N20 V$_{DD}$	N21 TRIGGERIN	N22 I2CGO	N23 GND	N24 OV$_{DD}$
M	M1 OV$_{DD}$	M2 GND	M3 ADOUT4	M4 GND	M5 V$_{DD}$	M6 GND	M7 V$_{DD}$	M8 GND	M9 OV$_{DD}$	M10 GND	M11 V$_{DD}$	M12 GND	M13 V$_{DD}$	M14 GND	M15 V$_{DD}$	M16 GND	M17 V$_{DD}$	M18 PROCID2	M19 PROCID1	M20 GND	M21 V$_{DD}$	M22 GND	M23 V$_{DD}$	M24 GND
L	L1 ADOUT3	L2 $\overline{\text{SROUT0}}$	L3 SROUT0	L4 V$_{DD}$	L5 GND	L6 V$_{DD}$	L7 GND	L8 V$_{DD}$	L9 GND	L10 OV$_{DD}$	L11 GND	L12 V$_{DD}$	L13 GND	L14 V$_{DD}$	L15 GND	L16 OV$_{DD}$	L17 GND	L18 V$_{DD}$	L19 PROCID0	L20 V$_{DD}$	L21 SRIN1	L22 $\overline{\text{SRIN1}}$	L23 GND	L24 SRIN0
K	K1 GND	K2 ADOUT6	K3 ADOUT2	K4 ADOUT5	K5 OV$_{DD}$	K6 GND	K7 V$_{DD}$	K8 GND	K9 V$_{DD}$	K10 GND	K11 V$_{DD}$	K12 GND	K13 V$_{DD}$	K14 GND	K15 V$_{DD}$	K16 GND	K17 OV$_{DD}$	K18 GND	K19 V$_{DD}$	K20 GND	K21 OV$_{DD}$	K22 ADIN6	K23 V$_{DD}$	K24 $\overline{\text{SRIN0}}$
J	J1 OV$_{DD}$	J2 V$_{DD}$	J3 GND	J4 V$_{DD}$	J5 GND	J6 V$_{DD}$	J7 GND	J8 OV$_{DD}$	J9 GND	J10 OV$_{DD}$	J11 GND	J12 V$_{DD}$	J13 GND	J14 OV$_{DD}$	J15 GND	J16 V$_{DD}$	J17 GND	J18 OV$_{DD}$	J19 GND	J20 V$_{DD}$	J21 ADIN1	J22 ADIN3	J23 GND	J24 ADIN8
H	H1 ADOUT8	H2 ADOUT1	H3 ADOUT7	H4 GND	H5 V$_{DD}$	H6 GND	H7 V$_{DD}$	H8 GND	H9 V$_{DD}$	H10 GND	H11 V$_{DD}$	H12 GND	H13 V$_{DD}$	H14 GND	H15 V$_{DD}$	H16 GND	H17 V$_{DD}$	H18 GND	H19 V$_{DD}$	H20 GND	H21 ADIN0	H22 ADIN2	H23 ADIN7	H24 OV$_{DD}$
G	G1 SROUT1	G2 GND	G3 ADOUT13	G4 ADOUT9	G5 GND	G6 V$_{DD}$	G7 GND	G8 V$_{DD}$	G9 GND	G10 V$_{DD}$	G11 GND	G12 V$_{DD}$	G13 GND	G14 V$_{DD}$	G15 GND	G16 V$_{DD}$	G17 GND	G18 V$_{DD}$	G19 ADIN14	G20 ADIN9	G21 ADIN11	G22 V$_{DD}$	G23 GND	G24 ADIN13
F	F1 $\overline{\text{SROUT1}}$	F2 ADOUT10	F3 OV$_{DD}$	F4 ADOUT11	F5 V$_{DD}$	F6 GND	F7 OV$_{DD}$	F8 GND	F9 V$_{DD}$	F10 GND	F11 V$_{DD}$	F12 GND	F13 V$_{DD}$	F14 GND	F15 V$_{DD}$	F16 GND	F17 V$_{DD}$	F18 GND	F19 OV$_{DD}$	F20 GND	F21 ADIN25	F22 GND	F23 ADIN10	F24 GND
E	E1 OV$_{DD}$	E2 ADOUT12	E3 $\overline{\text{CLKOUT}}$	E4 V$_{DD}$	E5 GND	E6 V$_{DD}$	E7 GND	E8 V$_{DD}$	E9 GND	E10 V$_{DD}$	E11 GND	E12 ADOUT16	E13 GND	E14 V$_{DD}$	E15 GND	E16 V$_{DD}$	E17 GND	E18 V$_{DD}$	E19 GND	E20 ADIN21	E21 ADIN22	E22 V$_{DD}$	E23 GND	E24 CLKIN
D	D1 GND	D2 ADOUT26	D3 CLKOUT	D4 GND	D5 V$_{DD}$	D6 ADOUT23	D7 V$_{DD}$	D8 ADOUT27	D9 OV$_{DD}$	D10 GND	D11 ADOUT15	D12 GND	D13 V$_{DD}$	D14 GND	D15 ADIN18	D16 GND	D17 V$_{DD}$	D18 ADIN30	D19 V$_{DD}$	D20 ADIN32	D21 V$_{DD}$	D22 ADIN12	D23 V$_{DD}$	D24 $\overline{\text{CLKIN}}$
C	C1 ADOUT20	C2 OV$_{DD}$	C3 GND	C4 ADOUT32	C5 ADOUT21	C6 ADOUT36	C7 ADOUT33	C8 ADOUT35	C9 ADOUT39	C10 ADOUT41	C11 ADOUT19	C12 ADOUT28	C13 ADIN4	C14 ADIN28	C15 ADIN17	C16 ADIN42	C17 ADIN29	C18 ADIN35	C19 ADIN34	C20 V$_{DD}$	C21 GND	C22 ADIN20	C23 GND	C24 OV$_{DD}$
B	B1 GND	B2 ADOUT22	B3 V$_{DD}$	B4 ADOUT31	B5 GND	B6 ADOUT30	B7 OV$_{DD}$	B8 ADOUT14	B9 GND	B10 ADOUT18	B11 OV$_{DD}$	B12 GND	B13 V$_{DD}$	B14 GND	B15 ADIN15	B16 OV$_{DD}$	B17 ADIN26	B18 GND	B19 ADIN27	B20 OV$_{DD}$	B21 ADIN31	B22 GND	B23 ADIN23	B24 ADIN24
A	A1 OV$_{DD}$	A2 ADOUT25	A3 GND	A4 ADOUT37	A5 ADOUT24	A6 ADOUT43	A7 ADOUT34	A8 ADOUT42	A9 ADOUT38	A10 ADOUT40	A11 ADOUT17	A12 ADOUT29	A13 ADIN5	A14 ADIN16	A15 ADIN40	A16 ADIN19	A17 ADIN41	A18 ADIN39	A19 ADIN43	A20 ADIN38	A21 ADIN36	A22 ADIN33	A23 ADIN37	A24 OV$_{DD}$
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**

4.3 PowerPC 970FX Microprocessor Pinout Listings

Table 4-2 provides the pinout listing for the CBGA package.

Table 4-2. Pinout Listing for the CBGA Package (Page 1 of 5)

Signal Name	Pin Number	Active	I/O PI/PO[5]	Notes
ADIN(0:43)	H21, J21, H22, J22, C13, A13, K22, H23, J24, G20, F23, G21, D22, G24, G19, B15, A14, C15, D15, A16, C22, E20, E21, B23, B24, F21, B17, B19, C14, C17, D18, B21, D20, A22, C19, C18, A21, A23, A20, A18, A15, A17, C16, A19	—	PI Input	—
ADOUT(0:43)	N3, H2, K3, L1, M3, K4, K2, H3, H1, G4, F2, F4, E2, G3, B8, D11, E12, A11, B10, C11, C1, C5, B2, D6, A5, A2, D2, D8, C12, A12, B6, B4, C4, C7, A7, C8, C6, A4, A9, C9, A10, C10, A8, A6	—	PI Output	—
AFN	AA12	—	—	2
ANALOG_GND	R24	—	Analog GND	
ATTENTION	AD12	High	Output	—
AVDD	P24	—	Analog V_{DD}	—
$\overline{\text{AVP\_RESET\_B}}$	W23	Low	Input	1
$\overline{\text{BI\_MODE\_B}}$	AC24	Low	Input	1
BUS_CFG(0:2)	AA19, AC19, AB16	—	Input	10
$\overline{\text{BYPASS\_B}}$	V24	Low	Input	—
C1_UND_GLOBAL	AC16	High	Input	—
C2_UND_GLOBAL	AC15	High	Input	—
$\overline{\text{CHKSTOP\_B}}$	R20	Low	Open Drain/Bidirectional	—
CKTERM_DIS	AA14	High	Input	8
CLKIN	E24	—	PI Input	—

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal system operation.
2. These pins are reserved for potential future use.
3. TCK must be tied high or low for normal system operation. If used, TDI, TMS, and $\overline{\text{TRST\_B}}$ must be pulled up to OV_{DD}.
4. These are test signals for factory use only and must be pulled down with a 10 kΩ resistor to GND for normal system operation.
5. I = Input, O = Output, PI = Processor Interface Input, PO = Processor Interface Output. For additional information, see the *PowerPC 970FX RISC Microprocessor Users Manual*.
6. These pins can be used to measure on-chip voltage drop and noise. They should be connected to a backside probe point immediately behind the module. They should not be connected to GND and V_{DD} planes.
7. PSRO_ENABLE, Z_OUT, Z_SENSE, SPARE_GND, and SPARE2 must be tied to GND for correct operation.
8. CKTERM_DIS high disables SYSCLK termination.
9. If GPULDBG = ‘1’ during HRESET transition from low to high: Run power-on reset (POR) in debug mode and stop after each POR instruction.
   If GPULDBG = ‘0’ during HRESET transition from low to high: Run POR once in automatic mode without stopping after each POR instruction.
   Toggling GPULDBG from ‘1’ to ‘0’ later will finish POR debug mode and continue without stopping after each instruction.
10. The PLL_MULT and PLL_RANGE bits can be overwritten by Joint Test Action Group (JTAG) commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note* for more details.

Table 4-2. Pinout Listing for the CBGA Package (Page 2 of 5)

Signal Name	Pin Number	Active	I/O PI/PO[5]	Notes
CLKIN_B	D24	—	PI Input	—
CLKOUT	D3	—	PI Output	—
CLKOUT_B	E3	—	PI Output	—
$\overline{\text{DI2\_B}}$	U24	Low	Input	1
DIODENEG	AA1	—	—	—
DIODEPOS	Y1	—	—	—
EI_DISABLE	P20	High	Input	—
GND	A3, B1, B5, B9, B12, B14, B18, B22, C3, C21, C23, D1, D4, D10, D12, D14, D16, E5, E7, E9, E11, E13, E15, E17, E19, E23, F6, F8, F10, F12, F14, F16, F18, F20, F22, F24, G2, G5, G7, G9, G11, G13, G15, G17, G23, H4, H6, H8, H10, H12, H14, H16, H18, H20, J3, J5, J7, J9, J11, J13, J15, J17, J19, J23, K1, K6, K8, K10, K12, K14, K16, K18, K20, L5, L7, L9, L11, L13, L15, L17, L23, M2, M4, M6, M8, M10, M12, M14, M16, M20, M22, M24, N5, N7, N9, N11, N13, N15, N17, N23, P4, P6, P8, P10, P12, P14, P16, P18, P22, R3, R5, R7, R9, R11, R13, R15, R17, R19, R21, R23, T4, T6, T8, T10, T12, T14, T16, T18, T24, U1, U3, U5, U7, U9, U11, U13, U15, U17, U21, U23, V2, V4, V6, V8, V10, V12, V14, V16, V18, W1, W3, W5, W7, W9, W11, W13, W15, W17, W19, W21, Y2, Y4, Y6, Y8, Y10, Y12, Y14, Y16, Y18, Y20, Y24, AA3, AA7, AA11, AA15, AA17, AA21, AA23, AB2, AB8, AB10, AB14, AB18, AB20, AB22, AC1, AC3, AC5, AC7, AC11, AC13, AC17, AC21, AC23, AD2, AD4, AD6, AD10, AD16, AD20, AD24	—	GND	—
GPULDBG	AA22	High	Input	9
$\overline{\text{HRESET\_B}}$	V20	Low	Input	—
$\overline{\text{I2CCK\_B}}$	AA20	—	OD BiDi	—
$\overline{\text{I2CDT\_B}}$	Y21	—	OD BiDi	—
I2CGO	N22	—	OD	—

Notes:

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3. TCK must be tied high or low for normal system operation. If used, TDI, TMS, and $\overline{\text{TRST\_B}}$ must be pulled up to OV_{DD}.
4. These are test signals for factory use only and must be pulled down with a 10 kΩ resistor to GND for normal system operation.
5. I = Input, O = Output, PI = Processor Interface Input, PO = Processor Interface Output. For additional information, see the *PowerPC 970FX RISC Microprocessor Users Manual*.
6. These pins can be used to measure on-chip voltage drop and noise. They should be connected to a backside probe point immediately behind the module. They should not be connected to GND and V_{DD} planes.
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8. CKTERM_DIS high disables SYSCLK termination.
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   Toggling GPULDBG from ‘1’ to ‘0’ later will finish POR debug mode and continue without stopping after each instruction.
10. The PLL_MULT and PLL_RANGE bits can be overwritten by Joint Test Action Group (JTAG) commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note* for more details.

Table 4-2. Pinout Listing for the CBGA Package (Page 3 of 5)

Signal Name	Pin Number	Active	I/O PI/PO[5]	Notes
$\overline{\text{INT\_B}}$	AB19	Low	Input	
KVPRBGND	T2	—	GND Test Points	6
KVPRBVDD	R2	—	V_{DD} Test Points	6
LSSDMODE	AB5	High	Input	4
LSSD_SCAN_ENABLE	U19	High	Input	4
LSSD_STOP_ENABLE	AD11	High	Input	4
LSSD_STOPC2_ENABLE	AD8	High	Input	4
LSSD_STOPC2STAR_ENABLE	AD7	High	Input	4
$\overline{\text{MCP\_B}}$	AD18	Low	Input	—
PLL_LOCK	T20	High	Output	—
PLL_MULT	AA8	—	Input	10
PLL_RANGE(1:0)	AA9, AB7	—	Input	10
PLLTEST	W22	High	Input	—
PLLTESTOUT	T19	—	Output	—
PROCID(0:2)	L19, M19, M18	—	Input	—
PSRO_ENABLE	V5	—	—	7
PSRO0	V23	—	Output	—
PSYNC	AA10	—	Input	—
PSYNC_OUT	AD14	—	Output	—
PULSE_SEL(0:2)	AC9, AB11, AC10	—	Input	—
$\overline{\text{QACK\_B}}$	V21	Low	Input	—
$\overline{\text{QREQ\_B}}$	AB12	Low	Output	—

Notes:

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4. These are test signals for factory use only and must be pulled down with a 10 kΩ resistor to GND for normal system operation.
5. I = Input, O = Output, PI = Processor Interface Input, PO = Processor Interface Output. For additional information, see the *PowerPC 970FX RISC Microprocessor Users Manual*.
6. These pins can be used to measure on-chip voltage drop and noise. They should be connected to a backside probe point immediately behind the module. They should not be connected to GND and V_{DD} planes.
7. PSRO_ENABLE, Z_OUT, Z_SENSE, SPARE_GND, and SPARE2 must be tied to GND for correct operation.
8. CKTERM_DIS high disables SYSCLK termination.
9. If GPULDBG = ‘1’ during HRESET transition from low to high: Run power-on reset (POR) in debug mode and stop after each POR instruction.
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10. The PLL_MULT and PLL_RANGE bits can be overwritten by Joint Test Action Group (JTAG) commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note* for more details.

Table 4-2. Pinout Listing for the CBGA Package (Page 4 of 5)

Signal Name	Pin Number	Active	I/O PI/PO[5]	Notes
RAMSTOP_ENABLE	AB6	High	Input	4
$\overline{\text{RI\_B}}$	AA5	Low	Input	1
SPARE	AA13	—	Input	1, 2
SPARE2	W4	—	—	7
SPARE_GND	N1	—	—	7
$\overline{\text{SRESET\_B}}$	AB4	Low	Input	—
SRIN(0:1)	L24, L21	—	PI Input	—
SRIN_B(0:1)	K24, L22	—	PI Input	—
SROUT(0:1)	L3, G1	—	PI Output	—
SROUT_B(0:1)	L2, F1	—	PI Output	—
SYNC_ENABLE	AB24	High	Input	4
SYSCLK	R22	—	Input	—
SYSCLK_B	T22	—	Input	—
TBEN	AD17	High	Input	—
TCK	AD21	—	Input	3
TDI	AB21	—	Input	3
TDO	AD13	—	Output	—
$\overline{\text{THERM\_INT\_B}}$	V22	Low	Input	—
TMS	AD22	—	Input	3
TRIGGERIN	N21	High	Input	—
TRIGGEROUT	N19	High	Output	—
$\overline{\text{TRST\_B}}$	W20	Low	Input	3

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Table 4-2. Pinout Listing for the CBGA Package (Page 5 of 5)

Signal Name	Pin Number	Active	I/O PI/PO[5]	Notes
V_{DD}	B3, B13, C20, D5, D7, D13, D17, D19, D21, D23, E4, E6, E8, E10, E14, E16, E18, E22, F5, F9, F11, F13, F15, F17, G6, G8, G10, G12, G14, G16, G18, G22, H5, H7, H9, H11, H13, H15, H17, H19, J2, J4, J6, J12, J16, J20, K7, K9, K11, K13, K15, K19, K23, L4, L6, L8, L12, L14, L18, L20, M5, M7, M11, M13, M15, M17, M21, M23, N2, N4, N6, N8, N10, N12, N14, N16, N18, N20, P1, P3, P5, P7, P9, P11, P13, P15, P19, P21, P23, R4, R6, R8, R10, R12, R14, R16, R18, T1, T3, T5, T7, T9, T13, T17, T23, U2, U4, U6, U8, U10, U12, U14, U16, U18, U20, U22, V1, V3, V7, V9, V11, V13, V15, V17, V19, W2, W6, W8, W10, W12, W14, W16, W18, Y3, Y5, Y7, Y9, Y11, Y15, Y19, Y22, Y23, AA2, AA4, AA16, AA18, AB1, AB3, AB9, AB13, AB15, AB17, AB23, AC2, AC4, AC6, AC8, AC12, AC14, AC18, AC20, AC22, AD3, AD5	—	V_{DD}	—
OV_{DD}	A1,A24,B7, B11, B16, B20, C2, C24, D9, E1, F3, F7, F19, H24, J1, J8, J10, J14, J18, K5, K17, K21, L10, L16, M1, M9, N24, P17, T11, T15, T21, W24, Y13, Y17, AA6, AA24, AD1, AD9, AD15, AD19, AD23	—	OV_{DD}	—
Z_OUT	P2	—	—	7
Z_SENSE	R1	—	—	7

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Table 4-3. Voltage and Ground Assignments (Page 1 of 2)

Type	Assignments
V_{DD}	B3, B13 C20 D5, D7, D13, D17, D19, D21, D23 E4, E6, E8, E10, E14, E16, E18, E22 F5, F9, F11, F13, F15, F17 G6, G8, G10, G12, G14, G16, G18, G22 H5, H7, H9, H11, H13, H15, H17, H19 J2, J4, J6, J12, J16, J20 K7, K9, K11, K13, K15, K19, K23 L4, L6, L8, L12, L14, L18, L20 M5, M7, M11, M13, M15, M17, M21, M23 N2, N4, N6, N8, N10, N12, N14, N16, N18, N20 P1, P3, P5, P7, P9, P11, P13, P15, P19, P21, P23 R4, R6, R8, R10, R12, R14, R16, R18 T1, T3, T5, T7, T9, T13, T17, T23 U2, U4, U6, U8, U10, U12, U14, U16, U18, U20, U22 V1, V3, V7, V9, V11, V13, V15, V17, V19 W2, W6, W8, W10, W12, W14, W16, W18 Y3, Y5, Y7, Y9, Y11, Y15, Y19, Y22, Y23 AA2, AA4, AA16, AA18 AB1, AB3, AB9, AB13, AB15, AB17, AB23 AC2, AC4, AC6, AC8, AC12, AC14, AC18, AC20, AC22 AD3, AD5
OV_{DD}	A1, A24 B7, B11, B16, B20 C2, C24 D9, E1 F3, F7, F19 H24, J1, J8, J10, J14, J18, K5, K17, K21, L10, L16 M1, M9, N24 P17 T11, T15, T21 W24 Y13, Y17 AA6, AA24 AD1, AD9, AD15, AD19, AD23

Table 4-3. Voltage and Ground Assignments (Page 2 of 2)

Type	Assignments
GND	A3 B1, B5, B9, B12, B14, B18, B22 C3, C21, C23 D1, D4, D10, D12, D14, D16 E5, E7, E9, E11, E13, E15, E17, E19, E23 F6, F8, F10, F12, F14, F16, F18, F20, F22, F24 G2, G5, G7, G9, G11, G13, G15, G17, G23 H4, H6, H8, H10, H12, H14, H16, H18, H20 J3, J5, J7, J9, J11, J13, J15, J17, J19, J23 K1, K6, K8, K10, K12, K14, K16, K18, K20 L5, L7, L9, L11, L13, L15, L17, L23 M2, M4, M6, M8, M10, M12, M14, M16, M20, M22, M24 N5, N7, N9, N11, N13, N15, N17, N23 P4, P6, P8, P10, P12, P14, P16, P18, P22 R3, R5, R7, R9, R11, R13, R15, R17, R19, R21, R23 T4, T6, T8, T10, T12, T14, T16, T18, T24 U1, U3, U5, U7, U9, U11, U13, U15, U17, U21, U23 V2, V4, V6, V8, V10, V12, V14, V16, V18 W1, W3, W5, W7, W9, W11, W13, W15, W17, W19, W21 Y2, Y4, Y6, Y8, Y10, Y12, Y14, Y16, Y18, Y20, Y24 AA3, AA7, AA11, AA15, AA17, AA21, AA23 AB2, AB8, AB10, AB14, AB18, AB20, AB22 AC1, AC3, AC5, AC7, AC11, AC13, AC17, AC21, AC23 AD2, AD4, AD6, AD10, AD16, AD20, AD24

5. System Design Information

This section provides electrical and thermal design recommendations for the successful application of the PowerPC 970FX.

5.1 External Resistors

The PowerPC 970FX contains no internal pull-up resistors for any Joint Test Action Group (JTAG), I^2C, mode select, or asynchronous inputs. System designs must include these external resistors where required. See *Table 5-6* on page 69*, Table 5-7* on page 70*,* and *Section 3.10.3 I^2C and JTAG Considerations* on page 43 for information about implementing external pullups and pulldowns.

5.2 Phase-Locked Loop Configuration

This section helps the user configure the phase-locked loop (PLL) and determine SYSCLK input frequency for IBM PowerPC 970FX systems.

5.2.1 Determining PLLMULT and BUS_CFG Settings

The first step is to determine the bus frequency. This parameter is a critical component of overall system performance. The bus should run as fast as your memory controller and bridge chip can support. When you have determined your maximum bus frequency, select a bus multiplier ratio that will deliver the optimal processor core frequency.

Note: The PLL_MULT and PLL_RANGE bits can be overwritten by JTAG commands, and the BUS_CFG bits can be changed by SCOM commands, during the power-on reset (POR) sequence. See the *PowerPC 970FX Power On Reset Application Note* for more details.

Table 5-1 shows the available bus ratios. In most applications, this would be the highest frequency possible for a given PowerPC 970FX part number, but other considerations (for example, available power) might take precedence.

Table 5-1. PowerPC 970FX RISC Microprocessor Bus Configuration (Page 1 of 2)

BUS_CFG(0:2)	Ratio	Notes
000	2:1	
001	3:1	
010	4:1	2
011	6:1	2
100	8:1	1

Note: BUS_CFG bits can be changed by SCOM commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note.*

Notes:

1. Bus ratios of 8:1 and 16:1 are not supported for processor interface (PI) input functionality or for power tuning.
2. Limited power-tuning frequency scaling.
3. No power-tuning frequency scaling.

Table 5-1. PowerPC 970FX RISC Microprocessor Bus Configuration (Page 2 of 2)

BUS_CFG(0:2)	Ratio	Notes
101	12:1	3
110	16:1	1
111	Not valid	

Note: BUS_CFG bits can be changed by SCOM commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note.*

Notes:

1. Bus ratios of 8:1 and 16:1 are not supported for processor interface (PI) input functionality or for power tuning.
2. Limited power-tuning frequency scaling.
3. No power-tuning frequency scaling.

The bus frequency multiplier ratio typically indicates the required PLL multiplier setting. Ratios based on multiples of 3 (3:1, 6:1, 12:1) should always use PLLMULT = ‘0’ (low) for a PLL multiplier of 12. The required core frequency should be divided by 12 to determine the required input SYSCLK frequency. Ratios based on multiples of 2 (2:1, 4:1, 8:1, 16:1) should always use PLLMULT = ‘1’ (high) to multiply SYSCLK by 8.

Note: Using bus frequency ratios of 3:1, 6:1 or 12:1 with PLLMULT = 1 or ratios of 8:1 or 16:1 with PLLMULT = 0 is not recommended. Internal clock synchronization delays might reduce performance.

After the correct BUS_CFG(0:2) and PLLMULT pin settings are determined, the required SYSCLK input frequency can be determined. The selected SYSCLK input frequency should be within the minimum and maximum frequencies specified in *Table 3-8 Clock ac Timing Specifications* on page 26.

5.2.2 PLL_RANGE Configuration

Table 5-2 shows the PLL voltage controlled oscillator (VCO) configuration for the PowerPC 970FX, using the pins PLL_RANGE1 and PLL_RANGE0.

Table 5-2. PowerPC 970FX RISC Microprocessor PLL Configuration

PLL_RANGE(1:0) Settings			
Range Name	PLL_RANGE1	PLL_RANGE0	Frequency Range
Low	0	0	Frequency ≤ 1.2 GHz
Medium	0	1	1.2 GHz < Frequency < 1.8 GHz
High	1	0	1.8 GHz ≤ Frequency
Reserved	1	1	Reserved

Notes:

1. The PLL_MULT and PLL_RANGE(1:0) bits can be overwritten by JTAG commands, and the BUS_CFG bits can be changed by SCOM commands, during the POR sequence. See the 970FX *PowerPC 970FX Power On Reset Application Note* for more details.
2. PLL frequency range settings are not an indicator of available PowerPC 970FX processor speeds.

5.2.3 Typical PLL and SYSCLK Configurations

Table 5-3 provides a few examples of typical system configurations.

Table 5-3. System Configuration - Typical Examples of Pin Settings

System Configuration	BUS_CFG(0:2) Pins (core:processor interface[PI] ratio)	PLL_RANGE(1:0) Pins	PLL_MULT Pin	SYSCLK, $\overline{\text{SYSCLK}}$ Frequency
2.0 GHz core, 1000 MHz PI	000 (2:1)	10	1	250 MHz
2.0 GHz core, 667 MHz PI	001 (3:1)	10	0	167 MHz
1.8 GHz Core, 900 MHz PI	000 (2:1)	01	1	225 MHz
1.8 GHz core, 600 MHz PI	001 (3:1)	01	0	150 MHz
1.6 GHz core, 800 MHz PI	000 (2:1)	01	1	200 MHz
1.6 GHz core, 533 MHz PI	001 (3:1)	01	0	133 MHz
1.4 GHz core, 700 MHz PI	000 (2:1)	01	1	175 MHz
1.4 GHz core, 467 MHz PI	001 (3:1)	01	0	116.7 MHz
1.2 GHz core, 600 MHz PI	000 (2:1)	00	1	150 MHz
1.0 GHz core, 500 MHz PI	000 (2:1)	00	1	125 MHz

5.3 PLL Power Supply Filtering

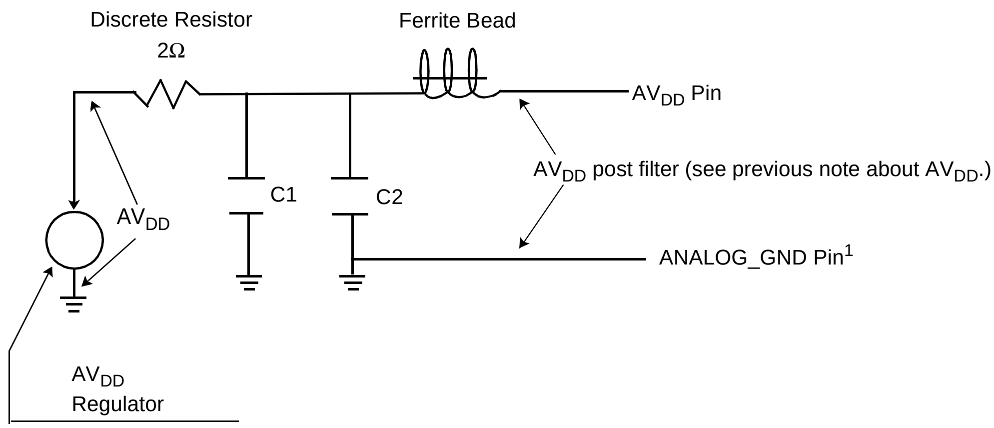
The PowerPC 970FX microprocessor has a separate AV_{DD} pin that provides power to the clock generation PLL.

To ensure stability of the internal clock, filter the power supplied to the AV_{DD} PLL using a circuit similar to *Figure 5-1*. To ensure that the capacitor filters out as much noise as possible, the capacitor should be placed as close as possible to the AV_{DD} and ANALOG_GND pins. The capacitor used should have minimal inductance. The ferrite bead shown in *Figure 5-1* should supply an impedance of less than 70 Ω in the 100 - 500 MHz region.

Note: AV_{DD} measured at the pins of the part should never be more than 50 mV lower than the AV_{DD} voltage range specified in *Table 3-2 Recommended Operating Conditions* on page 21.

Figure 5-1. PLL Power Supply Filter Circuit

AV_{DD} Power Supply Filter Circuit



Item	Description/Value
Resistor	2 Ω
C1	0.1 µF X7R
C2	10.0 µF Y5V
Ferrite Bead	Murata BLM21P300SN1 or similar

Notes:

1. Connected to analog ground without a filter.

5.4 Decoupling Recommendations

Capacitor decoupling is required for the PowerPC 970FX. Decoupling capacitors act to reduce high-frequency chip switching noise and to provide localized bulk charge storage to reduce major power surge effects. Recommendations for high-frequency noise decoupling are provided. Bulk decoupling requires a more complete understanding of the system and system power architecture, and is beyond the scope of this document.

High-frequency decoupling capacitors should be located as close as possible to the processor with low lead inductance to the ground and voltage planes. The recommended placement of the decoupling capacitors is shown in *Figure 5-2* on page 68. The decoupling layout is divided into three groups:

- Group 1 is located in the center of the package and under the PowerPC 970FX die.
- Group 2 includes Group 1 and is located in the center of the package and under the PowerPC 970FX die.
- Group 3, located adjacent to Group 2 (which includes Group 1), lies under the module footprint. Printed circuit board vias for the decoupling capacitors should ideally be through-type vias with via-in-pad for low impedance.

The recommended decoupling capacitor specifications are provided in *Table 5-4*.

Table 5-4. Recommended Decoupling Capacitor Specifications

Specification	Value
Size	0402 (1.00 × 0.50 mm)
Capacitance	100 nF
Dielectric type	Y5V or X7R
Voltage rating	10 V

The minimum recommended number of decoupling capacitors for Group 1 and Group 2 is provided in*Table 5-5*.

Table 5-5. Recommended Minimum Number of Decoupling Capacitors (See *Figure 5-2* on page 68)

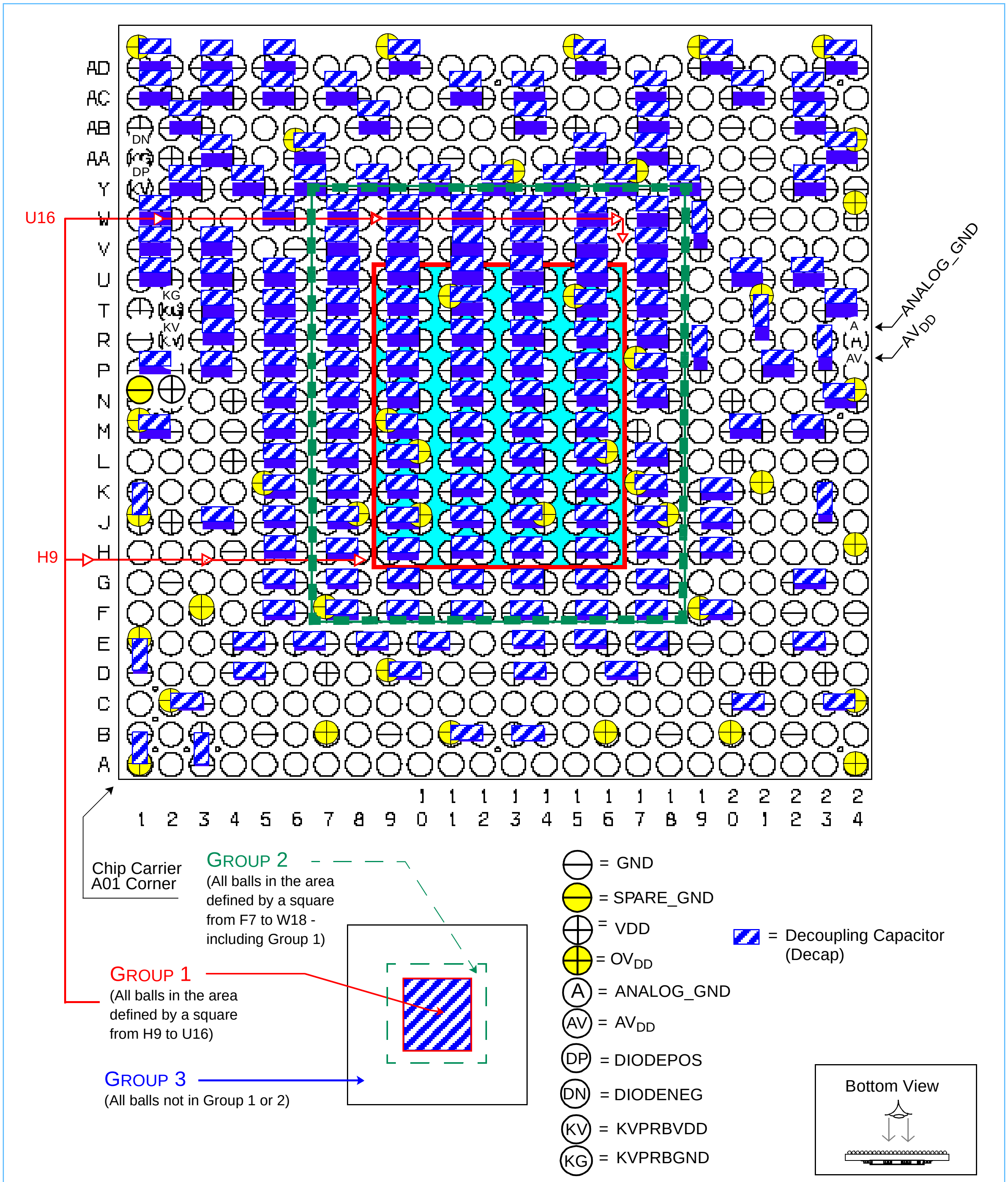
Group 1 Includes all balls in the area defined by a red rectangle from H9 to U16.	Group 2 Includes all balls in the area defined by a dotted-green rectangle from F7 to W18. Also includes all balls in Group 1.	Group 3 Includes all balls on the chip not in Groups 1 and 2.
Minimum of 40: 33 V_{DD} - GND 7 OV_{DD} - GND	Minimum of 80 capacitors (including all 12 OV_{DD} capacitors)	Minimum of 35 V_{DD} - GND Minimum of 4 OV_{DD} - GND
Note: Add additional decoupling capacitors to improve noise performance.		

5.4.1 Using the KVPRBVDD and KVPRBGND Pins

The PowerPC 970FX features one pair of V_{DD} and GND pins to assist in analyzing on-chip noise and voltage drop. These pins should not be connected into the normal V_{DD} and GND planes, but should be brought out to test pads by traces that are as short as possible. An oscilloscope can be used on these test pads to measure on-chip V_{DD} noise and thus to verify the decoupling and voltage regulation in a design. If these pins are not needed, they should be left unconnected.

5.5 Decoupling Layout Guide

Figure 5-2. Decoupling Capacitor Locations



5.6 Pullup and Pulldown Recommendations

For reliable operation, it is highly recommended that the unused inputs be connected to an appropriate signal level. For example:

- Unused active-low inputs should be tied to V_{DD}.
- Multiple unused active-high inputs can be ganged together for convenience.
- Unused active-high inputs should be connected to GND.
- Multiple unused active-low inputs can be ganged together for convenience.
- All no-connect signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} and GND pins of the PowerPC 970FX.

Table 5-6 provides details about the pin settings and information of the PowerPC 970FX debug and bringup signals. *Table 5-7* on page 70 provides details about the appropriate connections for the PowerPC 970FX manufacturing test-only signals.

Table 5-6. PowerPC 970FX Debug and Bringup Pin Settings and Information

Pin Name	Pin Location	In/Out/BiDi/JTAG[1]	Pull-Up or Pull-Down Resistor Setting[2] (For Normal Operation)		Comments
$\overline{\text{AVP\_RESET}}$	W23	In	Up		
C1_UND_GLOBAL	AC16	In	Down		
C2_UND_GLOBAL	AC15	In	Down		
GPULDBG	AA22	In	Up		
I2CGO	N22	Out	Up		Arbitrates between I^2C and JTAG.
TBEN	AD17	In	Down		
TCK	AD21	In-JTAG	Down		JTAG – test clock
TDI	AB21	In-JTAG	Down		JTAG – test data in
TDO	AD13	Out-JTAG	Down		JTAG – test data out
TMS	AD22	In-JTAG	Down		JTAG – test mode select
TRIGGERIN	N21	In	Down		
TRIGGEROUT	N19	Out	—		.
$\overline{\text{TRST}}$	W20	In-JTAG	Up		Not needed – $\overline{\text{HRESET}}$ performs the Common On-Chip Processor (COP) reset function. Pulled up to OV_{DD} by a 10 kΩ resistor.

Notes:

1. BiDi = Bidirectional.
2. Pullups should use a 10 kΩ resistor to OV_{DD}. Pulldowns should use a 10 kΩ resistor to GND.
3. For I^2C or JTAG operation, see *Section 3.10.3* on page 43.

Table 5-7. PowerPC 970FX Pins for Manufacturing Test Only

Pin Name	Pin Location	In/Out	Pullup/Pulldown	Notes
AFN	AA12	Out	—	—
$\overline{\text{BI\_MODE}}$	AC24	In	Up	1
$\overline{\text{DI2}}$	U24	In	Up	1
LSSDMODE	AB5	In	Down	2
LSSD_SCAN_ENABLE	U19	In	Down	2
LSSD_STOPC2_ENABLE	AD8	In	Down	2
LSSD_STOPC2STAR_ENABLE	AD7	In	Down	2
LSSD_STOP_ENABLE	AD11	In	Down	2
PLLTEST		In	Down	2
PSRO_Enable	V5	Out	Down	3
PSRO0	V23	Out	—	—
PULSE_SEL(0:2)	AC9, AB11, AC10	In	Down	2
RAMSTOP_ENABLE	AB6	In	Down	2
$\overline{\text{RI}}$	AA5	In	Up	1
SPARE	AA13	In/Out	—	—
SPARE2	W4	In/Out	Down	3
SPARE_GND	N1	In	Down	3
SYNC_ENABLE	AB24	In	Down	2
Z_OUT	P2	In	Down	3
Z_SENSE	R1	In	Down	3

Note:

1. Pullups should use a 10 kΩ resistor to OV_{DD}.
2. Pulldowns should use a 10 kΩ resistor to GND.
3. Must be tied to GND for correct operation.

5.7 Input-Output Use

This section provides information about the PowerPC 970FX input and output signals and their use.

5.7.1 Chip Signal I/O and Test Pins

Table 5-8 shows the system signal names, debug, and test pins. There are 172 total chip pads. These include three power/capacitance pins.

Table 5-8. Input/Output Signal Descriptions (Page 1 of 4)

Pin Name	Width	In/Out	System/Debug Function	Notes
ADIN(0:43)	44	In	System: Processor interface (PI) address or data and control information.	—
ADOUT(0:43)	44	Out	System: PI address or data and control information out.	—
AFN	1	Out	Pin AFN is a spare output pin.	5
ANALOG_GND	1		Analog ground.	—
ATTENTION	1	Out	Debug: signal from PowerPC 970FX.	—
AV_{DD}	1	In	Analog power supply.	—
$\overline{\text{AVP\_RESET}}$	1	In	For manufacturing test use only.	1
$\overline{\text{BI\_MODE}}$	1	In	Dedicated manufacturing signal.	1
BUS_CFG(0:2)	3	In	Bus configuration select. These signals select the bus frequency division ratio from the processor clock to the bus speed. ‘000’ 2:1 ‘001’ 3:1 ‘010’ 4:1 ‘011’ 6:1 ‘100’ 8:1 ‘101’ 12:1 ‘110’ 16:1 ‘111’ Not valid	3, 8
$\overline{\text{BYPASS}}$	1	In	This signal is used to bypass the PLL.	1
C1_UND_GLOBAL	1	In	Debug: adjusts the C1 clock to internal latches and is not used for normal operation.	10

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal processor operation.
2. For I^2C or JTAG operation, the TCK and TDI signals must be pulled down to ground with a 10 kΩ resistor. See *Section 3.10.3* on page 43.
3. Bus ratios 8:1 and 16:1 are not supported for PI Input functionality.
4. These are test signals for factory use only and must be pulled down to GND for normal processor operation.
5. This signal should not be connected.
6. These pins can be used to measure on-chip voltage drop and noise. They should be connected to a backside probe point immediately behind the module. They should not be connected to GND and V_{DD} planes.
7. BiDi = bidirectional. OD = open drain.
8. Using the 4:1 or 12:1 ratio with multiplier of 12 limits the use of power tuning to (frequency)/2.
9. The PLL_MULT and PLL_RANGE(1:0) bits can be overwritten by JTAG commands and the BUS_CFG bits can be changed by SCOM commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note* for more details
10. Must be pulled down with a 10 kΩ resistor to GND.
11. The $\overline{\text{TRST}}$ signal must be pulled up to OV_{DD} with a 10 kΩ resistor.

Table 5-8. Input/Output Signal Descriptions (Page 2 of 4)

Pin Name	Width	In/Out	System/Debug Function	Notes
C2_UND_GLOBAL	1	In	Debug: adjusts the C2 clock to internal latches and is not used for normal operation.	10
$\overline{\text{CHKSTOP}}$	1	OD /BiDi	System: checkstop input and output.	7
CKTERM_DIS	1	In	Disable internal termination in clock receiver.	—
CLKIN $\overline{\text{CLKIN}}$	2	In	System: PI clock in; differential clock to the processor.	—
CLKOUT $\overline{\text{CLKOUT}}$	2	Out	System: PI differential clock to the bus.	—
$\overline{\text{DI2}}$	1	In	Dedicated manufacturing signal.	1
EI_DISABLE	1	In	Debug: Disables the use of the initial alignment procedure (IAP) to adjust clock skew on the processor interface.	—
GPULDBG	1	In	Debug: POR debug mode select.	—
$\overline{\text{HRESET}}$	1	In	System: POR.	—
$\overline{\text{I2CCK}}$	1	OD /BiDi	System: I^2C signal clock.	7
$\overline{\text{I2CDT}}$	1	OD /BiDi	System: I^2C interface data.	7
I2CGO	1	OD	Debug: handshake signal to arbitrate JTAG or I^2C access.	7
$\overline{\text{INT}}$	1	In	System: external interrupt when low.	—
LSSD_SCAN_ENABLE	1	In	For manufacturing test use only.	4
KVPRBVDD	1	In	V_{DD} test point.	6
KVPRBGND	1	In	GND test point.	6
LSSD_STOP_ENABLE	1	In	For manufacturing test use only.	4
LSSD_STOPC2_ENABLE	1	In	For manufacturing test use only.	4
LSSD_STOPC2STAR_ENABLE	1	In	For manufacturing test use only.	4
LSSDMODE	1	In	For manufacturing test use only.	4
$\overline{\text{MCP}}$)	1	In	System: machine check interrupt.	—
PLL_LOCK	1	Out	Indicates that the PLL has locked.	—

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal processor operation.
2. For I^2C or JTAG operation, the TCK and TDI signals must be pulled down to ground with a 10 kΩ resistor. See *Section 3.10.3* on page 43.
3. Bus ratios 8:1 and 16:1 are not supported for PI Input functionality.
4. These are test signals for factory use only and must be pulled down to GND for normal processor operation.
5. This signal should not be connected.
6. These pins can be used to measure on-chip voltage drop and noise. They should be connected to a backside probe point immediately behind the module. They should not be connected to GND and V_{DD} planes.
7. BiDi = bidirectional. OD = open drain.
8. Using the 4:1 or 12:1 ratio with multiplier of 12 limits the use of power tuning to (frequency)/2.
9. The PLL_MULT and PLL_RANGE(1:0) bits can be overwritten by JTAG commands and the BUS_CFG bits can be changed by SCOM commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note* for more details
10. Must be pulled down with a 10 kΩ resistor to GND.
11. The $\overline{\text{TRST}}$ signal must be pulled up to OV_{DD} with a 10 kΩ resistor.

Table 5-8. Input/Output Signal Descriptions (Page 3 of 4)

Pin Name	Width	In/Out	System/Debug Function	Notes
PLL_MULT	1	In	Selects the PLL multiplication factor: ‘0’ Multiply reference frequency by 12. ‘1’ Multiply reference frequency by 8.	9
PLL_RANGE(1:0)	2	In	To select the PLL frequency range, see *Table 5-2. PowerPC 970FX RISC Microprocessor PLL Configuration on page 64*.	9
PLLTEST	1	In	For manufacturing test use only.	4
PLLTESTOUT	1	Out	For measuring the PLL output (divide by 64).	—
PROCID(0:2)	3	In	System: processor ID maximum eight processors	—
PSRO_Enable	1	Out	For manufacturing test use only.	4
PSRO0	1	Out	For manufacturing test use only.	5
PSYNC	1	In	System: phase synchronization from North Bridge.	—
PSYNC_OUT	1	Out	System: Phase synchronization signal for observation that processors are in sync.	—
PULSE_SEL(0:2)	3	In		—
$\overline{\text{QACK}}$	1	In	System: acknowledgment of quiesce from the system.	—
$\overline{\text{QREQ}}$	1	Out	System: request from the processor to quiesce the system (nap mode).	—
RAMSTOP_ENABLE	1	In	For manufacturing test use only.	4
$\overline{\text{RI}}$	1	In	Dedicated manufacturing input.	1
SPARE	1	In/Out		—
SPARE2	1	In/Out		4
$\overline{\text{SRESET}}$	1	In	System: soft reset input.	—
SRIN(0:1)	2	In	System: PI snoop response input.	—
$\overline{\text{SRIN}}$(0:1)	2	In	System: PI inverse of snoop response input.	—
SROUT(0:1)	2	Out	System: PI snoop response output.	—
$\overline{\text{SROUT}}$(0:1)	2	Out	System: PI inverse of snoop response output.	—
SYNC_ENABLE	1	In	For manufacturing test use only.	4
SYSCLK $\overline{\text{SYSCLK}}$	2	In	System reference clock (differential input).	—

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal processor operation.
2. For I^2C or JTAG operation, the TCK and TDI signals must be pulled down to ground with a 10 kΩ resistor. See *Section 3.10.3* on page 43.
3. Bus ratios 8:1 and 16:1 are not supported for PI Input functionality.
4. These are test signals for factory use only and must be pulled down to GND for normal processor operation.
5. This signal should not be connected.
6. These pins can be used to measure on-chip voltage drop and noise. They should be connected to a backside probe point immediately behind the module. They should not be connected to GND and V_{DD} planes.
7. BiDi = bidirectional. OD = open drain.
8. Using the 4:1 or 12:1 ratio with multiplier of 12 limits the use of power tuning to (frequency)/2.
9. The PLL_MULT and PLL_RANGE(1:0) bits can be overwritten by JTAG commands and the BUS_CFG bits can be changed by SCOM commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note* for more details
10. Must be pulled down with a 10 kΩ resistor to GND.
11. The $\overline{\text{TRST}}$ signal must be pulled up to OV_{DD} with a 10 kΩ resistor.

Table 5-8. Input/Output Signal Descriptions (Page 4 of 4)

Pin Name	Width	In/Out	System/Debug Function	Notes
TBEN	1	In	System: time base enable.	—
TCK	1	In	JTAG: test clock that is separate from the system clock. Controls all test access port functions.	2
TDI	1	In	JTAG: serial input used to feed test data and test access port instructions.	2
TDO	1	Out	JTAG: Serial output used to extract data from the chip under test control.	—
$\overline{\text{THERM\_INT}}$	1	In	System: external thermal interrupt when low.	—
TMS	1	In	JTAG: Select used to control the operation of the JTAG state machine.	—
TRIGGERIN	1	In	External trigger to start trace collection.	—
TRIGGEROUT	1	Out	Signal that indicates that internal trace collection has begun.	—
$\overline{\text{TRST}}$	1	In	JTAG: asynchronous reset for the JTAG state machine.	11

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal processor operation.
2. For I^2C or JTAG operation, the TCK and TDI signals must be pulled down to ground with a 10 kΩ resistor. See *Section 3.10.3* on page 43.
3. Bus ratios 8:1 and 16:1 are not supported for PI Input functionality.
4. These are test signals for factory use only and must be pulled down to GND for normal processor operation.
5. This signal should not be connected.
6. These pins can be used to measure on-chip voltage drop and noise. They should be connected to a backside probe point immediately behind the module. They should not be connected to GND and V_{DD} planes.
7. BiDi = bidirectional. OD = open drain.
8. Using the 4:1 or 12:1 ratio with multiplier of 12 limits the use of power tuning to (frequency)/2.
9. The PLL_MULT and PLL_RANGE(1:0) bits can be overwritten by JTAG commands and the BUS_CFG bits can be changed by SCOM commands during the POR sequence. See the *PowerPC 970FX Power On Reset Application Note* for more details
10. Must be pulled down with a 10 kΩ resistor to GND.
11. The $\overline{\text{TRST}}$ signal must be pulled up to OV_{DD} with a 10 kΩ resistor.

5.8 Thermal Management Information

5.8.1 Thermal Management Pins

The PowerPC 970FX features an on-board temperature sensing diode, which connects to pins AA1 (DIODENEG) and Y1 (DIODEPOS).

This diode is calibrated at two points: a low temperature point and a high temperature point, both of which are relative terms. For example, the low temperature point can be 30°C and the high temperature point can be 85°C or 105°C. The actual values used for this calibration are stored in the fuse data of each chip. These two temperatures are applied externally with no self heating of the die, when the diode calibration is being done. At these two temperatures, with no power applied (V_{DD} = 0 V), a current of 100 μA is forced through the diode and the voltage drop is logged. The voltages at these two temperatures are also stored in the fuse data for each chip. Using these two temperature points and their corresponding voltage, a linear relationship is developed that correlates the voltage across the diode with a corresponding temperature. (See *Figure 5-3 PowerPC 970FX Thermal Diode Implementation* on page 76.) The chip temperature can be determined by interpreting the voltage across the diode pins when a controlled 100 μA current is forced through the diode by an external source. See the *Thermal Diode Calibration Application Note* for more details.

Other temperature sensors or monitoring hardware can also be implemented with the PowerPC 970FX and mounted as close to the PowerPC 970FX as practical. If the external temperature-sensing hardware determines that an unsafe operating temperature has been reached, the $\overline{\text{THERM\_INT}}$ input should be asserted to initiate either power management or shutdown of the system.

Note: The unsafe operating temperature setting is application dependent.

5.8.2 Reading Thermal Diode Calibration Data through JTAG

To access the thermal diode calibration data stored in each processor, a sequence of JTAG commands must be issued. By using JTAG commands, the data is accessed serially on the 970FX TDO pin and can also be read using the I^2C interface. Details for reading the thermal diode data are contained in the section about accessing thermal diode calibration data in the *PowerPC 970FX Power On Reset Application Note*. The temperature values and voltage values stored as fuse data must be interpreted as shown in *Table 5-9 Thermal Diode Data Encoding* on page 76.

This is a one-time only procedure. It is assumed the thermal diode calibration data stored in each processor is captured and stored in system read-only memory for subsequent use. This procedure is not meant to be run at every system startup because reading out this calibration data leaves the processor in an unusable state until it is restarted.

During the POR sequence, the processor comes to a WAIT state to allow the service processor to scan the MODE ring facility (address modifier x‘00C08000’, x‘00C04000’, or x‘00804001’). It is during this WAIT state that the thermal diode data can be scanned out. Scanning the MODE ring is not necessary.

Note: For correct fuse operation, ensure that the SPARE2 and SPARE_GND pins are tied to GND.

Figure 5-3. PowerPC 970FX Thermal Diode Implementation

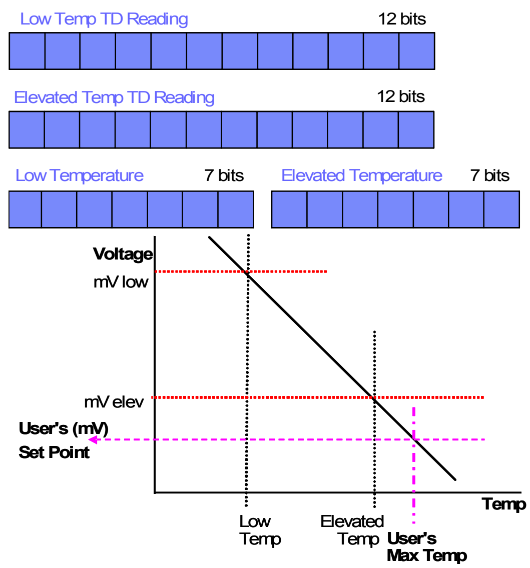


Table 5-9. Thermal Diode Data Encoding

Field Name	Ring Position	Offset within First 64-Bit Read	Length in Bits	Adjustment
temp_low	1546:1552	39:46	7	Value - 40
temp_high	1553:1559	32:38	7	None
voltage_low	1560:1571	20:31	12	Value/2 + 300
voltage_high	1572:1583	8:19	12	Value/2 + 300
Note: All values are stored least-significant bit to most-significant bit (bit reversed). They should be bit-swapped before applying the adjustments shown in this table. Temperatures are stored in degrees centigrade and voltages are stored in millivolts.				

5.8.3 Heatsink Attachment and Mounting Forces

Table 5-10 and *Figure 5-4* on page 77 describe the allowable forces for the PowerPC 970FX package. The heatsink design should not exceed these static or dynamic forces.

Table 5-10. Allowable Forces on the PowerPC 970FX RISC Microprocessor Package (Page 1 of 2)

Callout Number	Characteristic		Symbol	Maximum	Unit[1]	Note
1	Compressive force on chip	Static	F_C	133.5	N	
		Dynamic	F_C	133.5	N	

Note:

1. One newton = 0.2248089 pound-force.
2. The maximum force value for callout item 3 must include the force value for callout item 1. ($F_{BGA} + F_{C(Static)} < F_{BGA(Static)}$)

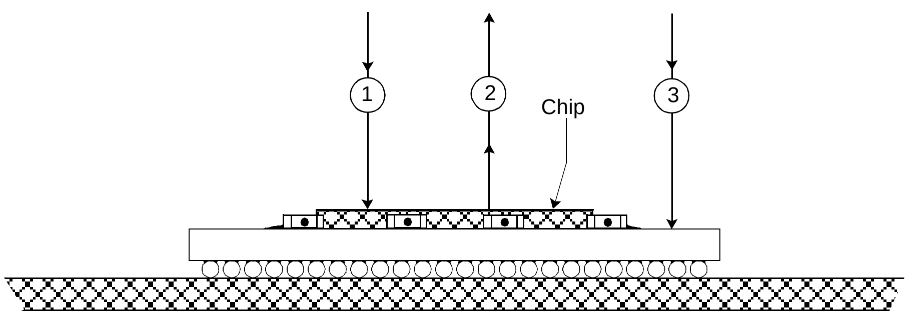
Table 5-10. Allowable Forces on the PowerPC 970FX RISC Microprocessor Package (Page 2 of 2)

Callout Number	Characteristic		Symbol	Maximum	Unit[1]	Note
2	Tensile force on chip	Static	F_T	0	N	
		Dynamic	F_T	17.6	N	
3	Compressive force on ball grid array balls	Static	F_{BGA}	90.3	N	2
		Dynamic	F_{BGA}	113.0	N	

Note:

1. One newton = 0.2248089 pound-force.
2. The maximum force value for callout item 3 must include the force value for callout item 1.
   ($F_{BGA} + F_{C(Static)} < F_{BGA(Static)}$)

Figure 5-4. Force Diagram for the PowerPC 970FX Package



Note:

1. The legend for this figure is provided by callout number in *Table 5-10*.

5.9 Operational and Design Considerations

5.9.1 Power-On Reset Considerations

For additional information, see the *PowerPC 970 RISC Microprocessor Power-On Reset Application Note.*

5.9.2 Debugging PowerPC 970FX Power-On and Reset Sequence

For additional information, see the *PowerPC 970 RISC Microprocessor Power-On Reset Application Note.*

5.9.3 I^2C Addressing of PowerPC 970FX

The I^2C address of PowerPC 970FX RISC Microprocessor is specified by the binary value ‘1000ppp’ where ppp = the settings of the processor ID bits PROCID(0:2). For example, if the PROCID bits are set to ‘000’ (pulled low), the I^2C address is ‘1000000’. If the PROCID bits are set to ‘001’, the I^2C address is ‘1000001’, and so forth.