IBM®

# IBM PowerPC®970MP RISC Microprocessor

# Datasheet

## Electrical Information

Version 1.0

July 31, 2006

IBM®



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July 31, 2006

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# About This Datasheet

This datasheet describes the IBM PowerPC PPC970MP™ RISC Microprocessor. The PowerPC PPC970MP™ is a dual core, 64-bit implementation of the IBM PowerPC® family of reduced instruction set computer (RISC) microprocessors that are based on the PowerPC Architecture™.

## Who Should Read This Datasheet

This datasheet is intended for designers who plan to develop products using the PowerPC PPC970MP.

## Related Publications

Related IBM publication includes the following:

- *PowerPC 970MP RISC Microprocessor Users Manual*
- *PowerPC 970MP Power On Reset Application Note*
- *PowerPC 970MP DD1.x Errata List*

**Note:** Subscribe to PowerPC at the IBM customer connect web site or contact your IBM Technical Support representative to verify that you have the latest version of the publication.

https://www-306.ibm.com/servlet/oem/edge/index.jsp

Other related publications include the following:

- *I2C Bus Specification*
  This document is produced by Philips Semiconductors and can be downloaded from the Philips Semiconductors web site.

## Conventions and Notations Used in This Datasheet

The use of overbars, for example $\overline{\text{DDEL\_OUT}}$, designates signals that are active low or the compliment

of differential signals.

The following software documentation conventions are used in this manual:

1. Function names are written in **bold** type. For example, **np_npms_proc_register ()**.
2. Variables are written in italic type. For example, *enable_mode*.
3. Keywords and data types are shown by being written all in capitals with underlines between words. For example, OFF_DISABLED.

# 1. General Information

## 1.1 Description

The IBM PowerPC PPC970MP RISC Microprocessor is a dual-core, 64-bit implementation of the IBM PowerPC® family of reduced instruction set computer (RISC) microprocessors that are based on the PowerPC Architecture. This dual microprocessor, also called the PowerPC PPC970MP, includes a Vector/SIMD facility which supports high-bandwidth data processing and compute-intensive operations. The PPC970MP is also designed to support multiple system organizations, including desktop and low-end server applications, up through 4-way SMP configurations.

**Note:** The IBM PowerPC PPC970MP incorporates two complete microprocessors on a single chip, along with some common logic to connect these microprocessors to a system. The terms microprocessor, processor, and processing unit (PU) will be used interchangeably to describe each of the two individual processors. The term core refers to the instruction fetch and execution logic, including the L1 caches, but excluding the storage subsystem, of each processor. The term PPC970MP refers to the single chip module comprising the two processors and common logic.

*Figure 1-1* on page 13 is a block diagram of a single PowerPC PPC970MP processor, indicating the main functional units of the core and storage subsystem (STS).

*Figure 1-2* on page 14 is a block diagram of the entire PPC970MP design, showing how the two processing units (PU0 and PU1) are connected through the common logic to the processor interface.

This document also provides pertinent physical characteristics of the PowerPC PPC970MP module.

## 1.2 Processor Features

- 64-bit implementation of the PowerPC AS Architecture Specification (Version 2.0)
  - Binary compatibility for all PowerPC AS application level code (problem state)
  - Binary compatibility for all PowerPC application level code (problem state)
  - Support for 32-bit O/S *bridge facility*
  - Vector/SIMD unit
- Layered implementation strategy for very high frequency operation
  - Deeply pipelined design
    - 16 stages for most fixed-point register-register operations
    - 18 stages for most load and store operations (assuming L1 Dcache hit)
    - 21 stages for most floating point operations
    - 19, 22, and 25 stages for fixed-point, complex-fixed, and floating point operations, respectively in the VALU.
    - 19 stages for VMX permute operations
- Dynamic instruction cracking for some instructions allows for simpler inner core dataflow
  - Dedicated dataflow for cracking one instruction into two internal operations
  - Microcoded templates for longer emulation sequences
- Speculative superscalar inner core organization
  - Aggressive branch prediction
    - Prediction for up to two branches per cycle
    - Support for up to 16 predicted branches in flight
    - Prediction support for branch direction and branch addresses

- In order dispatch of up to five operations into distributed issue queue structure
- Out of order issue of up to 10 operations into 10 execution pipelines
  - Two load or store operations
  - Two fixed-point register-register operations
  - Two floating-point operations
  - One branch operation
  - One condition register operation
  - One VMX permute operation
  - One VMX ALU operation
- Register renaming on GPRs, FPRs, VRFs, CR Fields, XER (parts), FPSCR, VSCR, VRSAVE, Link and Count

- Large number of instructions in flight (theoretical maximum of 215 instructions)
  - Up to 16 instructions in instruction fetch unit (fetch buffer and overflow buffer)
  - Up to 32 instructions in instruction fetch buffer in instruction decode unit
  - Up to 35 instructions in 3 decode pipe stages and 4 dispatch buffers
  - Up to 100 instructions in the inner-core (after dispatch)
  - Up to 32 stores queued in the STQ (available for forwarding)
- Fast, selective flush of incorrect speculative instructions and results

- Specific focus on storage latency management
  - Out-of-order and speculative issue of load operations
  - Support for up to 8 outstanding L1 cache line misses
  - Hardware initiated instruction prefetching from L2 cache
  - Software initiated data stream prefetching
    - Support for up to 8 active streams
  - Critical word forwarding / critical sector first
  - New branch processing / prediction hints added to branch instructions

- Power management
  - Static power management
    - Software initiated doze and nap and deep nap modes
  - Dynamic power management
    - Parts of the design stop their (hardware initiated) clocks when not in use
  - PowerTune
    - Software initiated slow down of the processor; selectable to half or quarter of the nominal operating frequency
    - Programmable latency for power mode transitions to control current spikes

## 1.3 PPC970MP Module Features

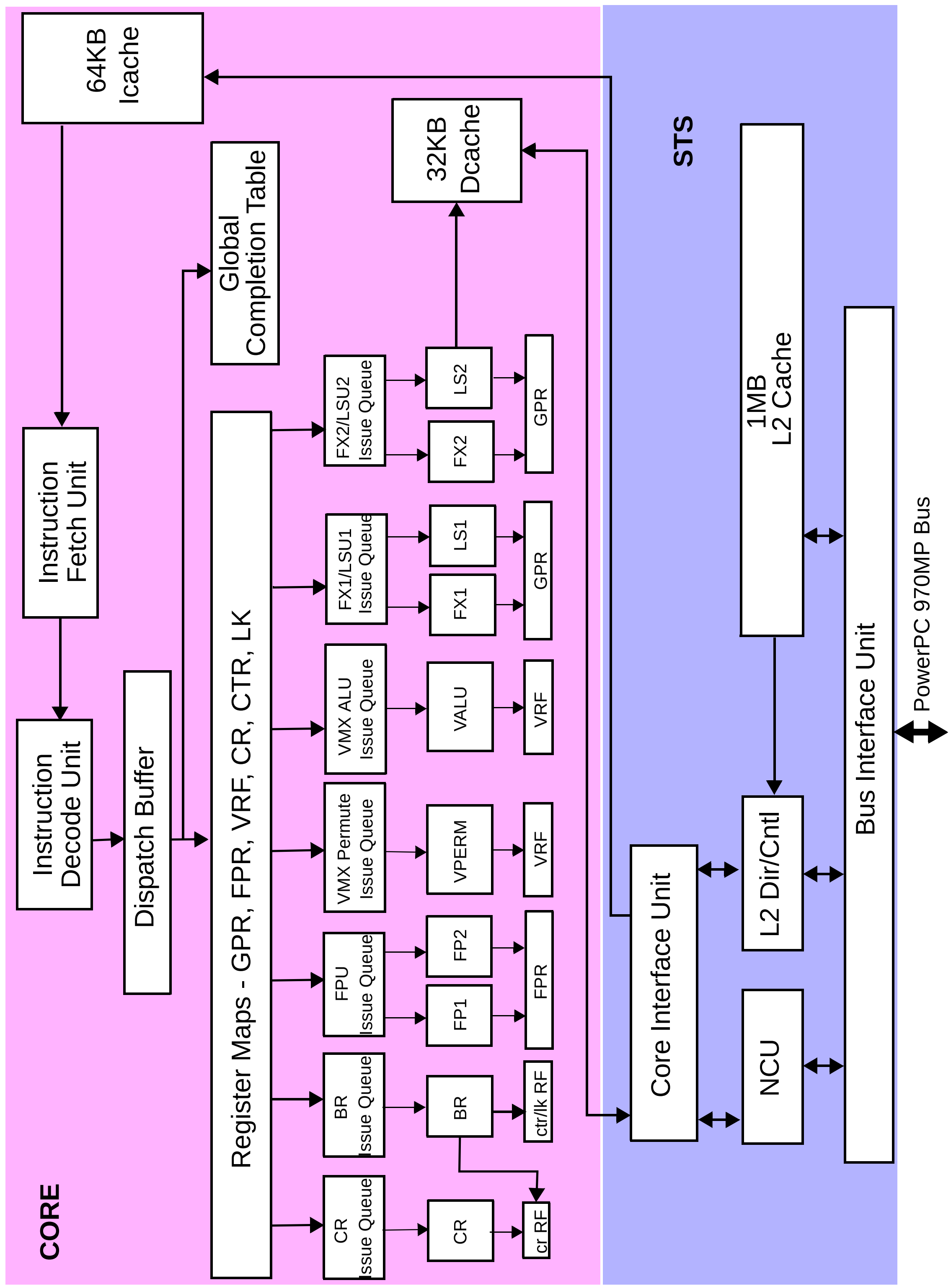
- Dual processors on a single die
  - Each processor has its own dedicated storage subsystem, including 1MB L2 cache per core.
  - Each processor has its own dedicated resets, external interrupt, thermal diode and voltage plane (common logic is powered on
  - Common logic provides arbitration for bus access between the two cores
  - Single external interface allows a companion chip with a single interface to support two processors

- Processor interface (PI) supports higher bus speeds

- Pervasive logic supports fencing off one processor for fault isolation or power management

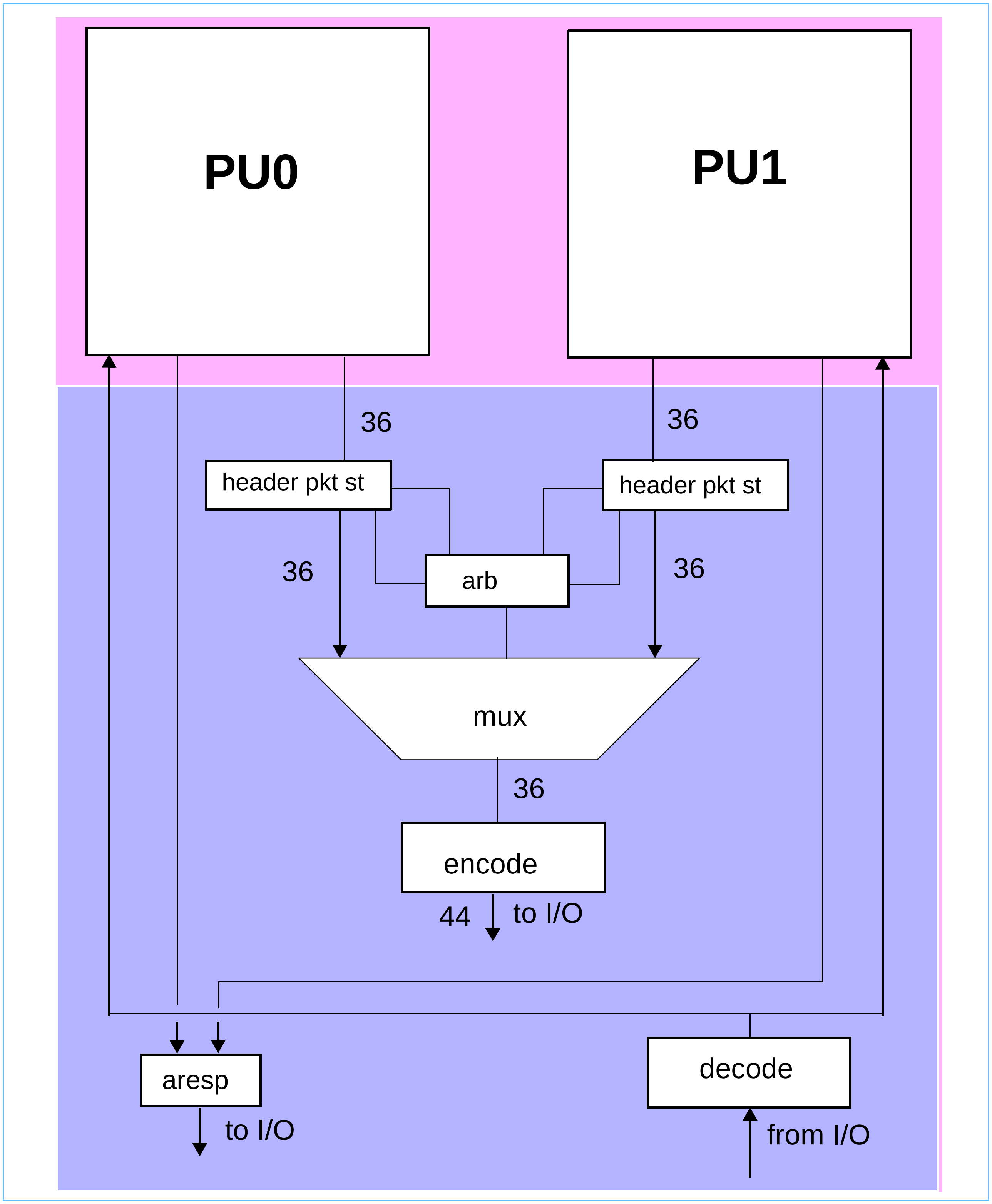
## 1.4 PowerPC 970MP Processing Unit Block Diagram

*Figure 1-1. PowerPC 970MP Processing Unit Block Diagram*



## 1.5 PowerPC 970MP Dual Core with Common Arbitration Logic

*Figure 1-2. PowerPC 970MP Dual Core with Common Arbitration Logic*



## 1.6 Ordering Information

The PowerPC 970MP has the following part numbers and Processor Version Register (PVR) values for the respective design revision levels.

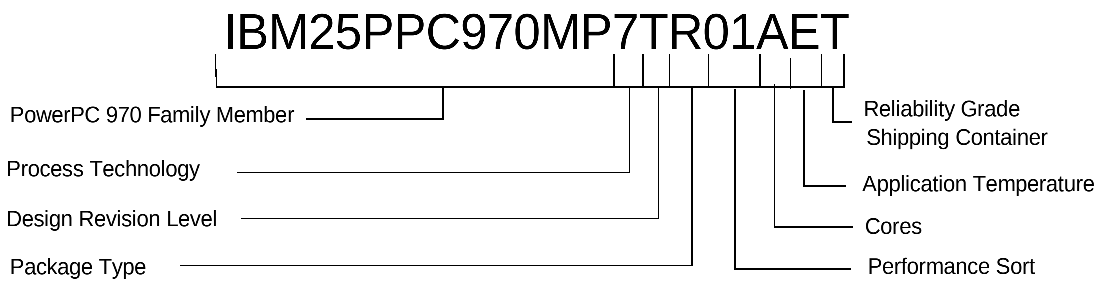
*Table 1-1. Power PC 970MP Ordering and Processor Version Register (PVR) Power Optimized*

| Order Part Number | Frequency GHz | Revision Level | PVR |
|---|---|---|---|
| IBM25PPC970MP7TR50AET | 1.2 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR60AET | 1.4 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR64AET | 1.6 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR67AET | 1.8 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR80AET | 2.0 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR84AET | 2.5 | DD1.1x | 0x00440101 |
| **Note:** Refer to *Table 3-6* for power and *Table 3-7* for voltage rating. | | | |

*Table 1-2. Power PC 970MP Ordering and Processor Version Register (PVR) Standard*

| Order Part Number | Frequency GHz | Revision Level | PVR |
|---|---|---|---|
| IBM25PPC970MP7TR01AET | 1.2 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR05AET | 1.4 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR20AET | 1.6 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR23AET | 1.8 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR30AET | 2.0 | DD1.1x | 0x00440101 |
| IBM25PPC970MP7TR40AET | 2.5 | DD1.1x | 0x00440101 |
| **Note:** Refer to *Table 3-8* for power and *Table 3-9* for voltage rating. | | | |

*Figure 1-3. Part Number Legend*




| | |
|---|---|
| Process Technology | 7 = 10KE (90 nm CSOI) |
| Design Revision Level | T = DD1.1x |
| Package Type | R = 576 CBGA Pb reduced |
| Perfromance sort | 01 = 1.2 GHz, Standard<br>05 = 1.4 GHz, Standard<br>20 = 1.6 GHz, Standard<br>23 = 1.8 GHz, Standard<br>30 = 2.0 GHz, Standard<br>40 = 2.5 GHz, Standard<br>50 = 1.2 GHz, Power Optimized<br>60 = 1.4 GHz, Power Optimized<br>64 = 1.6 GHz, Power Optimized<br>67 = 1.8 GHz, Power Optimized<br>80 = 2.0 GHz, Power Optimized<br>84 = 2.5 GHz, Power Optimized |
| Cores | A = Dual Core |
| Application Temperature | E = 105 $^{\circ}C$ |
| Reliability Grade<br>Shipping Container | T = Tray, Grade 2 Reliability<br>**Note 1:** Automatic array recovery must be enabled as detailed in the *POR Application Note*.<br>**Note 2:** Grade 2 is 25 FITs AFR (Average Failure Rate) @ 60$^{\circ}C$ for 40K and 100K POH (Power-on-Hours). |

# 2. General Parameters

*Table 2-1* provides a summary of the general parameters of the PowerPC PPC970MP.

*Table 2-1. General Parameters of the PowerPC 970MP*

| Item | Description | Notes |
|---|---|---|
| Maximum Die Size | 153.8 sq. mm | |
| Maximum Die Dimensions | 13.225 mm x 11.629 mm | |
| Transistor Count | 183 Million | 1 |
| Package | 575-pin Ceramic ball grid array (CBGA), 25x25mm (1.0mm pitch) | |

**Note:**
1. For information only. Use of this value to calculate reliability is not valid.

# 3. Electrical and Thermal Characteristics

This section provides both AC and DC electrical specifications and thermal characteristics for the PowerPC PPC970MP.

## 3.1 DC Electrical Characteristics

The tables in this section describe the PowerPC 970MP's DC electrical characteristics.

### 3.1.1 Absolute Maximum Ratings

*Table 3-1. Absolute Maximum Ratings*

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltages | V0,V1 ($V_{DD}$) | -0.3 to 1.5 | V | 1, 3 |
| I/O Supply Voltage | V2 ($OV_{DD}$) | -0.3 to 1.7 | V | 1, 3 |
| PLL supply voltage | $AV_{DD}$ | -0.3 to 3.0 | V | 1, 3 |
| Input voltage | $V_{IN}$ | -0.3 to 1.7 | V | 1, 2 |
| Storage temperature range | $T_{STG}$ | TBD | °C | 1 |

**Note:**
1. Functional and tested operating conditions are given in the Datasheet Supplement. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed above may affect device reliability or cause permanent damage to the device.
2. This is an implied DC voltage specification. Pending further evaluation, an allowance for AC overshoot or undershoot may be accommodated beyond this input voltage specification.
3. Power supply ramping recommendations:
   The order does not matter as long as the supplies reach their final destination in 2s.
   V0 can not exceed $OV_{DD}$ by more than 0.8V (Except for 2s during power up or down, where it is allowed to be ≤ 1.55V).
   $OV_{DD}$ can not exceed V0 by more than 0.8V (Except for 2s during power up/down, where it is allowed to be ≤ 1.5V).
   $AV_{DD}$ can not exceed V0 by more than 2.5V (Except for 2s during power up/down, where it is allowed to be ≤.2.75V).
   The V1 circuitry is independent of V0, $AV_{DD}$, and $OV_{DD}$.

*Table 3-2. Maximum Allowable Current on Kelvin Probe pins (DD1.1x)*

| Pin Name | Package Location | Maximum Current |
|---|---|---|
| CP0_KELV_GND0 | W2 | 2.7 mA |
| CP1_KELV_GND1 | W22 | 2.7 mA |
| CP0_KELV_V0 | AB4 | 2.7 mA |
| CP1_KELV_V1 | W21 | 2.7 mA |
| $KELV\_OV_{DD}$ | A10 | 13 mA |
| KELV_GND2 | B13 | 13 mA |

### 3.1.2 Recommended Operating Conditions

*Table 3-3. Recommended Operating Conditions*

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| PLL supply voltage[1] | $AV_{DD}$ | 2.70 ±50 mV | V |
| PLL supply current, max | $AI_{DD}$ | 20 | mA |
| I/O supply voltage | $OV_{DD}$ | 1.5 ±50 mV | V |
| I/O supply current, max[2] | $OI_{DD}$ | 2 | A |
| Input voltage | $V_{IN}$ | GND to $OV_{DD}$ | V |
| Thermal Diode temperature | $T_{DIODE}$ | 0 to 105 | °C |

**Note:** 1. The PLL supply voltage has been adjusted to account for the maximum possible DC drop across the filter circuit *Section 5.3 PLL Power Supply Filtering*

**Note:** 2. The I/O current is for regulator sizing and power distribution information only. The I/O power for thermal design is included in *Table 3-6 Power Consumption for Power-Optimized Parts* and *Table 3-8 Power Consumption for Standard Parts*

**Note:** These figures are preliminary and subject to change after characterization.

### 3.1.3 Package Thermal Characteristics

*Table 3-4. Package Thermal Characteristics*

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| CBGA thermal conductance to board | $\theta_{JB}$ | 5.4 | °C/W |

### 3.1.4 DC Electrical Specifications

*Table 3-5. DC Electrical Specifications*

| Characteristic | Symbol | Voltage | | Unit | Notes |
|---|---|---|---|---|---|
| | | Minimum | Maximum | | |
| SYSCLK, $\overline{\text{SYSCLK}}$ input high voltage | — | 0.7 x $OV_{DD}$ | $OV_{DD}$ + 0.3 | V | 1 |
| SYSCLK, $\overline{\text{SYSCLK}}$ input low voltage | — | -0.3 | 0.3 x $OV_{DD}$ | V | 1 |
| Processor Interface (PI) input high voltage | $V_{IH}$ | (0.5 x $OV_{DD}$) + 0.2 | — | V | 2 |
| Processor Interface (PI) input low voltage | $V_{IL}$ | — | (0.5 x $OV_{DD}$) - 0.2 | V | 2 |
| Non-PI input high voltage | $V_{IH}$ | 0.7 x $OV_{DD}$ | — | V | 3 |
| Non-PI input low voltage | $V_{IL}$ | — | 0.3 x $OV_{DD}$ | V | 3 |
| PI output high voltage | $V_{OH}$ | 0.78 x $OV_{DD}$ | — | V | 4 |
| PI output low voltage | $V_{OL}$ | — | 0.22 x $OV_{DD}$ | V | 4 |
| Non-PI output high voltage, $I_{OH}$ = -2mA | $V_{OH}$ | $OV_{DD}$ - 0.2 | — | V | — |
| Non-PI output low voltage, $I_{OL}$ = 2mA | $V_{OL}$ | — | 0.2 | V | — |
| OD output low, IOL = 2mA (CHKSTOP, I2CGO) | $V_{OL}$ | — | 0.2 | V | 5 |
| OD output low, IOL = 5mA (I2C) | $V_{OL}$ | — | 0.2 | V | — |
| Input leakage current, $V_{IN}$ = $OV_{DD}$ and $V_{IN}$ = 0 | $I_{IN}$ | — | 60 | µA | — |
| Hi-Z (off state) leakage current, $V_{OUT}$ = $OV_{DD}$ and $V_{OUT}$ = 0 | $I_{TSO}$ | — | 60 | µA | — |
| Input Capacitance, $V_{IN}$ = 0 V, f = 1MHz | $C_{IN}$ | — | 5.0 | pF | 6 |

**Notes:**

1. SYSCLK differential receiver requires HSTL differential signaling level. See the JEDEC HSTL standard.
2. Section 3.5 Processor Interconnect Specifications on Page 26. Minimum input must meet the EYE OPENING REQUIREMENTS of the link.
3. The JTAG signals TDI, TMS, and $\overline{\text{TRST}}$ do not have internal pullups; therefore, pullup must be added on the board. Pullups should be added and adjusted according to the system implementation. These input/outputs meet the DC specification in the JEDEC standard JESD8-11 for 1.5V Normal Power Supply Range.
4. A 100Ω split terminator is the test load. Note a 40Ω driver has an up level of (0.78 x $OV_{DD}$) for $V_{OH}$ and (0.22 x $OV_{DD}$) at $V_{OL}$. See Section 3.5 Processor Interconnect Specifications on Page 26 for information about other drivers.
5. There are two open drain signals on this type of driver: CHKSTOP and $I^2$CGO. The pullup for these nets depend on the rise time requirement, net load, and topology. The following are two bounding suggestions based on a point-to-point 50Ω net with two lengths (5cm and 61cm). A 33Ω series source terminator was added in both runs.

   Examples:
   500Ω Pullup DC Low Level 0.18V @ Receiver
   Trise 0.2V - 0.8V = 55ns @ 61cm
   Trise 0.2V - 0.8V = 10ns @ 5cm

   1KΩ Pullup DC Low Level 0.13V @ Receiver
   Trise 0.2V - 0.8V = 115ns @ 61cm
   Trise 0.2V - 0.8V = 20ns @ 5cm
6. Capacitance values are guaranteed by design and characterization, and are not tested.

### 3.1.5 Power Consumption

#### *3.1.5.1 Power Table for Power Optimized Parts*

*Table 3-6. Power Consumption for Power-Optimized Parts*

| Frequency | Condition | Voltage | Power (W) | Power Int[1] (W) | Doze Power | Nap Power | Notes |
|---|---|---|---|---|---|---|---|
| 1.2 GHz | Typical Average @ 65C | See *Table 3-7* | 23 | - | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | - | - | 3 |
| | Maximum @ 105C | | 28 | 24.4 | - | - | 2,3 |
| 1.4 GHz | Typical Average @ 65C | See *Table 3-7* | 28 | - | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 35 | 30.5 | - | - | 2,3 |
| 1.6 GHz | Typical Average @ 65C | See *Table 3-7* | 32 | - | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 40 | 34.8 | - | - | 2,3 |
| 1.8 GHz | Typical Average @ 65C | See *Table 3-7* | 40 | - | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 50 | 43.5 | - | - | 2,3 |
| 2.0 GHz | Typical Average @ 65C | See *Table 3-7* | 48 | - | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 60 | 52.2 | - | - | 2,3 |
| 2.5 GHz | Typical Average @ 65C | See *Table 3-7* | 92 | - | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 115 | 100 | - | - | 2,3 |

1. Maximum power numbers are measured by tester code that includes FP & VMX instructions. Characterizion results indicate that similar power test code that is integer only is an average of 13 % less. The values in this column are not tested but based on the characterization information. The FP and VMX units are automatically clock gated when not in use.
2. Maximum power is projected at the nominal $V_{DD}$ worst case Iddq, and max temperature as specified
3. Voltage tolerance is per the $V_{DD}$ Fuse Code, VFC, *Table 3-7*

### *3.1.5.2 Voltage Table for Power Optimized Parts*

V0 and V1 voltage information for the PPC970MP is stored in the fuse ring of each core of the microprocessor using a 3 bit code, with one parity bit. This information should be read for core 0 and the board voltages set appropriately. See Section 5.9.2 "VFC Fusing Implementation," on page 67 for more information.

*Table 3-7. 970MP V0 and V1, $V_{DD}$*

| $V_{DD}$ Fuse Code, Parity | **1.2 GHz** | **1.4 GHz** | **1.6 GHz** | **1.8 GHz** | **2.0 GHz** | **2.5 GHz** |
|---|---|---|---|---|---|---|
| | V0 and V1 $\pm 50$ mV | V0 and V1 $\pm 50$ mV | V0 and V1 $\pm 50$ mV | V0 and V1 $\pm 50$ mV | V0 and V1 $\pm 50$ mV | V0 and V1 $\pm 50$ mV |
| 001,1 | 0.950 V | 0.950 V | 0.950 V | 0.950 V | 1.000 V | 1.200 V |
| 010,1 | 0.975 V | 0.975 V | 0.975 V | 0.975 V | 1.025 V | 1.225 V |
| 011,0 | 1.000 V | 1.000 V | 1.000 V | 1.000 V | 1.050 V | 1.250 V |
| 100,1 | 1.025 V | 1.025 V | 1.025 V | 1.025 V | 1.075 V | 1.275 V |
| 101,0 | 1.050 V | 1.050 V | 1.050 V | 1.050 V | 1.100 V | 1.300 V |
| 110,0 | 1.075 V | 1.075 V | 1.075 V | 1.075 V | 1.125 V | 1.325 V |
| 111,1 | 1.100 V | 1.100 V | 1.100 V | 1.100 V | 1.150 V | 1.350 V |

**Notes:**

1. Voltage and tolerance should be measured at CP0_KELV_V0 and CP0_KELV_GND0 for $V_{DD}$Core0, CP1_KELV_V1 and CP1_KELV_GND1 for $V_{DD}$Core1.. Most applications should expect an offset between these Kelvin pins and the Voltage and Ground plane(s) of the PCB which will be design dependent and should be verified by characterization.
2. The entry for 111,1 should be used as the Boot voltage, see Section 5.9.3 on Page 67

### *3.1.5.3 Power Table for Standard Parts*

*Table 3-8. Power Consumption for Standard Parts*

| Frequency | Condition | Voltage | Power (W) | Power Int[1] (W) | Doze Power | Nap Power | Notes |
|---|---|---|---|---|---|---|---|
| 1.2 GHz | Typical Average @ 65C | See *Table 3-9* | 26 | | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | - | - | 3 |
| | Maximum @ 105C | | 32 | 27.8 | - | - | 2,3 |
| 1.4 GHz | Typical Average @ 65C | See *Table 3-9* | 32 | | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 40 | 34.8 | - | - | 2,3 |
| 1.6 GHz | Typical Average @ 65C | See *Table 3-9* | 36 | | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 45 | 39.2 | - | - | 2,3 |
| 1.8 GHz | Typical Average @ 65C | See *Table 3-9* | 44 | | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 55 | 47.9 | - | - | 2,3 |

*Table 3-8. Power Consumption for Standard Parts*

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 2.0 GHz | Typical Average @ 65C | See *Table 3-9* | 56 | | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 70 | 60.9 | - | - | 2,3 |
| 2.5 GHz | Typical Average @ 65C | See *Table 3-9* | 100 | | - | - | 3 |
| | Maximum @ 85C | | TBD | TBD | TBD | TBD | 3 |
| | Maximum @ 105C | | 125 | 108.8 | - | - | 2,3 |

1. Maximum power numbers are measured by tester code that includes FP & VMX instructions. Characterizion results indicate that similar power test code that is integer only is an average of 13 % less. The values in this column are not tested but based on the characterization information. The FP and VMX units are automatically clock gated when not in use.
2. Maximum power is projected at the nominal $V_{DD}$ worst case Iddq, and max temperature as specified
3. Voltage tolerance is per the $V_{DD}$ Fuse Code, VFC, *Table 3-9*

### *3.1.5.4 Voltage Table for Standard Parts*

V0 and V1 voltage information for the 970MP is stored in the fuse ring of each core of the microprocessor using a 3 bit code, with one parity bit. This information should be read for core 0 and the board voltages set appropriately. See Section 5.9.2 “VFC Fusing Implementation,” on page 67 for more information

*Table 3-9. 970MP V0 and V1, $V_{DD}$*

| $V_{DD}$ Fuse Code, Parity | **1.2 GHz** | **1.4 GHz** | **1.6 GHz** | **1.8 GHz** | **2.0 GHz** | **2.5 GHz** |
|---|---|---|---|---|---|---|
| | V0 and V1 +/- TBD mV | V0 and V1 +/- TBD mV | V0 and V1 +/- TBD mV | V0 and V1 +/- TBD mV | V0 and V1 +/- TBD mV | V0 and V1 +/- TBD mV |
| 001,1 | 0.950 V | 0.950 V | 0.950 V | 0.950 V | 1.000 V | 1.200 V |
| 010,1 | 0.975 V | 0.975 V | 0.975 V | 0.975 V | 1.025 V | 1.225 V |
| 011,0 | 1.000 V | 1.000 V | 1.000 V | 1.000 V | 1.050 V | 1.250 V |
| 100,1 | 1.025 V | 1.025 V | 1.025 V | 1.025 V | 1.075 V | 1.275 V |
| 101,0 | 1.050 V | 1.050 V | 1.050 V | 1.050 V | 1.100 V | 1.300 V |
| 110,0 | 1.075 V | 1.075 V | 1.075 V | 1.075 V | 1.125 V | 1.325 V |
| 111,1 | 1.100 V | 1.100 V | 1.100 V | 1.100 V | 1.150 V | 1.350 V |

**Notes:**

1. Voltage and tolerance should be measured at CP0_KELV_V0 and CP0_KELV_GND0 for $V_{DD}$Core0, CP1_KELV_V1 and CP1_KELV_GND1 for $V_{DD}$Core1.. Most applications should expect an offset between these Kelvin pins and the Voltage and Ground plane(s) of the PCB which will be design dependent and should be verified by characterization
2. The entry for 111,1 should be used as the Boot voltage, see Section 5.9.3 on Page 67

## 3.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PowerPC PPC970MP. After fabrication, parts are sorted by maximum processor core frequency as shown in *Section 3.3 Clock AC Specifications*, and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the SYSCLK and the settings of the PLL_MULT signal.

This section only describes asynchronous and mode-select inputs and outputs. For bus timing information, see Section 3.5 Processor Interconnect Specifications on Page 26.

## 3.3 Clock AC Specifications

*Table 3-10* provides the clock AC timing specifications as defined in *Figure 3-1* on page 24.

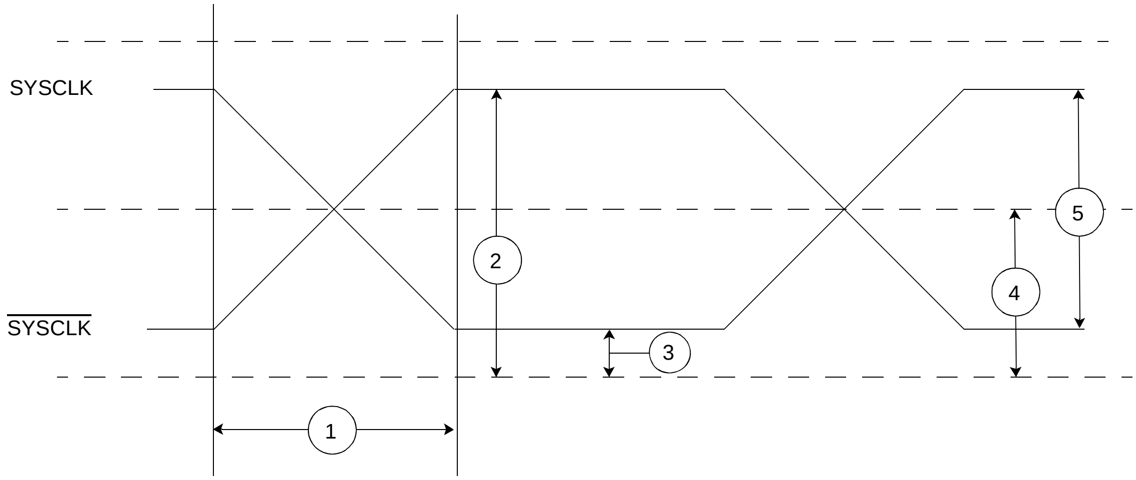
*Table 3-10. Clock AC Timing Specifications*

| Call Out Number | Characteristic | Value | | Unit | Notes |
|---|---|---|---|---|---|
| | | Minimum | Maximum | | |
| — | SYSCLK frequency | 100 | 700 | MHz | 1, 2, 4, 8 |
| — | SYSCLK input jitter (cycle to cycle period jitter) | — | ±75 | ps | 4 |
| 1 | SYSCLK rise and fall time | — | 500 | ps | 3, 4, 5 |
| 2 | SYSCLK and $\overline{\text{SYSCLK}}$ input high voltage | — | $OV_{DD}$ + 0.3 | V | 4, 5 |
| 3 | SYSCLK and $\overline{\text{SYSCLK}}$ input low voltage | -0.3 | — | V | 4, 5 |
| 4 | Differential Crossing Point voltage | 0.4 x $OV_{DD}$ | 0.6 x $OV_{DD}$ | V | 4, 5 |
| 5 | Differential voltage \| (SYSCLK - $\overline{\text{SYSCLK}}$) \| | 0.385 | 1.6 | V | 4, 7, 5 |
| — | PLL lock time | — | 800 | µSec | 4, 6 |
| — | Duty Cycle | 40% | 60% | — | — |

**Notes:**

1. **Important:** Processor frequency is determined by PLL_MULT and SYSCLK input frequency. PLL_RANGE(1:0) must be set to the correct values for expected processor frequency. Consult *Table 5-1. PowerPC 970MP Bus Configuration on page 53* for the allowable frequency range for these pins. **Caution:** The PLL_MULT and PLL_RANGE bits may be overwritten by JTAG commands (ie, in test mode) during the POR (power on reset) sequence. Refer to the PowerPC 970MP Power On Reset Application Note for more details.
2. PowerPC PPC970MP minimum processor frequency will be determined by characterization. The minimum frequency is an estimation.
3. Rise and fall times for the SYSCLK inputs are measured from 0.4 to 1.0V.
4. **Important:** The data in this table is based on simulation and may be revised after hardware characterization.
5. For a timing diagram, see *Figure 3-1*.
6. Guaranteed by design and not tested.
7. The differential voltage is the minimum peak to peak voltage on both the SYSCLK and $\overline{\text{SYSCLK}}$ pins (similar to what would be measured with single ended oscilloscope probes)
8. SYSCLK minimum frequency is for PLL mode. In PLL bypass mode ($\overline{\text{BYPASS}}$ low), SYSCLK frequency may be as low as 10MHz when not in functional mode (i.e. reading the fuse ring).

*Figure 3-1. Clock Differential HSTL Signal*




**Note:** The legend for this figure is provided in *Table 3-10 Clock AC Timing Specifications*.

To determine the core clock, multiply the SYSCLK by one of the following:

- 12 for PLL_MULT = 0
- 8 for PLL_MULT = 1

For more information about the PLL configuration, see *Table 5-2* on page 54.

## 3.4 Core-Clock Timing Relationship Between PSYNC and SYSCLK

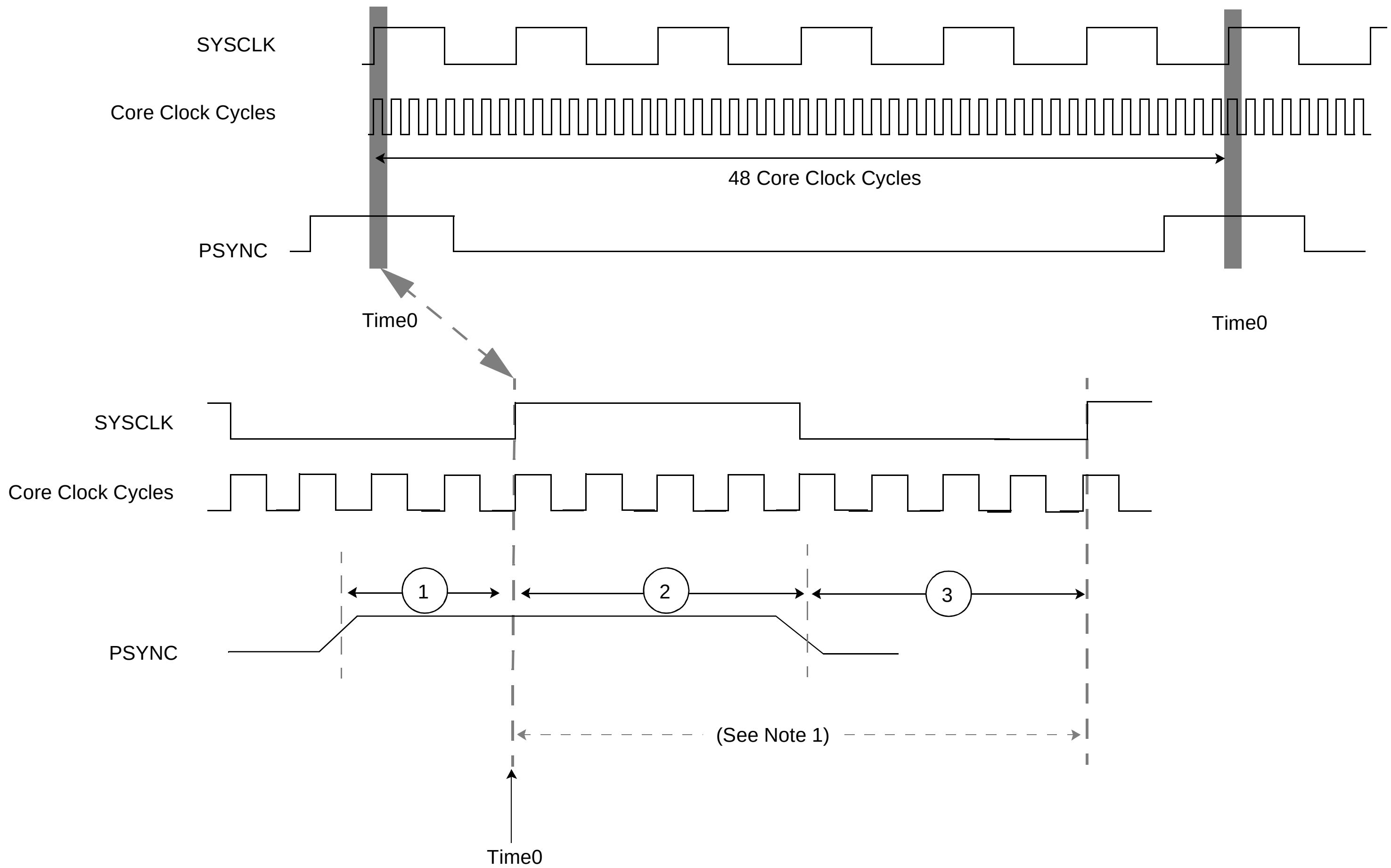
*Table 3-11* and *Figure 3-2. Core-Clock Timing Relationship Between PSYNC and SYSCLK* provide a description of the processor-clock timing relationship between PSYNC and SYSCLK.

*Table 3-11. Core-Clock Timing Relationship Between PSYNC and SYSCLK*

| Call Out Number | Characteristic | | Value | | Unit |
|---|---|---|---|---|---|
| | | | Minimum | Maximum | |
| 1 | Setup time | $t_{SETUP}$ | 600 | — | ps |
| 2 | Hold time | $t_{HOLD}$ | 100 | — | ps |
| 3 | Guard time | $t_{GUARD}$ | 600 | — | ps |

**Note:** See *Figure 3-2* on page 25 for the corresponding timing diagram.

*Figure 3-2. Core-Clock Timing Relationship Between PSYNC and SYSCLK*




**Notes:**

1. The maximum rate of occurrence between PSYNCs is 48 core clock cycles independent of the PLL multiplier. One pulse per 24 SYSCLKs is suggested.
2. The legend for this figure is provided by callout number in *Table 3-11* on page 24.

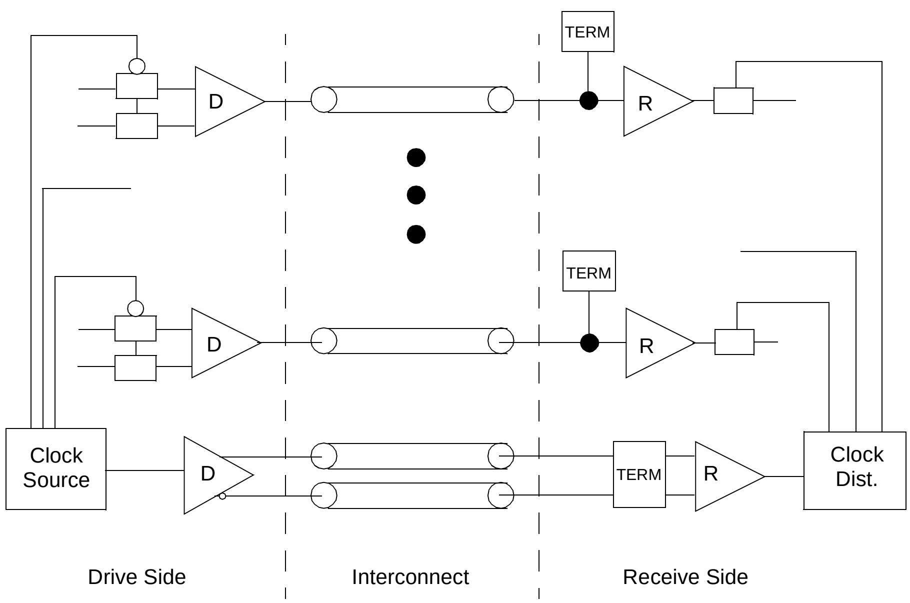
## 3.5 Processor Interconnect Specifications

### 3.5.1 Electrical and Physical Specifications

#### *3.5.1.1 Source Synchronous Bus (SSB)*

*Figure 3-3* depicts a representative block diagram of an SSB for a PowerPC 970MP Processor Interconnect implementation. Each SSB consists of three major subsections: the drive side, the module-to-module interconnect, and the receive side. Data is first either Balance-Coding-Method (BCM) encoded or checksummed, then clock-phase multiplexed, and finally launched from the drive side onto the module interconnect. The receive side includes far-end termination and circuitry to demultiplex, deskew data, align clocks, and synchronize the received data.

*Figure 3-3. Block Diagram of an SSB for aPPC970MPProcessor Interconnect Implementation*




NOTE: The PI on-chip termination network can consume several watts of power. To minimize power consumption, It may be possible to disable the on-chip termination through careful selection of bus speed and detailed modeling of the board layout.

#### *3.5.1.2 Drive Side Characteristics*

*Figure 3-4* shows a typical implementation for a single-ended line. The drivers are of the push-pull type with a nominal impedance (R0 of 20 ohms) that overdrives the line impedance. The nominal swing at the receiver, terminated with resistance (TR0 of 110 ohms) to each rail, is 13% $OV_{DD}$ to 87% $OV_{DD}$. R0 is 20 ohms when the driver is in the low output impedance mode. The 20 ohm setting is suitable for all bus speeds. The PPC970MP has a 40 ohm nominal output impedance mode that is suitable for bus speeds below 800 MT/s in some applications.

The maximum skew between any of the outputs is 150 ps at the BGA pin. The maximum interconnect skew on the card(s) between any two outputs must be less than 150 ps. The interconnect skew on the card(s) between any two inputs must be less than 300 ps.

*Figure 3-4. Typical Implementation for a Single-ended Line*

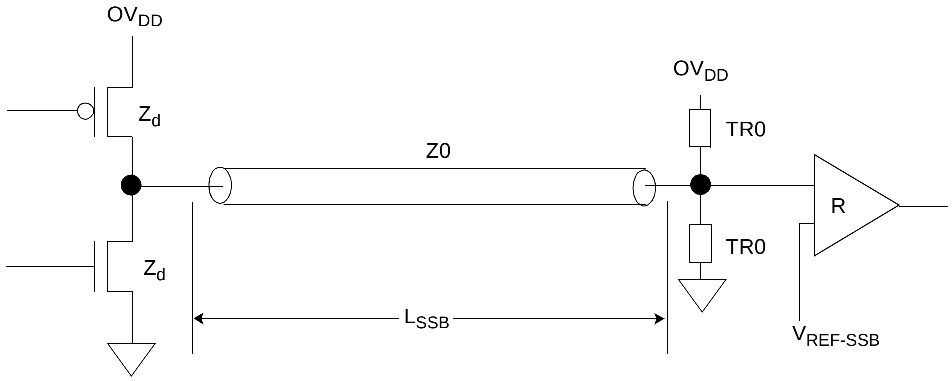



*Table 3-12. Processor Interconnect SSB Driver Specifications*

| Symbol | Description | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OH}DC$ | High output level at DC | | 0.87 $OV_{DD}$ | | mV | |
| $V_{OL}DC$ | Low output level at DC | | 0.13 $OV_{DD}$ | | mV | |
| $T_{DR}$ | Driver rise time | 70 | 133 | 171 | ps | 20% to 80% of swing |
| $T_{DF}$ | Driver fall time | 81 | 155 | 162 | ps | 20% to 80% of swing |
| $Z_D$ | Driver output impedance | 15 | 20 | 25 | Ohms | Low Ohm mode |
| $Z_D$ | Driver output impedance | 30 | 40 | 50 | Ohms | High Ohm mode |

### 3.5.1.3 Module-to-Module Interconnect Characteristics

All traces are to be routed as striplines or microstrip. The tolerance on trace impedance is 10%. Care must be taken when mixing transmission line styles to manage propagation delay differences. The clock delay should be longer than the longest data delay for bus speeds at or above 1.1 Gb/s or on lines above 13 cm.

*Table 3-13. Processor Interconnect SSB PCB Trace Specifications*

| Symbol | Description | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $L_{SSB}$ | Trace length | | | 18 | cm | For transfer speeds of 1.5G/s. |
| | | | | 22.5 | cm | For transfer speeds of 1.0G/s. |
| $Z_0$ | Trace impedance | 45 | 50 | 55 | Ohms | |
| $S_{DPCB}$ | PCB data trace skew | | | 150 | ps | |

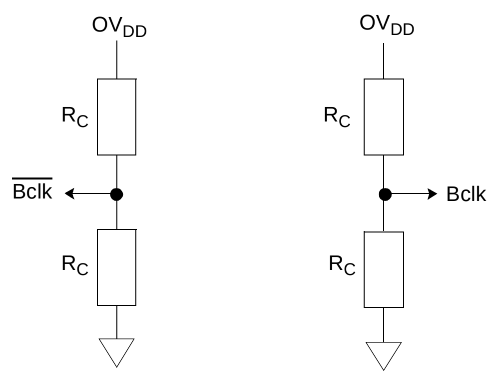
### *3.5.1.4 Receive Side Characteristics*

The receive side contains far-end termination circuitry as shown in *Figure 3-4* for the single-end lines. The total skew from the drive side to the module input pins on the receive side is 350ps ($S_{DS}$+ $S_{PCB}$) between any two signals (clocks or data). The differential clock termination scheme is shown in *Figure 3-5*. All receivers are pseudo-differential with reference to $V_{REF\text{-}SSB}$ and with common-mode rejection of at least $0.5 \times V_{DD}$. $V_{REF\text{-}SSB}$ may be generated internally by the receive-side circuitry or may be derived from the supply voltage.

*Table 3-14. Processor Interconnect SSB Receiver Specifications*

| Symbol | Description | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{REF\text{-}SSB}$ | SSB reference voltage | | 0.5 x $OV_{DD}$ | | mV | ($V_{OH}$DC + $V_{OL}$DC)/2 |
| $Bclk_{DC}$ | Bus clock duty cycle | 48 | 50 | 52 | % | |
| TR0 | Single-ended terminator | 83 | 110 | 137 | Ohms | 110 +/-25% |

*Figure 3-5. Differential Clock Termination Circuitry*

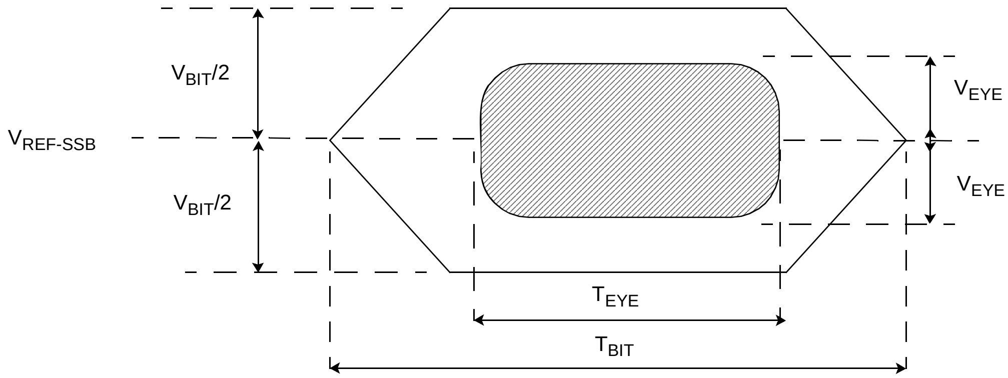



For high-performance operation, the PI supports the inclusion and operation of receive-side circuitry for clock alignment and individual bit-level deskew. An initialization alignment procedure (IAP) is activated at power-on reset (POR) for bit-level deskew and clock alignment. The IAP uses delay elements in the receive-side circuitry to first equalize the delay of the incoming data signals and then center the clock transition in the timing window. The timing parameters for the delay elements and flip-flops that register the data signals are summarized in *Table 3-15*.

*Table 3-15. Processor Interconnect SSB Timing Parameters for the Deskew and Clock Alignment*

| Symbol | Description | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{BIT}$ | Bit time | | 1/(2xBclk) | | ns | |
| $T_{DED}$ | Delay element time increment | 18 | 25 | 35 | ps | Thirty-one delay elements for data |
| $T_{DEC}$ | Delay element time increment | 18 | 25 | 35 | ps | Sixty-four delay elements for clock |

*Figure 3-6. Post-IAP Eye Opening*




The reference level for $V_{EYE}$ is $V_{REF-SSB}$. Horizontal ($T_{EYE}$) eye opening is a function of the bit time ($T_{BIT}$) and the earliness of the bus clock transition relative to the slowest data signal.

*Table 3-16. Eye-Size Requirements*

| Bit Rate (Mb/s) | CPU Bus Ratio | CPU Core (MHz) | Step Time (ps) | Eye Requirement (ps) | Bit Time (ps) | Eye/Bit Time | $V_{EYE}$ (Minimum) |
|---|---|---|---|---|---|---|---|
| 400 | 3 | 1200 | 31.9 | 863 | 2500 | 34.5% | 150mv |
| 450 | 3 | 1350 | 31.9 | 797 | 2222.2 | 34.5% | 150mv |
| 500 | 3 | 1500 | 31.9 | 744 | 2000 | 37.2% | 150mv |
| 500 | 2 | 1000 | 31.9 | 744 | 2000 | 37.2% | 150mv |
| 666 | 3 | 1998 | 27.8 | 605 | 1501.5 | 40.3% | 150mv |
| 666 | 2 | 1332 | 31.9 | 625 | 1501.5 | 41.6% | 150mv |
| 866 | 2 | 1732 | 31.9 | 544 | 1154.7 | 47.1% | 150mv |
| 1066 | 2 | 2132 | 26.0 | 465 | 938.1 | 49.6% | 150mv |

## 3.6 Input AC Specifications

This section provides specifications for pins: CP0_INT, CP1_INT, MCP, CP0_QACK, CP1_QACK, CP0_HRESET, CP1_HRESET, CP0_SRESET, CP1_SRESET, and TBEN. *Table 3-17*, *Table 3-18* and *Table 3-19* provide the input AC timing specifications as defined in *Figure 3-7. Asynchronous Input Timing*.

*Table 3-17. Input AC Timing Specifications for pins: CP0_INT, CP1_INT, MCP, CP0_QACK, CP1_QACK, CP0_SRESET, CP1_SRESET*

| Call Out Number | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | Rise time | — | <1 | ns |
| 2 | Pulse width | 10 | — | ns |
| 3 | Fall time | — | <1 | ns |

*Table 3-18. Input AC Timing Specifications for CP0_HRESET and CP1_HRESET*[1]

| Call Out Number | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | Rise time | — | <1.5 | ns |
| 2 | Pulse width | 50 | — | ns |
| 3 | Fall time | — | <1.5 | ns |

1.Assumes that the power was up previously and the PLL is locked. This implies SYSCLK is running.

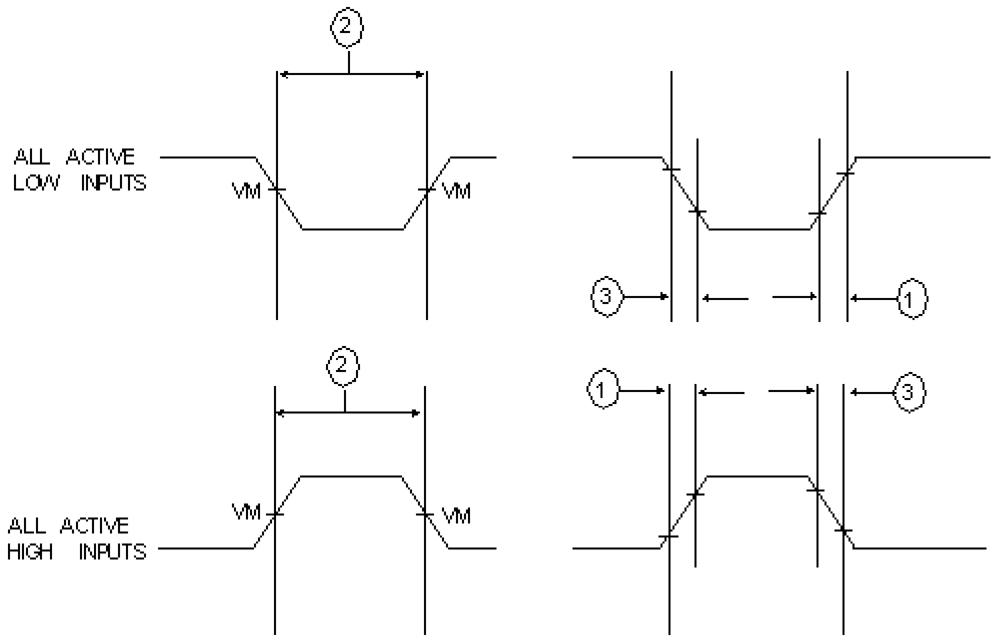
*Table 3-19. Input AC Timing Specifications for pins: TBEN*

| Call Out Number | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | Rise time | — | <1 | ns |
| 2 | Pulse width | $8*T_{full}$[1] | — | ns |
| 3 | Fall time | — | <1 | ns |

1. $T_{full}$ is the clock period of the full frequency processor clock.

**Note:** For bus timing information, see Section 3.5 Processor Interconnect Specifications on Page 26.

*Figure 3-7. Asynchronous Input Timing*




**Notes:**
1. No reference to SYSCLK because these inputs are sampled using the internal core clock.
2. VM = Midpoint Voltage ($OV_{DD}$/2)
3. These timings refer to the following pins: $\overline{\text{CP0\_INT}}$, $\overline{\text{CP1\_INT}}$, $\overline{\text{MCP}}$, $\overline{\text{CP0\_QACK}}$, $\overline{\text{CP1\_QACK}}$, $\overline{\text{CP0\_SRESET}}$, $\overline{\text{CP1\_SRESET}}$, $\overline{\text{CP0\_HRESET}}$, $\overline{\text{CP1\_HRESET}}$, TBEN.
4. The legend for this figure is provided in *Table 3-17*, *Table 3-18* and *Table 3-19*.
5. Rise and fall times are specified from 20% to 80%

### 3.6.1 TBEN Input Pin

The TBEN input pin can be used as either an enable for the internal timebase/decrementer or as an external clock input. The mode is controlled by the setting of HID0 bit 19.  When this bit is 0, the timebase and decrementer update at 1/16th the processor core frequency whenever TBEN is pulled up to $OV_{DD}$ (traditional enable mode for the internal timebase/decrementer). When HID0 bit 19 is 1, the timebase and decrementer are clocked by the rising edge of TBEN (external clock input mode). When the external clock input mode is used the TBEN input frequency must not exceed 1/16th of the core processor’s maximum frequency.

## 3.7 Asynchronous Output Specifications

This section describes the asynchronous outputs and bi-directionals. Timing information is not provided because these signals are launched by the internal core clock.

*Table 3-20*, *Table 3-21*, and *Table 3-22* list the signals for the asynchronous outputs and bi-directionals (BiDI).

*Table 3-20. Asynchronous Type Output Signals*

| Pin | Description | Comment | Pin |
|---|---|---|---|
| ATTENTION | Attention | To service processor | AC7 |
| $\overline{\text{CP0\_QREQ}}$ | Quiesce request | Power management - core 0 | AB9 |
| $\overline{\text{CP1\_QREQ}}$ | Quiesce request | Power management - core 1 | AC21 |
| TRIGGEROUT | | Debug only | R22 |
| **Note:** No reference to SYSCLK because this output is launched by the (internal) core clock. | | | |

*Table 3-21. Asynchronous Open Drain Output Signals*

| Pin | Description | Comment | Pin |
|---|---|---|---|
| I2CGO | I$^2$C interface go | Arbitration I$^2$C and JTAG | E13 |
| **Notes:**<br>The rise/fall times are measured at 20% to 80% of the input signal swing.<br>No reference to SYSCLK because this output is launched by the (internal) core clock.<br>Pull up resistor = TBD (Any value >200 Ohms should ensure a good down level, but it will really depend on loading on the system.) | | | |

*Table 3-22. Asynchronous Open Drain Bidirectional (BiDi) Signals*

| Pin | Description | Comment | Pin |
|---|---|---|---|
| $\overline{\text{CHKSTOP}}$ | Checkstop signal input/output | | T22 |
| **Notes:**<br>No reference to SYSCLK because this output is launched by the (internal) core clock.<br>Pull up resistor = TBD (Any value >200 Ohms should ensure a good down level, but it will really depend on loading on the system.) | | | |

## 3.8 Mode Select Input Timing Specifications

This section provides timing specifications for the mode-select pins. These pins are sampled by $\overline{\text{CP0\_HRESET}}$.

*Table 3-23* provides the input AC timing specifications as defined in *Figure 3-8*. The mode-select signals and debug pins are listed in *Table 3-24* and *Table 3-25* on page 35.

*Table 3-23. Input AC Timing Specifications*

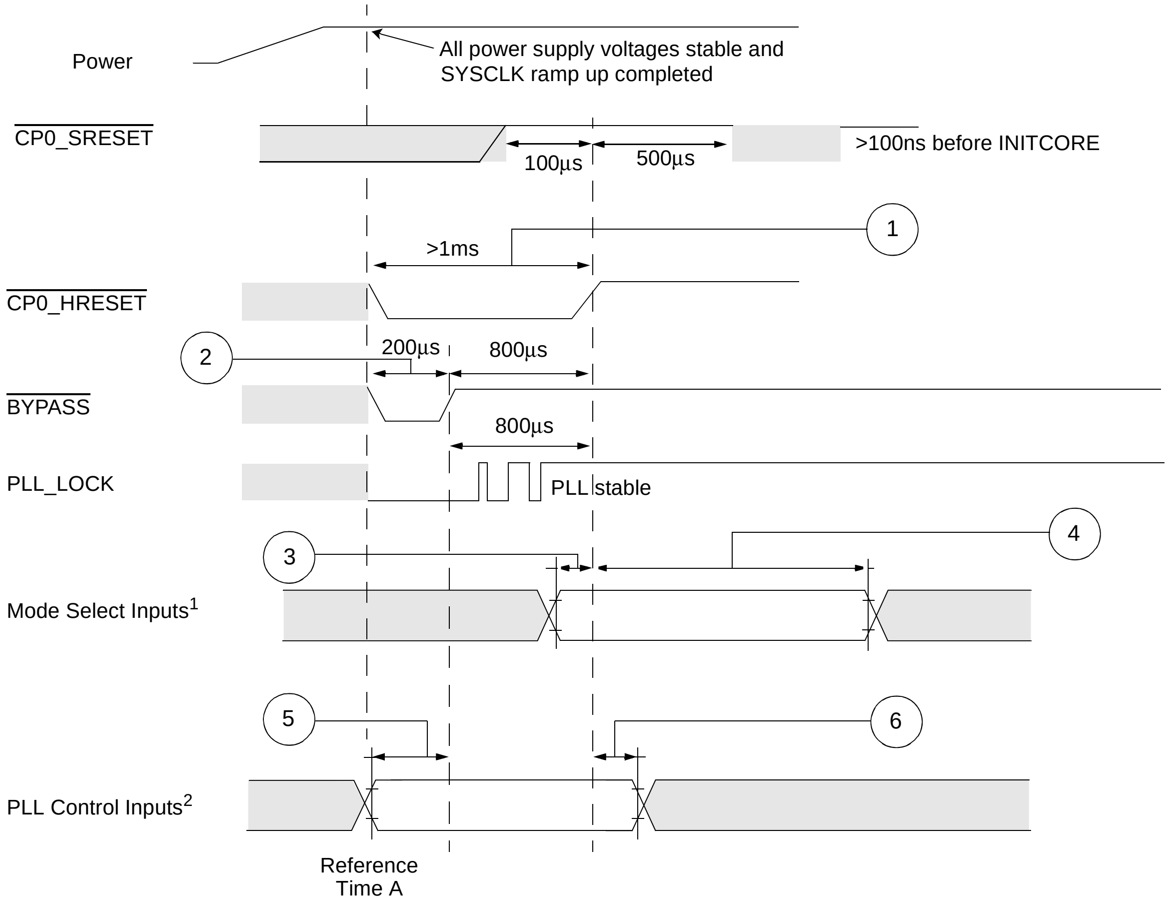
| Call Out Number | Characteristic | Value | | Unit | Notes |
|---|---|---|---|---|---|
| | | Minimum | Maximum | | |
| 1 | $\overline{\text{CP0\_HRESET}}$ Width | >1 | — | ms | 6 |
| 2 | $\overline{\text{BYPASS}}$ Width | 200 | — | µs | — |
| 3 | Mode select signals | 20 | — | Core clocks | 1, 5 |
| 4 | Mode select inputs hold time | 1000 | — | Core clocks | 1 |
| 5 | PLL control signals | 20 | — | Core clocks | 2, 3 |
| 6 | PLL control inputs hold time | 20 | — | Core clocks | 2, 3 |

**Notes:**

1. Mode select pins must not change level sooner than 20 core clocks before the rising edge of $\overline{\text{CP0\_HRESET}}$ and must be held for a minimum of 1000 core clocks after the rising edge of $\overline{\text{CP0\_HRESET}}$.
2. PLL control pins must not change level earlier than 20 core clocks before the rising edge of $\overline{\text{BYPASS}}$ and must be held for a minimum of 20 core clocks after the rising edge of $\overline{\text{CP0\_HRESET}}$.
3. PLL control inputs must not change while $\overline{\text{CP0\_HRESET}}$ is low.
4. For a timing diagram, see *Figure 3-8*.
5. Guaranteed by design and not tested.
6. $\overline{\text{CP0\_HRESET}}$ pulse width covers resetting the PLL ($\overline{\text{BYPASS}}$ Width) + 800 microseconds for the PLL to lock. POR sequence can only start if the PLL is good.

**Note:** For bus timing information, see Section 3.5 Processor Interconnect Specifications on Page 26.

*Figure 3-8. CP0_HRESET and BYPASS Timing Diagram*




**Notes:**

1. These timings refer to the following pins: BUS_CFG(0:2) and PROCID(0:1).
2. These timings refer to the following pins: CKTERM_DIS, PLL_MULT, and PLL_RANGE(1:0).
   These pins may only be changed by driving CP0_HRESET and BYBASS low.
3. CP0_HRESET and BYPASS may be low during initial IPL stages and not have to transition power prior to reference time A.
4. PLL control inputs must not change while CP0_HRESET is low.
5. The legend for this figure is provided in *Table 3-23* on page 33.

*Table 3-24. Mode Select Type Input Signals*

| Pin Name | Pin Location | Description | Comment |
|---|---|---|---|
| BUS_CFG(0:2) | A11, D12, B11 | Bus configuration | Select core clock to bus clock ratio |
| CKTERM_DIS | Y5 | Clock receiver termination | Disables 50Ω parallel SYSCLK termination. Pulled up to $OV_{DD}$ for applications using external termination on SYSCLK and $\overline{\text{SYSCLK}}$. Otherwise, pulled low to GND |
| PLL_MULT | AC5 | Select between multiplier 8 or 12 | |
| PLL_RANGE(1:0) | AD3,AA4 | PLL range select | |
| PROCID(0:1) | N21, N22 | Processor ID | For multi PPC970MP environment |

*Table 3-25. Debug Pins*

| Pin Name | Pin Location | Description | Comment |
|---|---|---|---|
| $\overline{\text{AVP\_RESET}}$ | U24 | | Changes POR sequence |
| EI_DISABLE | B12 | | Disables the use of IAP, Initial Alignment Procedure, to adjust clock skew on the processor interface. |
| GPULDBG | Y24 | PPC970MP POR in debug mode | Refer to the PowerPC 970MP Power On Reset Application Note for additional details |

## 3.9 Spread Spectrum Clock Generator (SSCG)

### 3.9.1 Design Considerations

When designing with the Spread Spectrum Clock Generator (SSCG), there are a several design issues that must be considered as described in this section. SSCG creates a controlled amount of long-term jitter. For a receiving PLL in the PowerPC 970MP to operate in this environment, it must be able to accurately track the SSCG clock jitter.

**Note:** The accuracy to which the PowerPC 970MP PLL can track the SSCG clock is called the *tracking skew*.

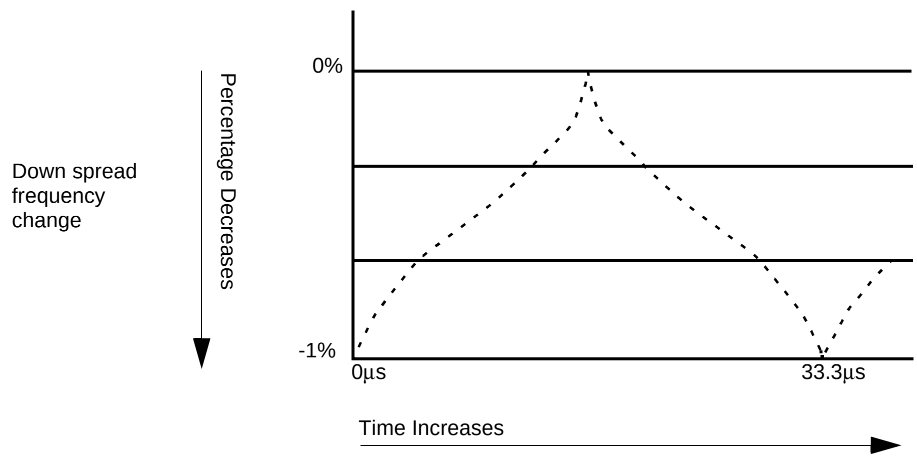
The following SSCG configuration is recommended:

- Down spread mode, less than or equal to 1% of the maximum frequency
- A modulation frequency of 30KHz
- A linear sweep profile, also called a *Hershey Kiss*™[1] profile (as in a Lexmark[2] profile), as shown in *Figure 3-9*.

In this configuration the tracking skew is less than 100ps.

1. Hershey Kiss is a trademark of Hershey Foods Corporation.
2. See patent 5,631,920.

*Figure 3-9.* Spread Spectrum Clock Generator (SSCG) *Modulation Profile*




## 3.10 I2C and JTAG

The single external I2C interface connects to two I2C controllers, one for each processing unit. The controllers are distinguished by the low order address bit, which is 0 for Processing Unit 0 and 1 for Processing Unit 1. Similarly, the single external JTAG interface connects to two daisy chained JTAG controllers, one for each processing unit.

### 3.10.1 I2C Bus Timing Information

The I2C bus specification can be downloaded from Philips Semiconductors web site at http://semiconductors.philips.com.

The PowerPC PPC970MP I2C bus conforms to the standard-mode timing specification and does not support the high-speed (Hs-mode) or fast-mode timing. The default I2C bus speed for the PowerPC PPC970MP is 50kHz. An SCOM write with the I2C bus running at 50kHz is needed to allow the bus to conform to the standard-mode timing specification of 100kHz. Refer to the PowerPC 970MP Power On Reset Application Note for more details.

The PowerPC PPC970MP I2C pins are limited to OVDD voltages. Level shifting and/or pullups may be required to interface to higher voltage devices. To avoid problems, level shifted PPC970MP I2C bus pins must not be wired together with non-PPC970MP parts in a system. The PPC970MP should have its own private level shifter. If one level shifter is used for multiple 970MP microprocessors, the length of the traces must be controlled very carefully. See the Philips $I^2C$ bus specifications for recommendations on level shifting and pullups.

### 3.10.2 IEEE 1149.1 AC Timing Specifications

*Table 3-26* provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in *Figure 3-10. JTAG Clock Input Timing Diagram* and *Figure 3-11. Test Access Port Timing Diagram*. The five JTAG signals are as follows:

1. TDI

2. TDO
3. TMS
4. TCK
5. $\overline{\text{TRST}}$

**Note:** The PowerPC PPC970MP diverges from the standard IEEE AC timing implementation in this regard:

JTAG is normally used with the PLL running, however, it may also be used with the PLL in bypass mode. If the PLL is in bypass mode, clock pulses must be supplied to the SYSCLK and SYSCLK pins at a rate 40 times higher than the TCK rate.

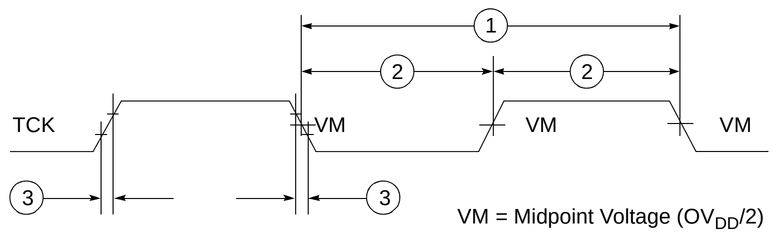
*Table 3-26. JTAG AC Timing Specifications (Dependent on SYSCLK)*

| Call Out Number | Characteristic | Minimum | Maximum | Unit | Notes |
|---|---|---|---|---|---|
| — | TCK frequency of operation | TBD | 1/40 | Core processor frequency | 1, 5 |
| 1 | TCK cycle time | 40 | — | Core clocks | 2, 5 |
| 2 | TCK clock pulse width | 20 | — | Core clocks | 2, 5 |
| 3 | TCK rise and fall times | 0 | 2 | ns | 3, 5 |
| 4 | TMS, TDI data setup time | 0 | — | ns | 5 |
| 5 | TMS, TDI data hold time | 15 | — | ns | 5 |
| 6 | TCK to TDO data valid | 2.5 | 12 | ns | 4, 5 |
| 7 | TCK to TDO high impedance | 3 | 9 | ns | 3, 5 |
| 8 | TCK to output data invalid (output hold) | 0 | — | ns | 5 |

**Notes:**

1. TCK frequency is limited by the core processor frequency.
2. Core clock cycles.
3. Guaranteed by characterization and not tested.
4. Minimum specification guaranteed by characterization and not tested.
5. JTAG timings are dependent on an active SYSCLK.
6. For a timing diagram, see *Figure 3-10. JTAG Clock Input Timing Diagram* and *Figure 3-11. Test Access Port Timing Diagram*.

*Figure 3-10. JTAG Clock Input Timing Diagram*

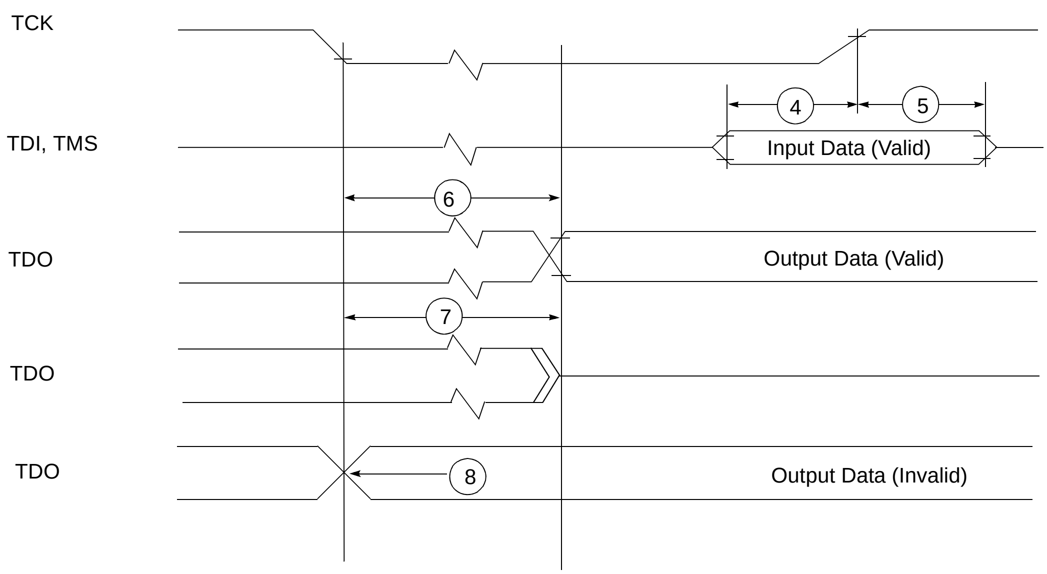



VM = Midpoint Voltage ($OV_{DD}/2$)

**Note:** The legend for this figure is provided in *Table 3-26 JTAG AC Timing Specifications (Dependent on SYSCLK)*.

*Figure 3-11 provides the test access port timing diagram.*

*Figure 3-11. Test Access Port Timing Diagram*




**Note:** The legend for this figure is provided in *Table 3-26 JTAG AC Timing Specifications (Dependent on SYSCLK)*.

### 3.10.3 I2C and JTAG Considerations

The PowerPC PPC970MP supports $I^2C$ and JTAG. The $I^2C$ data and clock pins as well as the TCK, TMS, TDO, and $\overline{TRST}$ pins should be pulled up to $OV_{DD}$. Use of the $I^2C$ or JTAG bus is mutually exclusive and controlled by the I2CSEL pin. If this pin is high, the $I^2C$ bus can be used. If the pin is low, the JTAG bus can be used. Traffic on the non-selected bus ($I^2C$ or JTAG depending on I2CSEL) is ignored and should not have any side effect.

#### 3.9.3.1 Guidance for Using Both $I^2C$ and JTAG

If a concurrent use of both interfaces is required, then the I2CSEL pin may be switched while the system is running. For correct operation, it is recommended to switch the I2CSEL pin only while no traffic is active on either interface to prevent misrecognition of a partial transmission. To ease this operation in debug mode (GPULDBG=1), the I2CGO pin may be monitored or directly connected to the I2CSEL pin. This pin will switch from 0 to 1 whenever it is safe to switch I2CSEL from 0 to 1 for $I^2C$ usage. Similarly, it will switch from 1 to 0 whenever it is safe to switch I2CSEL from 1 to 0 for JTAG usage. See the PowerPC 970MP Power On Reset Application Note for a description of how the I2CGO pin is controlled by software.

### 3.10.4 Boundary Scan Considerations

The PowerPC PPC970MP does not support the BSDL standard for implementing boundary scan testing. Boundary scan patterns are available for customer use, but require other signals to be controlled in addition to the JTAG port. Boundary scan testing requires an input clock (SYSCLK/SYSCLK) and control of CP0_HRESET. Details of how to do boundary scan testing on the PPC970MP can be found in the PowerPC 970MP Boundary Scan Application Note

# 4. PowerPC 970MP Microprocessor Dimension and Physical Signal Assignments

IBM offers a ceramic ball grid array, CBGA, which supports 575 balls as the PowerPC PPC970MP package. The PPC970MP is offered in a lead reduced package with SnAgCu (SAC) balls.

The following sections contain several views of the package, pin information, and a pin listing. *Figure 4-1* shows the side and top views of the package including the height from the top of the die to the bottom of the solder balls. *Figure 4-2* shows a bottom view of the PowerPC 970MP.

**Note:** All lead free or lead reduced BGA modules are classified as JEDEC Moisture Sensitive Level 3.Appropriate ESD handling procedures should be implemented and maintained for any facilities handling this component.

## 4.1 ESD Considerations

**Note:** Appropriate ESD handling procedures should be implemented and maintained for any facilities handling this component.

This product has been ESD tested to meet or exceed the JEDEC spec for .:

- HBM - Class 1B
- CDM - Class II
- MM - Class A

## 4.2 Mechanical Packaging

*Figure 4-1* shows the side and top views of the packages including the height from the top of the die to the bottom of the solder balls. *Figure 4-2* shows a bottom view of the PowerPC 970MP.

### 4.2.1 Reduced-Lead Package Version

This section describes the reduced-lead package, as indicated by the 'R' in the Package code field of the part number. For the reduced lead package, lead-free solder is used for the substrate capacitors and the BGA balls on the bottom of the package. Standard high melting point 97Pb3Sn solder (exempted by EU RoHS legislation) is used for the C4 balls that connect the die to the substrate. The resulting module is RoHS compatible.

All Datasheet electrical specifications apply equally to standard and reduced-lead parts.

#### *4.2.1.1 Mechanical Specifications*

The solder balls on the bottom of the reduced-lead package are slightly smaller, which will decrease the overall module height when assembled onto a board. Heatsink solutions should be modified accordingly

.

*Table 4-1. Leaded and Reduced-Lead Package, Layout, and Assembly Differences*

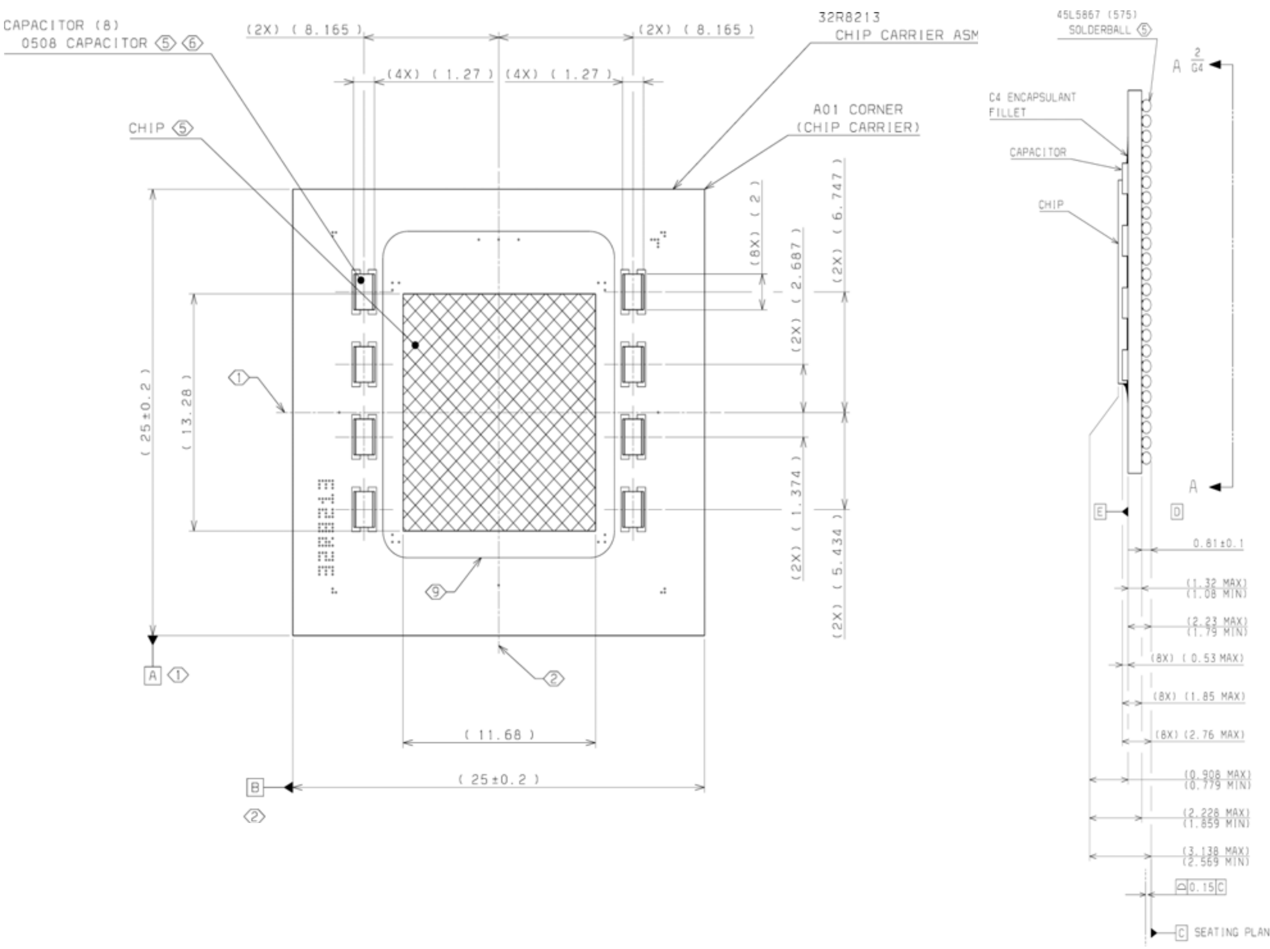
| Package | JEDEC MSL | Solder Ball Composition | Solder Ball Diameter | CBGA Substrate I/O Pad Diameter | Card Solder Mask Open-ing Diameter | Card Solder Screen Diameter | Card Pad Diameter |
|---|---|---|---|---|---|---|---|
| Leaded | 1 | Sn 10% Pb 90% | 31.5 (0.80) | 31.5 (0.80) | 31.5 (0.80) | 26.5mil open-ing in 7.5mil thick stencil, 2500-4600 cubic mils | 27.5 (0.70) |
| Reduced Lead | 3 | Sn 95.5% Ag 3.8% Cu 0.7% | 25 (0.635) | 31.5 (0.80) | 28 (0.72) | 23mil opening in 4mil thick stencil, 1400-2000 cubic mils | 24 (0.61) |
| **Note:** All dimensions in mils unless noted. Dimensions in parenthesis are in mm. | | | | | | | |

#### *4.2.1.2 Assembly Considerations*

The reduced-lead package is compatible with a 260C lead-free card assembly reflow profile. Refer to the INEMI Consortium, www.inemi.org, for industry-standard assembly and rework information. The coplanarity specification for the reduced-lead CBGA, like other single melt BGA packages, is 0.20 mm (8mil). The qualification testing included a lead-free water soluble solder paste with type 3 mesh size (-325/+500). The solder alloy is 95.5% Sn, 4.0% Ag, and 0.5% Cu, with a 90% metal loading. The paste viscosity range is 600 to 800 Kcps. The thickness of the stencil is 4 mils and the aperture size is 23 mil diameter. The target solder paste volume range is between 1400 to 2000 cubic mils. Achieving the correct paste volume is necessary for eliminating solder shorts and producing high reliability solder joints. The actual solder paste volume from the qualification build ranged from 1750 to 2000 cubic mils.

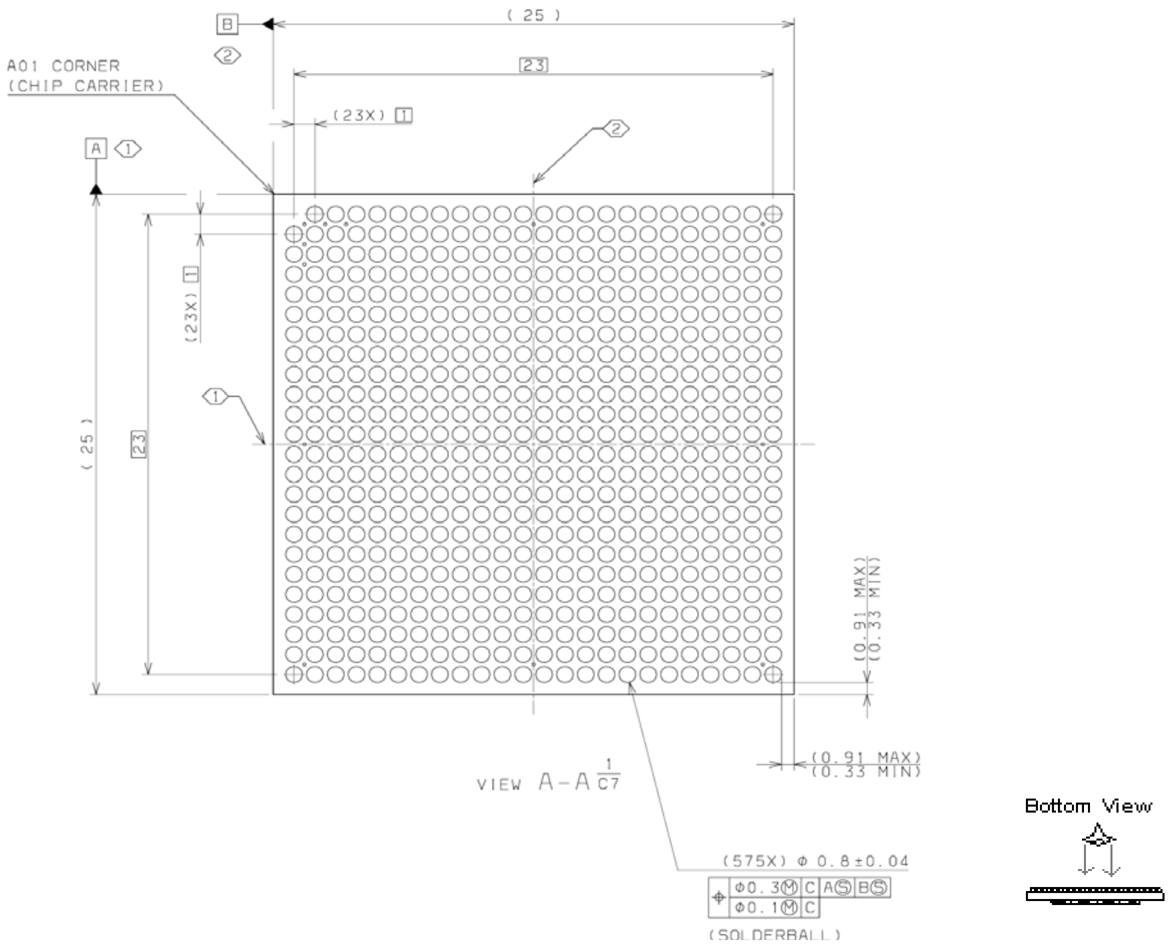
Another change is the JEDEC Moisture Sensitivity Level, which is MSL 3 for the reduced-lead package. Storage and assembly protocols should be modified accordingly.

*Figure 4-1. PowerPC 970MP Mechanical Package (Side and Top View) (Preliminary)*




| Legend | |
|---|---|
| 1 | DATUM A is the center plane of feature labeled DATUM A. |
| 2 | DATUM B is the center plane of feature labeled DATUM B. |
| 3 | Unless otherwise specified part is symmetrical about centerlines defined by DATUMs A and B. |
| 4 | Where not otherwise defined, centerlines indicated are to be interpreted as a datum frame work, established by DATUM D, A, and B respectively. |
| 9 | This line defines the approximate boundary configuration of encapsulant as dispensed. |
| 10 | The chip’s assembled height (which include silicon thickness and melted C4) for 300mm wafers is: 0.829mm - 0.908mm The 300mm silicon thickness is 0.785mm +/- 0.020mm |

*Figure 4-2. PowerPC 970MP Bottom Surface of CBGA Package (Bottom View) (Preliminary)*




| Legend | |
|---|---|
| 1 | DATUM A is the center plane of feature labeled DATUM A. |
| 2 | DATUM B is the center plane of feature labeled DATUM B. |
| 3 | Unless otherwise specified part is symmetrical about centerlines defined by DATUMs A and B. |
| 4 | Where not otherwise defined, centerlines indicated are to be interpreted as a datum frame work, established by DATUM D, A, and B respectively. |
| 9 | This line defines the approximate boundary configuration of encapsulant as dispensed. |
| 10 | The chip's assembled height (which include silicon thickness and melted C4) for 300mm wafers is: 0.829mm - 0.908mm The 300mm silicon thickness is 0.785mm +/- 0.020mm |

## *Table 4-2. PowerPC 970MP Ball Placement (Top View)*

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD24 $\overline{\text{BI\_MODE}}$ | AD23 GND | AD22 TMS | AD21 $\overline{\text{CP0\_QACK}}$ | AD20 $\overline{\text{CP1\_INT}}$ | AD19 GND | AD18 $\overline{\text{CP1\_QACK}}$ | AD17 CP1_FRED_EN | AD16 GND | AD15 TBEN | AD14 GND | AD13 V1 | AD12 GND | AD11 V0 | AD10 PULSE_SEL2 | AD9 V0 | AD8 TDO | AD7 V0 | AD6 SPARE1 | AD5 GND | AD4 $OV_{DD}$ | AD3 PLL_RANGE1 | AD2 GND | AD1 $OV_{DD}$ | **AD** |
| AC24 CP1_DIODE_NEG | AC23 $OV_{DD}$ | AC22 GND | AC21 $\overline{\text{CP1\_QREQ}}$ | AC20 $OV_{DD}$ | AC19 V1 | AC18 GND | AC17 $OV_{DD}$ | AC16 $\overline{\text{CP1\_HRESET}}$ | AC15 V1 | AC14 LSSD_STOP_ENABLE | AC13 $OV_{DD}$ | AC12 CP0_FRED_GND | AC11 GND | AC10 GND | AC9 $OV_{DD}$ | AC8 GND | AC7 ATTENTION | AC6 V0 | AC5 PLL_MULT | AC4 V0 | AC3 SPARE2 | AC2 $OV_{DD}$ | AC1 GND | **AC** |
| AB24 CP1_DIODE_POS | AB23 TCK | AB22 $\overline{\text{CP1\_SRESET}}$ | AB21 V1 | AB20 V1 | AB19 GND | AB18 V1 | AB17 C1_UND_GLOBAL | AB16 V1 | AB15 C2_UND_GLOBAL | AB14 V1 | AB13 $\overline{\text{CP0\_INT}}$ | AB12 V1 | AB11 LSSD_STOPC2_ENABLE | AB10 V0 | AB9 $\overline{\text{CP0\_QREQ}}$ | AB8 $OV_{DD}$ | AB7 $\overline{\text{CP0\_SRESET}}$ | AB6 V0 | AB5 GND | AB4 CP0_KELV_V0 | AB3 V0 | AB2 GND | AB1 $OV_{DD}$ | **AB** |
| AA24 GND | AA23 TDI | AA22 V1 | AA21 $\overline{\text{MCP}}$ | AA20 GND | AA19 V1 | AA18 GND | AA17 V1 | AA16 GND | AA15 V1 | AA14 GND | AA13 $\overline{\text{TRST}}$ | AA12 GND | AA11 V0 | AA10 GND | AA9 $\overline{\text{CP0\_HRESET}}$ | AA8 GND | AA7 V0 | AA6 GND | AA5 V0 | AA4 PLL_RANGE0 | AA3 V0 | AA2 GND | AA1 GND | **AA** |
| Y24 GPULDBG | Y23 V1 | Y22 GND | Y21 PSRO_ENABLE | Y20 V1 | Y19 GND | Y18 V1 | Y17 GND | Y16 V1 | Y15 GND | Y14 V1 | Y13 GND | Y12 CP1_FRED_GND | Y11 CP0_FRED_EN | Y10 $OV_{DD}$ | Y9 GND | Y8 V0 | Y7 GND | Y6 V0 | Y5 CKTERM_DIS | Y4 CP0_DIODE_NEG | Y3 CP0_DIODE_POS | Y2 V0 | Y1 $OV_{DD}$ | **Y** |
| W24 $\overline{\text{SYNC\_ENABLE}}$ | W23 $OV_{DD}$ | W22 CP1_KELV_GND1 | W21 CP1_KELV_V1 | W20 GND | W19 V1 | W18 GND | W17 V1 | W16 GND | W15 V1 | W14 $OV_{DD}$ | W13 V0 | W12 GND | W11 $OV_{DD}$ | W10 GND | W9 V0 | W8 GND | W7 V0 | W6 GND | W5 V0 | W4 $\overline{\text{RI}}$ | W3 GND | W2 CP0_KELV_GND0 | W1 GND | **W** |
| V24 $\overline{\text{I2CCK}}$ | V23 GND | V22 $\overline{\text{I2CDT}}$ | V21 GND | V20 V1 | V19 GND | V18 V1 | V17 GND | V16 V1 | V15 GND | V14 V1 | V13 GND | V12 V0 | V11 GND | V10 V0 | V9 GND | V8 V0 | V7 GND | V6 V0 | V5 GND | V4 V0 | V3 CP0_PSRO0 | V2 V0 | V1 PULSE_SEL0 | **V** |
| U24 $\overline{\text{AVP\_RESET}}$ | U23 PLLLOCK | U22 LSSD_SCAN_ENABLE | U21 V1 | U20 GND | U19 V1 | U18 GND | U17 V1 | U16 GND | U15 V1 | U14 GND | U13 V1 | U12 GND | U11 V0 | U10 GND | U9 V0 | U8 GND | U7 V0 | U6 GND | U5 V0 | U4 GND | U3 LSSD_STOP_C2STAR_ENABLE | U2 LSSDMODE | U1 I2CSEL | **U** |
| T24 $\overline{\text{BYPASS}}$ | T23 $OV_{DD}$ | T22 $\overline{\text{CHKSTOP}}$ | T21 GND | T20 V1 | T19 GND | T18 V1 | T17 GND | T16 V1 | T15 GND | T14 V1 | T13 GND | T12 V0 | T11 GND | T10 V0 | T9 GND | T8 V0 | T7 GND | T6 V0 | T5 GND | T4 V0 | T3 PULSE_SEL1 | T2 LSSD_RAMSTOP_ENABLE | T1 V0 | **T** |
| R24 $\overline{\text{DI2}}$ | R23 GND | R22 TRIGGEROUT | R21 V1 | R20 GND | R19 V1 | R18 GND | R17 V1 | R16 GND | R15 V1 | R14 GND | R13 V1 | R12 GND | R11 V0 | R10 GND | R9 V0 | R8 GND | R7 V0 | R6 GND | R5 V0 | R4 GND | R3 V0 | R2 MASTERSEL | R1 GND | **R** |
| P24 GND | P23 GND | P22 V1 | P21 GND | P20 V1 | P19 GND | P18 V1 | P17 GND | P16 V1 | P15 GND | P14 V1 | P13 GND | P12 V0 | P11 GND | P10 V0 | P9 GND | P8 V0 | P7 GND | P6 V0 | P5 GND | P4 PSYNC | P3 Z_OUT | P2 GND | P1 Z_SENSE | **P** |
| N24 SRIN0 | N23 V1 | N22 PROCID1 | N21 PROCID0 | N20 GND | N19 V1 | N18 GND | N17 V1 | N16 GND | N15 V1 | N14 GND | N13 V1 | N12 GND | N11 V0 | N10 GND | N9 V0 | N8 GND | N7 V0 | N6 GND | N5 V0 | N4 GND | N3 GND | N2 ADOUT0 | N1 $OV_{DD}$ | **N** |
| M24 $\overline{\text{SRIN0}}$ | M23 $OV_{DD}$ | M22 V1 | M21 GND | M20 V1 | M19 GND | M18 V1 | M17 GND | M16 V1 | M15 GND | M14 V1 | M13 GND | M12 V0 | M11 GND | M10 V0 | M9 GND | M8 V0 | M7 GND | M6 V0 | M5 GND | M4 V0 | M3 $OV_{DD}$ | M2 ADOUT4 | M1 SROUT0 | **M** |
| L24 ADIN8 | L23 $\overline{\text{SRIN1}}$ | L22 GND | L21 V1 | L20 V1 | L19 V1 | L18 GND | L17 V1 | L16 GND | L15 V1 | L14 GND | L13 V1 | L12 GND | L11 V0 | L10 GND | L9 V0 | L8 GND | L7 V0 | L6 GND | L5 V0 | L4 $OV_{DD}$ | L3 GND | L2 ADOUT3 | L1 $\overline{\text{SROUT0}}$ | **L** |
| K24 GND | K23 SRIN1 | K22 ADIN6 | K21 GND | K20 $OV_{DD}$ | K19 GND | K18 V1 | K17 GND | K16 V1 | K15 GND | K14 V1 | K13 GND | K12 V0 | K11 GND | K10 V0 | K9 GND | K8 V0 | K7 GND | K6 V0 | K5 $OV_{DD}$ | K4 GND | K3 ADOUT5 | K2 ADOUT6 | K1 GND | **K** |
| J24 ADIN2 | J23 ADIN7 | J22 GND | J21 $OV_{DD}$ | J20 GND | J19 V1 | J18 GND | J17 V1 | J16 GND | J15 V1 | J14 GND | J13 V0 | J12 GND | J11 V0 | J10 GND | J9 V0 | J8 GND | J7 V0 | J6 GND | J5 V0 | J4 GND | J3 $OV_{DD}$ | J2 ADOUT2 | J1 ADOUT8 | **J** |
| H24 $OV_{DD}$ | H23 ADIN0 | H22 ADIN3 | H21 GND | H20 V0 | H19 GND | H18 V1 | H17 GND | H16 V1 | H15 GND | H14 V1 | H13 GND | H12 V0 | H11 GND | H10 V0 | H9 GND | H8 V0 | H7 GND | H6 V0 | H5 $OV_{DD}$ | H4 GND | H3 ADOUT7 | H2 GND | H1 SROUT1 | **H** |
| G24 ADIN13 | G23 ADIN1 | G22 V1 | G21 V0 | G20 $OV_{DD}$ | G19 V1 | G18 GND | G17 V1 | G16 GND | G15 V1 | G14 $OV_{DD}$ | G13 V0 | G12 GND | G11 V0 | G10 GND | G9 V0 | G8 GND | G7 V0 | G6 GND | G5 GND | G4 GND | G3 ADOUT1 | G2 GND | G1 $\overline{\text{SROUT1}}$ | **G** |
| F24 GND | F23 ADIN14 | F22 $OV_{DD}$ | F21 GND | F20 GND | F19 $OV_{DD}$ | F18 V0 | F17 V1 | F16 $OV_{DD}$ | F15 GND | F14 V0 | F13 GND | F12 SYSCLK | F11 GND | F10 V0 | F9 $OV_{DD}$ | F8 V0 | F7 GND | F6 $OV_{DD}$ | F5 V0 | F4 $OV_{DD}$ | F3 ADOUT13 | F2 $OV_{DD}$ | F1 ADOUT10 | **F** |
| E24 ADIN11 | E23 GND | E22 ADIN9 | E21 ADIN21 | E20 ADIN31 | E19 ADIN32 | E18 GND | E17 ADIN30 | E16 ADIN29 | E15 ADIN18 | E14 $OV_{DD}$ | E13 I2CGO | E12 $\overline{\text{SYSCLK}}$ | E11 $OV_{DD}$ | E10 ADOUT15 | E9 ADOUT18 | E8 ADOUT39 | E7 ADOUT23 | E6 $OV_{DD}$ | E5 ADOUT21 | E4 ADOUT32 | E3 ADOUT9 | E2 GND | E1 ADOUT12 | **E** |
| D24 $OV_{DD}$ | D23 ADIN10 | D22 $OV_{DD}$ | D21 ADIN23 | D20 GND | D19 $OV_{DD}$ | D18 ADIN27 | D17 ADIN35 | D16 $OV_{DD}$ | D15 ADIN15 | D14 GND | D13 PLLTEST | D12 BUS_CFG1 | D11 GND | D10 ADOUT16 | D9 ADOUT41 | D8 $OV_{DD}$ | D7 ADOUT35 | D6 ADOUT36 | D5 GND | D4 ADOUT31 | D3 ADOUT11 | D2 CLKOUT | D1 $\overline{\text{CLKOUT}}$ | **D** |
| C24 CLKIN | C23 GND | C22 ADIN22 | C21 ADIN20 | C20 ADIN33 | C19 ADIN34 | C18 ADIN43 | C17 ADIN42 | C16 ADIN19 | C15 ADIN40 | C14 ADIN28 | C13 $OV_{DD}$ | C12 PLLTESTOUT | C11 $OV_{DD}$ | C10 ADOUT28 | C9 ADOUT40 | C8 GND | C7 ADOUT14 | C6 ADOUT27 | C5 ADOUT33 | C4 $OV_{DD}$ | C3 ADOUT25 | C2 $OV_{DD}$ | C1 ADOUT26 | **C** |
| B24 $\overline{\text{CLKIN}}$ | B23 ADIN25 | B22 ADIN24 | B21 $OV_{DD}$ | B20 ADIN36 | B19 $OV_{DD}$ | B18 ADIN39 | B17 GND | B16 $OV_{DD}$ | B15 ADIN16 | B14 ADIN4 | B13 KELV_GND2 | B12 EI_DISABLE | B11 BUS_CFG2 | B10 GND | B9 ADOUT17 | B8 ADOUT19 | B7 $OV_{DD}$ | B6 ADOUT43 | B5 ADOUT30 | B4 ADOUT37 | B3 GND | B2 ADOUT20 | B1 GND | **B** |
| A24 $OV_{DD}$ | A23 ADIN12 | A22 GND | A21 ADIN37 | A20 GND | A19 ADIN38 | A18 ADIN26 | A17 ADIN41 | A16 ADIN17 | A15 ADIN5 | A14 GND | A13 ANALOGGND | A12 AVDD | A11 BUS_CFG0 | A10 KELV_OVDD | A9 ADOUT29 | A8 ADOUT38 | A7 ADOUT42 | A6 ADOUT34 | A5 GND | A4 ADOUT24 | A3 $OV_{DD}$ | A2 ADOUT22 | | **A** |
| **24** | **23** | **22** | **21** | **20** | **19** | **18** | **17** | **16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | |

## *Table 4-3. PowerPC 970MP Ball Placement (Bottom View)*

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **AD** | AD1 $OV_{DD}$ | AD2 GND | AD3 PLL_RANGE1 | AD4 $OV_{DD}$ | AD5 GND | AD6 SPARE1 | AD7 V0 | AD8 TDO | AD9 V0 | AD10 PULSE_SEL2 | AD11 V0 | AD12 GND | AD13 V1 | AD14 GND | AD15 TBEN | AD16 GND | AD17 CP1_FRED_EN | AD18 $\overline{\text{CP1\_QACK}}$ | AD19 GND | AD20 $\overline{\text{CP1\_INT}}$ | AD21 $\overline{\text{CP0\_QACK}}$ | AD22 TMS | AD23 GND | AD24 $\overline{\text{BI\_MODE}}$ |
| **AC** | AC1 GND | AC2 $OV_{DD}$ | AC3 SPARE2 | AC4 V0 | AC5 PLL_MULT | AC6 V0 | AC7 ATTENTION | AC8 GND | AC9 $OV_{DD}$ | AC10 GND | AC11 GND | AC12 CP0_FRED_GND | AC13 $OV_{DD}$ | AC14 LSSD_STOP_ENABLE | AC15 V1 | AC16 $\overline{\text{CP1\_HRESET}}$ | AC17 $OV_{DD}$ | AC18 GND | AC19 V1 | AC20 $OV_{DD}$ | AC21 $\overline{\text{CP1\_QREQ}}$ | AC22 GND | AC23 $OV_{DD}$ | AC24 CP1_DIODE_NEG |
| **AB** | AB1 $OV_{DD}$ | AB2 GND | AB3 V0 | AB4 CP0_KELV_V0 | AB5 GND | AB6 V0 | AB7 $\overline{\text{CP0\_SRESET}}$ | AB8 $OV_{DD}$ | AB9 $\overline{\text{CP0\_QREQ}}$ | AB10 V0 | AB11 LSSD_STOPC2_ENABLE | AB12 V1 | AB13 $\overline{\text{CP0\_INT}}$ | AB14 V1 | AB15 C2_UND_GLOBAL | AB16 V1 | AB17 C1_UND_GLOBAL | AB18 V1 | AB19 GND | AB20 V1 | AB21 V1 | AB22 $\overline{\text{CP1\_SRESET}}$ | AB23 TCK | AB24 CP1_DIODE_POS |
| **AA** | AA1 GND | AA2 GND | AA3 V0 | AA4 PLL_RANGE0 | AA5 V0 | AA6 GND | AA7 V0 | AA8 GND | AA9 $\overline{\text{CP0\_HRESET}}$ | AA10 GND | AA11 V0 | AA12 GND | AA13 $\overline{\text{TRST}}$ | AA14 GND | AA15 V1 | AA16 GND | AA17 V1 | AA18 GND | AA19 V1 | AA20 GND | AA21 $\overline{\text{MCP}}$ | AA22 V1 | AA23 TDI | AA24 GND |
| **Y** | Y1 $OV_{DD}$ | Y2 V0 | Y3 CP0_DIODE_POS | Y4 CP0_DIODE_NEG | Y5 CKTERM_DIS | Y6 V0 | Y7 GND | Y8 V0 | Y9 GND | Y10 $OV_{DD}$ | Y11 CP0_FRED_EN | Y12 CP1_FRED_GND | Y13 GND | Y14 V1 | Y15 GND | Y16 V1 | Y17 GND | Y18 V1 | Y19 GND | Y20 V1 | Y21 PSRO_ENABLE | Y22 GND | Y23 V1 | Y24 GPULDBG |
| **W** | W1 GND | W2 CP0_KELV_GND0 | W3 GND | W4 $\overline{\text{RI}}$ | W5 V0 | W6 GND | W7 V0 | W8 GND | W9 V0 | W10 GND | W11 $OV_{DD}$ | W12 GND | W13 V0 | W14 $OV_{DD}$ | W15 V1 | W16 GND | W17 V1 | W18 GND | W19 V1 | W20 GND | W21 CP1_KELV_V1 | W22 CP1_KELV_GND1 | W23 $OV_{DD}$ | W24 $\overline{\text{SYNC\_ENABLE}}$ |
| **V** | V1 PULSE_SEL0 | V2 V0 | V3 CP0_PSRO0 | V4 V0 | V5 GND | V6 V0 | V7 GND | V8 V0 | V9 GND | V10 V0 | V11 GND | V12 V0 | V13 GND | V14 V1 | V15 GND | V16 V1 | V17 GND | V18 V1 | V19 GND | V20 V1 | V21 GND | V22 $\overline{\text{I2CDT}}$ | V23 GND | V24 $\overline{\text{I2CCK}}$ |
| **U** | U1 I2CSEL | U2 LSSDMODE | U3 LSSD_STOP_C2STAR_ENABLE | U4 GND | U5 V0 | U6 GND | U7 V0 | U8 GND | U9 V0 | U10 GND | U11 V0 | U12 GND | U13 V1 | U14 GND | U15 V1 | U16 GND | U17 V1 | U18 GND | U19 V1 | U20 GND | U21 V1 | U22 LSSD_SCAN_ENABLE | U23 PLLLOCK | U24 $\overline{\text{AVP\_RESET}}$ |
| **T** | T1 V0 | T2 LSSD_RAMSTOP_ENABLE | T3 PULSE_SEL1 | T4 V0 | T5 GND | T6 V0 | T7 GND | T8 V0 | T9 GND | T10 V0 | T11 GND | T12 V0 | T13 GND | T14 V1 | T15 GND | T16 V1 | T17 GND | T18 V1 | T19 GND | T20 V1 | T21 GND | T22 $\overline{\text{CHKSTOP}}$ | T23 $OV_{DD}$ | T24 $\overline{\text{BYPASS}}$ |
| **R** | R1 GND | R2 MASTERSEL | R3 V0 | R4 GND | R5 V0 | R6 GND | R7 V0 | R8 GND | R9 V0 | R10 GND | R11 V0 | R12 GND | R13 V1 | R14 GND | R15 V1 | R16 GND | R17 V1 | R18 GND | R19 V1 | R20 GND | R21 V1 | R22 TRIGGEROUT | R23 GND | R24 $\overline{\text{DI2}}$ |
| **P** | P1 Z_SENSE | P2 GND | P3 Z_OUT | P4 PSYNC | P5 GND | P6 V0 | P7 GND | P8 V0 | P9 GND | P10 V0 | P11 GND | P12 V0 | P13 GND | P14 V1 | P15 GND | P16 V1 | P17 GND | P18 V1 | P19 GND | P20 V1 | P21 GND | P22 V1 | P23 GND | P24 GND |
| **N** | N1 $OV_{DD}$ | N2 ADOUT0 | N3 GND | N4 GND | N5 V0 | N6 GND | N7 V0 | N8 GND | N9 V0 | N10 GND | N11 V0 | N12 GND | N13 V1 | N14 GND | N15 V1 | N16 GND | N17 V1 | N18 GND | N19 V1 | N20 GND | N21 PROCID0 | N22 PROCID1 | N23 V1 | N24 SRIN0 |
| **M** | M1 SROUT0 | M2 ADOUT4 | M3 $OV_{DD}$ | M4 V0 | M5 GND | M6 V0 | M7 GND | M8 V0 | M9 GND | M10 V0 | M11 GND | M12 V0 | M13 GND | M14 V1 | M15 GND | M16 V1 | M17 GND | M18 V1 | M19 GND | M20 V1 | M21 GND | M22 V1 | M23 $OV_{DD}$ | M24 $\overline{\text{SRIN0}}$ |
| **L** | L1 $\overline{\text{SROUT0}}$ | L2 ADOUT3 | L3 GND | L4 $OV_{DD}$ | L5 V0 | L6 GND | L7 V0 | L8 GND | L9 V0 | L10 GND | L11 V0 | L12 GND | L13 V1 | L14 GND | L15 V1 | L16 GND | L17 V1 | L18 GND | L19 V1 | L20 V1 | L21 V1 | L22 GND | L23 $\overline{\text{SRIN1}}$ | L24 ADIN8 |
| **K** | K1 GND | K2 ADOUT6 | K3 ADOUT5 | K4 GND | K5 $OV_{DD}$ | K6 V0 | K7 GND | K8 V0 | K9 GND | K10 V0 | K11 GND | K12 V0 | K13 GND | K14 V1 | K15 GND | K16 V1 | K17 GND | K18 V1 | K19 GND | K20 $OV_{DD}$ | K21 GND | K22 ADIN6 | K23 SRIN1 | K24 GND |
| **J** | J1 ADOUT8 | J2 ADOUT2 | J3 $OV_{DD}$ | J4 GND | J5 V0 | J6 GND | J7 V0 | J8 GND | J9 V0 | J10 GND | J11 V0 | J12 GND | J13 V0 | J14 GND | J15 V1 | J16 GND | J17 V1 | J18 GND | J19 V1 | J20 GND | J21 $OV_{DD}$ | J22 GND | J23 ADIN7 | J24 ADIN2 |
| **H** | H1 SROUT1 | H2 GND | H3 ADOUT7 | H4 GND | H5 $OV_{DD}$ | H6 V0 | H7 GND | H8 V0 | H9 GND | H10 V0 | H11 GND | H12 V0 | H13 GND | H14 V1 | H15 GND | H16 V1 | H17 GND | H18 V1 | H19 GND | H20 V0 | H21 GND | H22 ADIN3 | H23 ADIN0 | H24 $OV_{DD}$ |
| **G** | G1 $\overline{\text{SROUT1}}$ | G2 GND | G3 ADOUT1 | G4 GND | G5 GND | G6 GND | G7 V0 | G8 GND | G9 V0 | G10 GND | G11 V0 | G12 GND | G13 V0 | G14 $OV_{DD}$ | G15 V1 | G16 GND | G17 V1 | G18 GND | G19 V1 | G20 $OV_{DD}$ | G21 V0 | G22 V1 | G23 ADIN1 | G24 ADIN13 |
| **F** | F1 ADOUT10 | F2 $OV_{DD}$ | F3 ADOUT13 | F4 $OV_{DD}$ | F5 V0 | F6 $OV_{DD}$ | F7 GND | F8 V0 | F9 $OV_{DD}$ | F10 V0 | F11 GND | F12 SYSCLK | F13 GND | F14 V0 | F15 GND | F16 $OV_{DD}$ | F17 V1 | F18 V0 | F19 $OV_{DD}$ | F20 GND | F21 GND | F22 $OV_{DD}$ | F23 ADIN14 | F24 GND |
| **E** | E1 ADOUT12 | E2 GND | E3 ADOUT9 | E4 ADOUT32 | E5 ADOUT21 | E6 $OV_{DD}$ | E7 ADOUT23 | E8 ADOUT39 | E9 ADOUT18 | E10 ADOUT15 | E11 $OV_{DD}$ | E12 $\overline{\text{SYSCLK}}$ | E13 I2CGO | E14 $OV_{DD}$ | E15 ADIN18 | E16 ADIN29 | E17 ADIN30 | E18 GND | E19 ADIN32 | E20 ADIN31 | E21 ADIN21 | E22 ADIN9 | E23 GND | E24 ADIN11 |
| **D** | D1 $\overline{\text{CLKOUT}}$ | D2 CLKOUT | D3 ADOUT11 | D4 ADOUT31 | D5 GND | D6 ADOUT36 | D7 ADOUT35 | D8 $OV_{DD}$ | D9 ADOUT41 | D10 ADOUT16 | D11 GND | D12 BUS_CFG1 | D13 PLLTEST | D14 GND | D15 ADIN15 | D16 $OV_{DD}$ | D17 ADIN35 | D18 ADIN27 | D19 $OV_{DD}$ | D20 GND | D21 ADIN23 | D22 $OV_{DD}$ | D23 ADIN10 | D24 $OV_{DD}$ |
| **C** | C1 ADOUT26 | C2 $OV_{DD}$ | C3 ADOUT25 | C4 $OV_{DD}$ | C5 ADOUT33 | C6 ADOUT27 | C7 ADOUT14 | C8 GND | C9 ADOUT40 | C10 ADOUT28 | C11 $OV_{DD}$ | C12 PLLTESTOUT | C13 $OV_{DD}$ | C14 ADIN28 | C15 ADIN40 | C16 ADIN19 | C17 ADIN42 | C18 ADIN43 | C19 ADIN34 | C20 ADIN33 | C21 ADIN20 | C22 ADIN22 | C23 GND | C24 CLKIN |
| **B** | B1 GND | B2 ADOUT20 | B3 GND | B4 ADOUT37 | B5 ADOUT30 | B6 ADOUT43 | B7 $OV_{DD}$ | B8 ADOUT19 | B9 ADOUT17 | B10 GND | B11 BUS_CFG2 | B12 EI_DISABLE | B13 KELV_GND2 | B14 ADIN4 | B15 ADIN16 | B16 $OV_{DD}$ | B17 GND | B18 ADIN39 | B19 $OV_{DD}$ | B20 ADIN36 | B21 $OV_{DD}$ | B22 ADIN24 | B23 ADIN25 | B24 $\overline{\text{CLKIN}}$ |
| **A** | | A2 ADOUT22 | A3 $OV_{DD}$ | A4 ADOUT24 | A5 GND | A6 ADOUT34 | A7 ADOUT42 | A8 ADOUT38 | A9 ADOUT29 | A10 KELV_OVDD | A11 BUS_CFG0 | A12 AVDD | A13 ANALOGGND | A14 GND | A15 ADIN5 | A16 ADIN17 | A17 ADIN41 | A18 ADIN26 | A19 ADIN38 | A20 GND | A21 ADIN37 | A22 GND | A23 ADIN12 | A24 $OV_{DD}$ |
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** | **16** | **17** | **18** | **19** | **20** | **21** | **22** | **23** | **24** |

## 4.3 PowerPC 970MP Microprocessor Pinout Listings

The following table provides the pinout listing for the CBGA package.

*Table 4-4. Pinout Listing for the CBGA Package*

| Signal Name | Pin Number | Active | I/O PI/PO[5] | Notes |
|---|---|---|---|---|
| ADIN(0:43) | H23,G23,J24,H22,B14,A15,K22,J23,L24,E22,D23,E24, A23,G24,F23,D15,B15,A16,E15,C16,C21,E21,C22,D21, B22,B23,A18,D18,C14,E16,E17,E20,E19,C20,C19,D17, B20,A21,A19,B18,C15,A17,C17,C18 | — | Processor Input | — |
| ADOUT(0:43) | N2,G3,J2,L2,M2,K3,K2,H3,J1,E3,F1,D3,E1,F3,C7,E10, D10,B9,E9,B8,B2,E5,A2,E7,A4,C3,C1,C6,C10,A9,B5,D4, E4,C5,A6,D7,D6,B4,A8,E8,C9,D9,A7,B6 | — | Processor Output | — |
| ANALOG_GND | A13 | — | Analog GND | — |
| ATTENTION | AC7 | High | Output | — |
| $AV_{DD}$ | A12 | — | Analog $V_{DD}$ | — |
| $\overline{\text{AVP\_RESET}}$ | U24 | Low | Input | — |
| $\overline{\text{BI\_MODE}}$ | AD24 | Low | Input | — |
| BUS_CFG(0:2) | A11, D12, B11 | — | Input | 4 |
| $\overline{\text{BYPASS}}$ | T24 | Low | Input | — |
| C1_UND_GLOBAL | AB17 | High | Input | — |
| C2_UND_GLOBAL | AB15 | High | Input | — |
| $\overline{\text{CHKSTOP}}$ | T22 | Low | OD BiDi | — |
| CKTERM_DIS | Y5 | High | Input | — |
| CLKIN | C24 | — | Processor Input | — |
| $\overline{\text{CLKIN}}$ | B24 | — | Processor Input | — |
| CLKOUT | D2 | — | Processor Output | — |
| $\overline{\text{CLKOUT}}$ | D1 | — | Processor Output | — |
| CP0_DIODE_NEG | Y4 | — | — | — |
| CP0_DIODE_POS | Y3 | — | — | — |
| CP0_FRED_EN | Y11 | High | Input | — |
| CP0_FRED_GND | AC12 | — | GND | — |
| $\overline{\text{CP0\_HRESET}}$ | AA9 | Low | Input | — |

**Notes:**

1. For correct operation, these pin must be tied to GND. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.
2. I = Input, O = Output, PI = Processor Input, PO= Processor Output, BiDi = Bidirectional, OD=Open Drain. For additional information, see Section 3.5 Processor Interconnect Specifications on Page 26.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They **must not** be connected to GND and $V_{DD}$ planes. Refer to Section 5.4.1 on Page 56 *Table 3-2. Maximum Allowable Current on Kelvin Probe pins (DD1.1x) on page 18* for more details
4. The PLL_MULT and PLL_RANGE (1:0) bits may be overwritten by JTAG commands and the BUS_CFG bits may be changed by SCOM commands during the POR (power on reset) sequence. Refer to the PowerPC 970MP Power On Reset Application Note for more details.

*Table 4-4. Pinout Listing for the CBGA Package (Continued)*

| Signal Name | Pin Number | Active | I/O PI/PO[5] | Notes |
|---|---|---|---|---|
| CP0_INT | AB13 | Low | Input | — |
| CP0_KELV_GND0 | W2 | — | GND Test Points | 3 |
| CP0_KELV_V0 | AB4 | — | $V_{DD}$ Test Points | 3 |
| CP0_PSRO0 | V3 | — | Output | — |
| CP0_QACK | AD21 | Low | Input | — |
| CP0_QREQ | AB9 | Low | Output | — |
| CP0_SRESET | AB7 | Low | Input | — |
| CP1_DIODE_NEG | AC24 | — | — | — |
| CP1_DIODE_POS | AB24 | — | — | — |
| CP1_FRED_EN | AD17 | High | Input | — |
| CP1_FRED_GND | Y12 | — | GND | — |
| CP1_HRESET | AC16 | Low | Input | — |
| CP1_INT | AD20 | Low | Input | — |
| CP1_KELV_GND1 | W22 | — | GND Test Points | 3 |
| CP1_KELV_V1 | W21 | — | $V_{DD}$ Test Points | 3 |
| CP1_QACK | AD18 | Low | Input | — |
| CP1_QREQ | AC21 | Low | Output | — |
| CP1_SRESET | AB22 | Low | Input | — |
| DI2 | R24 | Low | Input | — |
| EI_DISABLE | B12 | High | Input | — |

**Notes:**

1. For correct operation, these pin must be tied to GND. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.
2. I = Input, O = Output, PI = Processor Input, PO= Processor Output, BiDi = Bidirectional, OD=Open Drain. For additional information, see Section 3.5 Processor Interconnect Specifications on Page 26.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They **must not** be connected to GND and $V_{DD}$ planes. Refer to Section 5.4.1 on Page 56 *Table 3-2. Maximum Allowable Current on Kelvin Probe pins (DD1.1x) on page 18* for more details
4. The PLL_MULT and PLL_RANGE (1:0) bits may be overwritten by JTAG commands and the BUS_CFG bits may be changed by SCOM commands during the POR (power on reset) sequence. Refer to the PowerPC 970MP Power On Reset Application Note for more details.

*Table 4-4. Pinout Listing for the CBGA Package (Continued)*

| Signal Name | Pin Number | Active | I/O PI/PO[5] | Notes |
|---|---|---|---|---|
| GND | A5,A14,A20,A22<br>B1,B3,B10,B17<br>C8,C23<br>D5,D11,D14,D20<br>E2,E18,E23<br>F7,F11,F13,F15,F20,F21,F24<br>G2,G4,G5,G6,G8,G10,G12,G16,G18<br>H2,H4,H7,H9,H11,H13,H15,H17,H19,H21<br>J4,J6,J8,J10,J12,J14,J16,J18,J20,J22<br>K1,K4,K7,K9,K11,K13,K15,K17,K19,K21,K24<br>L3,L6,L8,L10,L12,L14,L16,L18,L22<br>M5,M7,M9,M11,M13,M15,M17,M19,M21<br>N3,N4,N6,N8,N10,N12,N14,N16,N18,N20<br>P2,P5,P7,P9,P11,P13,P15,P17,P19,P21,P23,P24<br>R1,R4,R6,R8,R10,R12,R14,R16,R18,R20,R23<br>T5,T7,T9,T11,T13,T15,T17,T19,T21<br>U4,U6,U8,U10,U12,U14,U16,U18,U20<br>V5,V7,V9,V11,V13,V15,V17,V19,V21,V23<br>W1,W3,W6,W8,W10,W12,W16,W18,W20<br>Y7,Y9,Y13,Y15,Y17,Y19,Y22<br>AA1,AA2,AA6,AA8,AA10,AA12,AA14,AA16,AA18,AA20,AA24<br>AB2,AB5,AB19<br>AC1,AC8,AC10,AC11,AC18,AC22<br>AD2,AD5,AD12,AD14,AD16,AD19,AD23 | — | GND | — |
| GPULDBG | Y24 | High | Input | — |
| $\overline{\text{I2CCK}}$ | V24 | — | OD<br>BiDi | — |
| $\overline{\text{I2CDT}}$ | V22 | — | OD<br>BiDi | — |
| I2CGO | E13 | — | OD | — |
| I2CSEL | U1 | High | Input | |
| KELV_GND2 | B13 | — | GND<br>Test Points | 3 |
| KELV_OVDD | A10 | — | $OV_{DD}$<br>Test Points | 3 |
| LSSDMODE | U2 | High | Input | — |
| LSSD_RAMSTOP_ENABLE | T2 | High | Input | — |
| LSSD_SCAN_ENABLE | U22 | High | Input | — |

**Notes:**

1. For correct operation, these pin must be tied to GND. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.
2. I = Input, O = Output, PI = Processor Input, PO= Processor Output, BiDi = Bidirectional, OD=Open Drain. For additional information, see Section 3.5 Processor Interconnect Specifications on Page 26.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They **must not** be connected to GND and $V_{DD}$ planes. Refer to Section 5.4.1 on Page 56 *Table 3-2. Maximum Allowable Current on Kelvin Probe pins (DD1.1x) on page 18* for more details
4. The PLL_MULT and PLL_RANGE (1:0) bits may be overwritten by JTAG commands and the BUS_CFG bits may be changed by SCOM commands during the POR (power on reset) sequence. Refer to the PowerPC 970MP Power On Reset Application Note for more details.

*Table 4-4. Pinout Listing for the CBGA Package (Continued)*

| Signal Name | Pin Number | Active | I/O PI/PO[5] | Notes |
|---|---|---|---|---|
| LSSD_STOP_ENABLE | AC14 | High | Input | — |
| LSSD_STOPC2_ENABLE | AB11 | High | Input | — |
| LSSD_STOP_C2STAR_ENABLE | U3 | High | Input | — |
| MASTERSEL | R2 | — | Input | — |
| $\overline{\text{MCP}}$ | AA21 | Low | Input | — |
| PLL_LOCK | U23 | High | Output | — |
| PLL_MULT | AC5 | — | Input | 4 |
| PLL_RANGE(1:0) | AD3, AA4 | — | Input | 4 |
| PLLTEST | D13 | High | Input | — |
| PLLTESTOUT | C12 | — | Output | — |
| PROCID(0:1) | N21, N22 | — | Input | — |
| PSRO_ENABLE | Y21 | — | Input | — |
| PSYNC | P4 | — | Input | — |
| PULSE_SEL(0:2) | V1,T3,AD10 | — | Input | — |
| $\overline{\text{RI}}$ | W4 | Low | Input | — |
| SPARE1 | AD6 | — | Input/Output | 1 |
| SPARE2 | AC3 | — | Input/Output | 1 |
| SRIN(0:1) | N24,K23 | — | Processor Input | — |
| $\overline{\text{SRIN}}$(0:1) | M24,L23 | — | Processor Input | — |
| SROUT(0:1) | M1,H1 | — | Processor Output | — |
| $\overline{\text{SROUT}}$(0:1) | L1,G1 | — | Processor Output | — |
| $\overline{\text{SYNC\_ENABLE}}$ | W24 | Low | Input | — |
| SYSCLK | F12 | — | Input | — |
| $\overline{\text{SYSCLK}}$ | E12 | — | Input | — |
| TBEN | AD15 | High | Input | — |
| TCK | AB23 | — | Input | — |
| TDI | AA23 | — | Input | — |
| TDO | AD8 | — | Output | — |
| TMS | AD22 | — | Input | — |

**Notes:**

1. For correct operation, these pin must be tied to GND. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.
2. I = Input, O = Output, PI = Processor Input, PO= Processor Output, BiDi = Bidirectional, OD=Open Drain. For additional information, see Section 3.5 Processor Interconnect Specifications on Page 26.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They **must not** be connected to GND and $V_{DD}$ planes. Refer to Section 5.4.1 on Page 56 *Table 3-2. Maximum Allowable Current on Kelvin Probe pins (DD1.1x) on page 18* for more details
4. The PLL_MULT and PLL_RANGE (1:0) bits may be overwritten by JTAG commands and the BUS_CFG bits may be changed by SCOM commands during the POR (power on reset) sequence. Refer to the PowerPC 970MP Power On Reset Application Note for more details.

*Table 4-4. Pinout Listing for the CBGA Package (Continued)*

| Signal Name | Pin Number | Active | I/O PI/PO[5] | Notes |
|---|---|---|---|---|
| TRIGGEROUT | R22 | High | Output | — |
| $\overline{TRST}$ | AA13 | Low | Input | — |
| V0 | F5,F8,F10,F14,F18<br>G7,G9,G11,G13,G21<br>H6,H8,H10,H12,H20<br>J5,J7,J9,J11,J13<br>K6,K8,K10,K12<br>L5,L7,L9,L11<br>M4,M6,M8,M10,M12<br>N5,N7,N9,N11<br>P6,P8,P10,P12<br>R3,R5,R7,R9,R11<br>T1,T4,T6,T8,T10,T12<br>U5,U7,U9,U11<br>V2,V4,V6,V8,V10,V12<br>W5,W7,W9,W13<br>Y2,Y6,Y8<br>AA3,AA5,AA7,AA11<br>AB3,AB6,AB10<br>AC4,AC6<br>AD7,AD9,AD11 | — | $V_{DD}$ | — |
| V1 | F17<br>G15,G17,G19,G22<br>H14,H16,H18<br>J15,J17,J19<br>K14,K16,K18<br>L13,L15,L17,L19,L20,L21<br>M14,M16,M18,M20,M22<br>N13,N15,N17,N19,N23<br>P14,P16,P18,P20,P22<br>R13,R15,R17,R19,R21<br>T14,T16,T18,T20<br>U13,U15,U17,U19,U21<br>V14,V16,V18,V20<br>W15,W17,W19<br>Y14,Y16,Y18,Y20,Y23,<br>AA15,AA17,AA19,AA22<br>AB12,AB14,AB16,AB18,AB20,AB21<br>AC15,AC19<br>AD13 | — | $V_{DD}$ | — |

**Notes:**

1. For correct operation, these pin must be tied to GND. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.
2. I = Input, O = Output, PI = Processor Input, PO= Processor Output, BiDi = Bidirectional, OD=Open Drain. For additional information, see Section 3.5 Processor Interconnect Specifications on Page 26.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They **must not** be connected to GND and $V_{DD}$ planes. Refer to Section 5.4.1 on Page 56 *Table 3-2. Maximum Allowable Current on Kelvin Probe pins (DD1.1x) on page 18* for more details
4. The PLL_MULT and PLL_RANGE (1:0) bits may be overwritten by JTAG commands and the BUS_CFG bits may be changed by SCOM commands during the POR (power on reset) sequence. Refer to the PowerPC 970MP Power On Reset Application Note for more details.

*Table 4-4. Pinout Listing for the CBGA Package (Continued)*

| Signal Name | Pin Number | Active | I/O PI/PO[5] | Notes |
|---|---|---|---|---|
| V2 | A3,A24<br>B7,B16,B19,B21<br>C2,C4,C11,C13<br>D8,D16,D19,D22,D24<br>E6,E11,E14<br>F2,F4,F6,F9,F16,F19,F22<br>G14,G20<br>H5,H24<br>J3,J21<br>K5,K20<br>L4<br>M3,M23<br>N1<br>T23<br>W11,W14,W23<br>Y1,Y10<br>AB1,AB8<br>AC2,AC9,AC13,AC17,AC20,AC23<br>AD1,AD4 | — | $OV_{DD}$ | — |
| Z_OUT | P3 | — | — | 1 |
| Z_SENSE | P1 | — | — | 1 |

**Notes:**

1. For correct operation, these pin must be tied to GND. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.
2. I = Input, O = Output, PI = Processor Input, PO= Processor Output, BiDi = Bidirectional, OD=Open Drain. For additional information, see Section 3.5 Processor Interconnect Specifications on Page 26.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They **must not** be connected to GND and $V_{DD}$ planes. Refer to Section 5.4.1 on Page 56 *Table 3-2. Maximum Allowable Current on Kelvin Probe pins (DD1.1x) on page 18* for more details
4. The PLL_MULT and PLL_RANGE (1:0) bits may be overwritten by JTAG commands and the BUS_CFG bits may be changed by SCOM commands during the POR (power on reset) sequence. Refer to the PowerPC 970MP Power On Reset Application Note for more details.

# 5. System Design Information

This section provides electrical and thermal design recommendations for the successful application of the PowerPC PPC970MP.

## 5.1 External Resistors

The PowerPC PPC970MP contains no internal "pullup" resistors for any JTAG, $I^2C$, mode select, or asynchronous inputs. System designs must include these external resistors where required. See *Table 5-7* and *Table 5-8* and *Section 3.10.3 I2C and JTAG Considerations* for information on implementing external pullups/pulldowns.

## 5.2 PLL Configuration

This section will help in configuring the PLL and determining SYSCLK input frequency for PowerPC 970MP systems.

**Note:** For applications using external termination resistors on SYSCLK and $\overline{\text{SYSCLK}}$, CKTERM_DIS should be pulled up to $OV_{DD}$ to disable the internal termination. To use the internal 50 ohm parallel termination, CKTERM_DIS should be pulled to GND to avoid problems with PLL lock

### 5.2.1 Determining PLLMULT and BUS_CFG settings

The first step is to determine the bus frequency. This parameter is a critical component of overall system performance. The bus should run as fast as your memory controller/bridge chip can support. Once you have determined your maximum bus frequency, you should select a bus multiplier ratio that will deliver the optimal processor core frequency.

> **Note:** The PLL_MULT and PLL_RANGE bits may be overwritten by JTAG commands and the BUS_CFG bits may be changed by SCOM commands during the POR (power on reset) sequence. These overrides disappear after every $\overline{\text{HRESET}}$. Refer to the *PowerPC 970MP Power On Reset Application Note* for more details.

The available bus ratios are shown in *Table 5-1*. In most applications this would be the highest frequency possible for a given PowerPC 970MP part number, but other considerations (i.e., available power) may take precedence.

*Table 5-1. PowerPC 970MP Bus Configuration*

| BUS_CFG(0:2) | Ratio | Notes |
|---|---|---|
| 000 | 2:1 | |
| 001 | 3:1 | |
| 010 | 4:1 | 2 |
| 011 | 6:1 | 2 |
| 100 | 8:1 | 1 |
| 101 | 12:1 | 3 |
| 110 | 24:1 | 1 |
| 111 | Invalid | |

**Note:** BUS_CFG bits may be changed by SCOM commands during the POR sequence. Refer to the PowerPC 970MP System Design Manual

1. Bus ratios of 8:1 and 24:1 are not supported for Processor Input (PI) functionality and powertune.
2. Limited PowerTune frequency scaling.
3. No PowerTune frequency scaling.

The bus frequency multiplier ratio will usually indicate the desired PLL multiplier setting. Ratios of 3 (3:1, 6:1, 12:1) should always use PLLMULT=0 (low) for a PLL multiplier of 12. The desired core frequency should be divided by 12 to determine the required input SYSCLK frequency. Ratios of 2 (2:1, 4:1, 8:1, 24:1) should always use PLLMULT=1 (high) to multiply SYSCLK by 8.

> **Note:** Using bus frequency ratios of 3:1, 6:1 or 12:1 with PLLMULT=1 or ratios of 8:1 or 24:1 with PLL-MULT=0 is not recommended. Internal clock synchronization delays may reduce performance.

After the correct BUS_CFG(0:2) and PLL_MULT pin settings are determined, the required SYSCLK input frequency can be determined. The selected SYSCLK input frequency should be within the minimum/maximum frequencies specified in *Table 3-10* on page 23.

### 5.2.2 PLL_RANGE configuration

The PLL VCO configuration for the PowerPC PPC970MP, using the pins PLL_RANGE1 and PLL_RANGE0, is shown in *Table 5-2*.

*Table 5-2. PowerPC 970MP PLL Configuration*

| PLL_RANGE(1:0) Settings | | | |
|---|---|---|---|
| Range Name | PLL_RANGE1 | PLL_RANGE0 | Frequency Range |
| *Low* | 0 | 0 | $Freq < 1.2GHz$ |
| *Medium* | 0 | 1 | $1.2GHz \le Freq < 1.6GHz$ |
| *High* | 1 | 0 | $1.6GHz \le Freq$ |
| *Reserved* | 1 | 1 | Reserved |

**Notes:**

1. The PLL_MULT and PLL_RANGE(1:0) bits may be overwritten by JTAG commands and the BUS_CFG bits may be changed by SCOM commands during the POR (power on reset) sequence. Refer to the PowerPC 970MP Power On Reset Application Note for more details
2. PLL frequency range settings are not an indicator of availble PPC970MP processor speeds..

## 5.3 PLL Power Supply Filtering

The PowerPC PPC970MP microprocessor has a separate pin, $AV_{DD}$, which provides power to the clock generation phase-locked loop.

To ensure stability of the internal clock, filter the $AV_{DD}$ power and ANALOG_GND supplied to the PLL using a circuit similar to *Figure 5-1*. To ensure that the capacitor filters out as much noise as possible, the capacitor should be placed as close as possible to the $AV_{DD}$ and ANALOG_GND pins. The capacitor used should have minimal inductance. The ferrite bead (FB) shown in *Figure 5-1* should supply an impedance of less than 70Ω in the100-500MHz region. It is recommended that the ferrite bead be placed within 1.5cm, preferably closer, to the $AV_{DD}$ pin.

The intent of all the recommendations it to provide a low noise voltage input to the PLL circuit. Close proximity of the filter to the pins, as well as avoiding coupling to nearby traces both on the same plane and internal layers, especially after the filter is critical.

**Note:** $AV_{DD}$ measured at the pins of the part should never be more than 50 mV lower than the $AV_{DD}$ voltage range specified in *Table 3-3 Recommended Operating Conditions*.

*Figure 5-1. PLL Power Supply Filter Circuit*

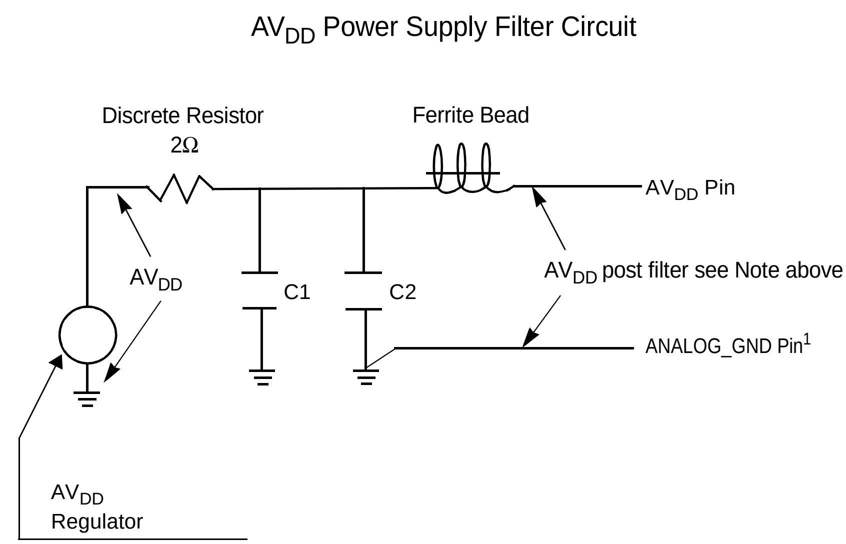



*Table 5-3. Filter Components*

| Item | Description/Value |
|---|---|
| Resistor | 2Ω |
| C1 | 0.1 µF X7F |
| C2 | 10.0 µF YV5 |
| Ferrite Bead | Murata BLM21PG300SN1 or similar |

**Notes:**

1. Connected to analog ground without a filter.

## 5.4 Decoupling Recommendations

Capacitor decoupling is required for the PowerPC PPC970MP. Decoupling capacitors act to reduce medium and high frequency chip switching noise and provide localized bulk charge storage to reduce major power surge effects. Guidelines for medium and high frequency noise decoupling will be provided. Bulk decoupling requires a more complete understanding of the system and system power architecture which precludes discussion in this document.

High frequency decoupling capacitors should be located as close as possible to the processor with low lead inductance to the ground and voltage planes.

The recommended placement of the decoupling capacitors is shown in *Figure 5-2* on page 58.

The decoupling capacitors in the center of the module, directly under the chip, are particularly potent in medium and high frequency noise reduction. Capacitance in this region should be maximized, while inductive parasitics are minimized. To achieve this, the recommended capacitor layout uses as many V0-GND and V1-GND capacitors as possible in this region.

*Table 5-4. Recommended Decoupling Capacitor Specifications*

| |
|---|
| 0402 size (1.00 x 0.50 mm) |
| 220 nF |
| Y5V or X7R dielectric |
| 6V voltage rating |

*Table 5-5. Required Minimum Number of Decoupling Capacitors*

| Required Minimum Number of Decoupling Capacitors<br>(See *Figure 5-2 on page 58)* |
|---|
| Minimum of 150 Total Decoupling Capacitors:<br>Minimum 67 V0-GND<br>Minimum 66 V1-GND<br>Minimum 17 OVDD-GND |
| **Note:** Add additional decoupling capacitors to improve noise performance. |

### 5.4.1 Using the Kelvin Voltage and Ground Pins

The PowerPC 970MP features 3 pairs of Kelvin voltage and GND pins to assist in analyzing on-chip noise and voltage drop. Pins CP0_KELV_V0 and CP0_KELV_GND0 are the V0-GND pair. Pins CP1_KELV_V1 and CP1_KELV_GND1 are the V1-GND pair. Pins KELV_OVDD and KELV_GND2 are the $OV_{DD}$-GND pair.

Table 3-2 on page 18 define the maximum current allowed on the Kelvin pins. Exceeding these maximum currents may cause permanent damage to the microprocessor. Oscilloscope probes should provide enough impedance to prevent excess current on these pins.

> **Caution:** The Kelvin Ground and Kelvin Voltage pins should never be connected into the normal voltage or GND planes. If a Kelvin pin is not in use, it requires a high impedance termination so that the current limits on the pins is not exceeded.

These pins should be brought out to test pads by traces that are as short as possible. An oscilloscope can be used on these test pads to measure on-chip voltage noise and thus to verify the decoupling and voltage regulation in a design.

It is recommended that the differential between CP0_KELV_V0 and CP0_KELV_GND0 be used as Vsense of the V0 voltage regulators, and that the differential between CP1_KELV_V1 and CP0_KELV_GND1 be used as Vsense of the V1 voltage regulators. If both V0 and V1 will share the same power plane, the V0 Kelvin pin should be used as Vsense of the voltage regulator. The KELV_V and KELV_GND pins used should be connected to the differential inputs of a suitable op-amp to limit current on those pins and also to provide some common mode noise rejection. The output of this op-amp is used as the Vsense of the voltage regulator.

This Vsense signal must be sufficiently filtered to ensure the tracking supply is not modulated by switching noise generated within the processor, consistent with maintaining stable regulation. The configuration and degree of filtering required will depend upon the response time and tracking accuracy of the power supplies, and the dynamics of application induced load changes.

### 5.4.2 Power Supply Sequencing and Ramping

The PowerPC 970MP power supplies may be ramped in any order as long as all supplies are stable and within the allowable tolerance within 2 seconds. The V1 supply is independent of any other supply rail during power up or down. However, when both V0 and V1 are powered, V0 and V1 should be regulated within 150mV of each other.

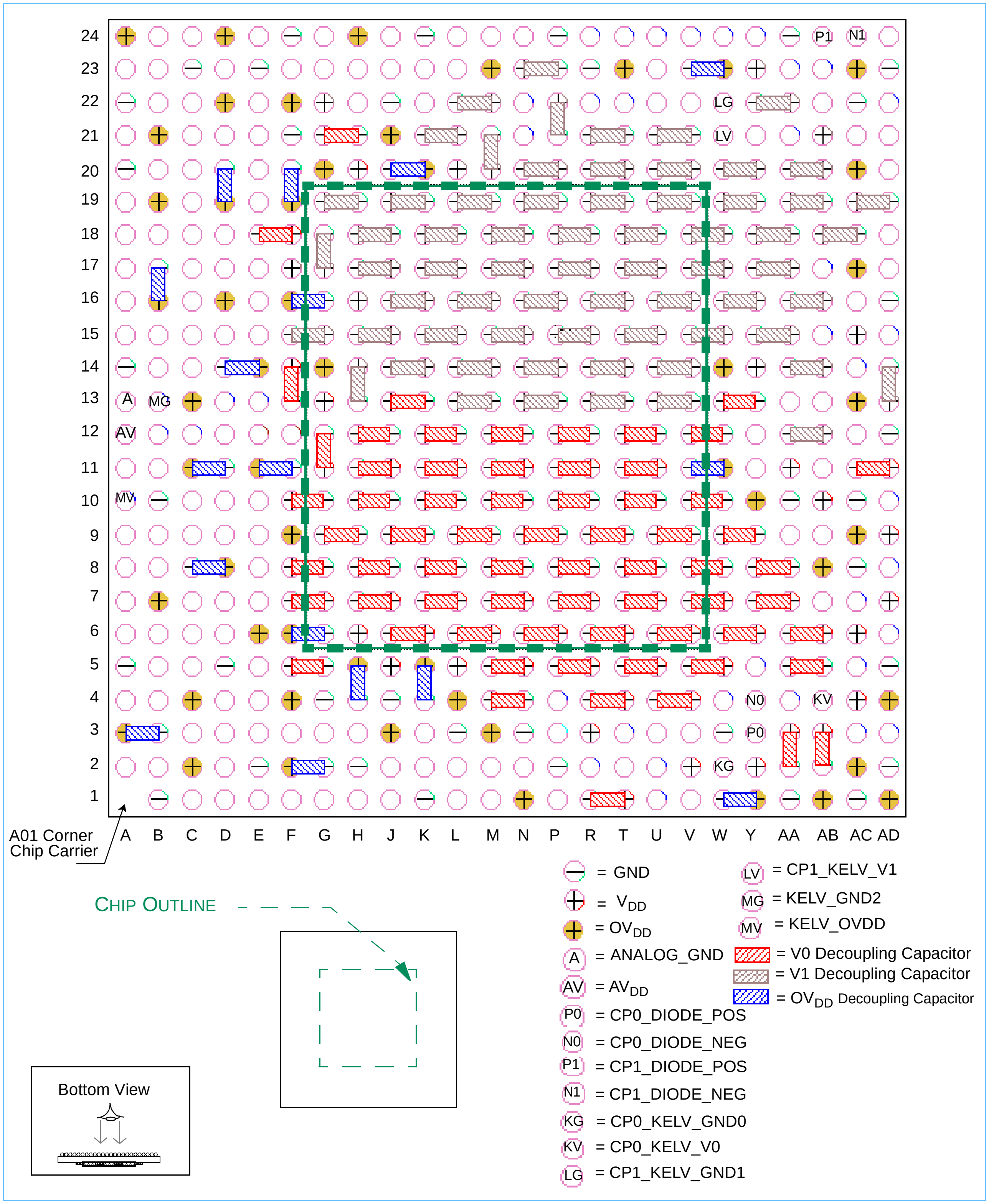
The maximum voltage differences during operation and while ramping must be maintained according to *Table 5-6* on page 57

*Table 5-6. Maximum Voltage Difference Between Supply Rails*

| Supply Rails | Maximum Difference During Operation (After 2 second ramp time) | Maximum Difference While Ramping (First 2 seconds) |
|---|---|---|
| V0 : $OV_{DD}$ | 0.8 V | 1.55 V |
| V0 : V1 | 150 mV | |
| V0 : $AV_{DD}$ | 2.5 V | 2.75 V |

## 5.5 *Decoupling Layout Guide*

*Figure 5-2. Decoupling Capacitor (Decap) Locations (Preliminary)*



## 5.6 Pull Up/Down Recommendations

For reliable operation, it is highly recommended that the unused inputs be connected to an appropriate signal level. For example:

- Unused active low inputs should be pulled up to $OV_{DD}$.
- Multiple unused active high inputs may be ganged together for convenience.
- Unused active high inputs should be connected to GND.
- Multiple unused active low inputs may be ganged together for convenience.
- All no-connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external V0, V1, $OV_{DD}$, $AV_{DD}$, ANALOG_GND, and GND pins of the PowerPC PPC970MP.

*Table 5-7* on page 59 provides details on the pin settings and information of the PowerPC 970MP Debug/Bringup signals. *Table 5-8* on page 60 provides details on the appropriate connections for the PowerPC 970MP Manufacturing Test only signals.

*Table 5-7. PowerPC 970MP Debug/Bringup Pin Settings and Information*

| Pin Name | In/Out/BiDi/JTAG[1] | Resistor Pull Up/Down Setting[2] | | Comments |
|---|---|---|---|---|
| $\overline{\text{AVP\_RESET}}$ | In | Up | | |
| C1_UND_GLOBAL | In | Down | | |
| C2_UND_GLOBAL | In | Down | | |
| GPULDBG[5] | In | UP | | |
| I2CGO | OD | Up | | Semaphore providing arbitration between $I^2C$ and JTAG. |
| I2CSEL[3] | In | —[4] | | Allows external selection of the $I^2C$ or JTAG interface for controlling scan functionality |
| TCK[3] | In-JTAG | Up | | JTAG – Test Clock |
| TDI[3] | In-JTAG | Up | | JTAG – Test Data In |
| TDO[3] | Out-JTAG | Up | | JTAG – Test Data Out |
| TMS[3] | In-JTAG | Up | | JTAG – Test Mode Select |
| TRIGGEROUT | Out | Down | | Make visible to external hardware. |
| $\overline{\text{TRST}}$ | In-JTAG | Up | | Not needed – $\overline{\text{HRESET}}$ does the cop reset function. Tie high and leave unconnected. |

**Notes:**

1. BiDi = Bidirectional
2. Pullups should use a 10K resistor to $OV_{DD}$. Pulldowns should use a 10K resistor to GND.
3. For $I^2C$ operation. Refer to *Section 3.10.3* on page 39.
4. Pull Up/Down Setting application dependent, refer to *Section 3.10.3* on page 39.
5. If GPULDBG = 1 during $\overline{\text{HRESET}}$ transition from low to high: Run POR in debug mode and stop after each POR instruction.
   If GPULDBG = 0 during $\overline{\text{HRESET}}$ transition from low to high: Run POR without stopping after each POR instruction.
   Toggling GPULDBG from 1 to 0 later on will exit POR debug mode and continue without stopping after each instruction
   Refer to the PowerPC 970MP Power On Reset Application Note

*Table 5-8. PowerPC 970MP Pins for Manufacturing Test Only*

| Pin Name | In/Out | Pullup/Pulldown | Notes |
|---|---|---|---|
| BI_MODE | In | Up | 1 |
| CP0_FRED_EN | In | Down | 2 |
| CP1_FRED_EN | In | Down | 2 |
| DI2 | In | Up | 1 |
| LSSDMODE | In | Down | 2 |
| LSSD_RAMSTOP_ENABLE | In | Down | 2 |
| LSSD_SCAN_ENABLE | In | Down | 2 |
| LSSD_STOPC2_ENABLE | In | Down | 2 |
| LSSD_STOP_C2STAR_ENABLE | In | Down | 2 |
| LSSD_STOP_ENABLE | In | Down | 2 |
| PLLTEST | In | Down | 2 |
| PSRO_ENABLE | In | Down | — |
| CP0_PSRO0 | Out | NC | — |
| PULSE_SEL(0:2) | In | Down | 2 |
| RI | In | Up | 1 |
| SPARE1 | In/Out | — | 3 |
| SPARE2 | In/Out | — | 3 |
| SYNC_ENABLE | In | —Down | 2 |
| Z_OUT | — | — | 3 |
| Z_SENSE | — | — | 3 |

**Note:**

1. Pullups should use a 10K resistor to $OV_{DD}$.
2. Pulldowns should use a 10K resistor to GND.
3. Should be tied to GND.

## 5.7 Input-Output Usage

*Table 5-9* on page 61 provides details on the input-output usage of the PowerPC 970MP signals.

### 5.7.1 Chip Signal I/O and Test Pins

The system signal names, debug and test pins are shown in *Table 5-9*.

*Table 5-9. Input/Output Signal Descriptions*

| Pin Name | Width | In/Out | System/Debug Function | Notes |
|---|---|---|---|---|
| ADIN(0:43) | 44 | In | **System: Processor Interface (PI)** Address or data and control information in | — |
| ADOUT(0:43) | 44 | Out | **System: PI** Address or data and control information out | — |
| ATTENTION | 1 | Out | If asserted, service processor should do a read of the JTAG register. | — |
| $\overline{\text{AVP\_RESET}}$ | 1 | In | **Manufacturing test use only** | — |
| $\overline{\text{BI\_MODE}}$ ) | 1 | In | **Manufacturing test use only** | — |
| $\overline{\text{BYPASS}}$ | 1 | In | Used to bypass the PLL. | — |
| BUS_CFG(0:2) | 3 | In | Bus configuration select. Select bus frequency division factor: Divide CPU clock by 2, 3, 4, 6, 8, 12, or 24<br>000 2:1<br>001 3:1<br>010 4:1<br>011 6:1<br>100 8:1<br>101 12:1<br>110 24:1<br>111 invalid | 1,3,4 |
| C1_UND_GLOBAL | 1 | In | **Debug:** adjusts C1 clock to internal latches, not used for normal operation | — |
| C2_UND_GLOBAL | 1 | In | **Debug:** adjusts C2 clock to internal latches, not used for normal operation | — |
| $\overline{\text{CHKSTOP}}$ | 1 | OD /BiDi | **System:** Checkstop in/out | 2 |
| CKTERM_DIS | 1 | In | Disables 50Ω parallel internal SYSCLK termination. Pulled up to $OV_{DD}$ for applications using external termination on SYSCLK and $\overline{\text{SYSCLK}}$. Otherwise, pulled low to GND. | — |
| CLKIN | 1 | In | **System: PI** Clock In; differential clock returned to the processor. | — |
| $\overline{\text{CLKIN}}$ | 1 | In | **System: PI** Clock In; differential clock returned to the processor. | — |
| CLKOUT | 1 | Out | **System: PI** Differential clock to the bus | — |

**Notes:**

1. Bus ratios 8:1 and 24:1 are not supported for Processor Input (PI) functionality
2. BiDi = Bidirectional. OD = Open Drain.
3. Using the 4:1 or 12:1 ratio with multiplier of 12 will limit the use of the PowerTune to (freq)/2.
4. The PLL_MULT may be overwritten by JTAG commands. Refer to the *PowerPC 970MP System Design Manual or PowerPC 970MP Users Manual* for more details.
5. For a 970MP, MASTERSEL should be controlled by the service processor in order to easily read the fuse string for each core. The fuse string is not to be read during normal operation. During normal operation of a 970MP, MASTERSEL must always be set to low (including during the entire power up sequence)
6. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.

*Table 5-9. Input/Output Signal Descriptions (Continued)*

| Pin Name | Width | In/Out | System/Debug Function | Notes |
|---|---|---|---|---|
| CLKOUT | 1 | Out | **System: PI** Differential clock to the bus | — |
| CP0_FRED_EN | 1 | In | Manufacturing only | — |
| CP1_FRED_EN | 1 | In | Manufacturing only | — |
| DI2 | 1 | In | **Manufacturing test use only** | — |
| EI_DISABLE | 1 | In | **Debug:** Disables the use of IAP, Initial Alignment Procedure,to adjust clock skew on the processor interface. | — |
| GPULDBG | 1 | In | **Debug:** POR debug mode select. | — |
| CP0_HRESET | 1 | In | **System:** Power on reset - core0 | — |
| CP1_HRESET | 1 | In | **System:** Power on reset - core1 | — |
| I2CCK | 1 | OD/BiDi | **System:** I$^2$C signal clock | 2 |
| I2CDT | 1 | OD/BiDi | **System:** I$^2$C interface data | 2 |
| I2CGO | 1 | OD | **Debug:** Semaphore signal to arbitrate JTAG/I$^2$C access | — |
| I2CSEL | 1 | In | **Debug:** Allows external selection of the I$^2$C or JTAG interface for controlling scan functionality | — |
| CP0_INT | 1 | In | **System**: External interrupt when low - core0 | — |
| CP1_INT | 1 | In | **System:** External interrupt when low - core1 | — |
| LSSD_RAMSTOP_ENABLE | 1 | In | **Manufacturing test use only** | — |
| LSSD_SCAN_ENABLE | 1 | In | **Manufacturing test use only** | — |
| LSSD_STOP_ENABLE | 1 | In | **Manufacturing test use only** | — |
| LSSD_STOPC2_ENABLE | 1 | In | **Manufacturing test use only** | — |
| LSSD_STOPC2STAR_ENABLE | 1 | In | **Manufacturing test use only** | — |
| LSSDMODE | 1 | In | **Manufacturing test use only** | — |
| MASTERSEL | 1 | In | **System:** External selection of PU0 or PU1 as the master core | 5 |
| MCP | 1 | In | **System:** Machine check interrupt | — |
| PLL_LOCK | 1 | Out | Indicates PLL has locked | — |
| PLL_MULT | 1 | In | Select PLL multiplication factor:<br>0 = multiply ref frequency by 12<br>1 = multiply ref frequency by 8 | 4 |
| PLL_RANGE(1:0) | 2 | In | To select PLL frequency range, refer to *Table 5-2 on page 54* | — |

**Notes:**

1. Bus ratios 8:1 and 24:1 are not supported for Processor Input (PI) functionality
2. BiDi = Bidirectional. OD = Open Drain.
3. Using the 4:1 or 12:1 ratio with multiplier of 12 will limit the use of the PowerTune to (freq)/2.
4. The PLL_MULT may be overwritten by JTAG commands. Refer to the *PowerPC 970MP System Design Manual or PowerPC 970MP Users Manual* for more details.
5. For a 970MP, MASTERSEL should be controlled by the service processor in order to easily read the fuse string for each core. The fuse string is not to be read during normal operation. During normal operation of a 970MP, MASTERSEL must always be set to low (including during the entire power up sequence)
6. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.

*Table 5-9. Input/Output Signal Descriptions (Continued)*

| Pin Name | Width | In/Out | System/Debug Function | Notes |
|---|---|---|---|---|
| PLLTEST | 1 | In | **Manufacturing test use only** | — |
| PLLTESTOUT | 1 | Out | Measure PLL output (divide by 64) | — |
| PROCID(0:1) | 2 | In | **System**: Processor id | — |
| PSRO_ENABLE | 1 | In | **Manufacturing test use only.** | — |
| CP0_PSRO0 | 1 | Out | **Manufacturing test use only** | — |
| PSYNC | 1 | In | **System:** Phase Synchronization with companion chip | — |
| PULSE_SEL(0:2) | 3 | In | | — |
| $\overline{\text{CP0\_QACK}}$ | 1 | In | **System:** Acknowledge of quiescence from system - core0 | — |
| $\overline{\text{CP1\_QACK}}$ | 1 | In | **System:** Acknowledge of quiescence from system - core1 | — |
| $\overline{\text{CP0\_QREQ}}$ | 1 | Out | **System:** Request from processor to quiesce system (nap mode) | |
| $\overline{\text{CP1\_QREQ}}$ | 1 | Out | **System:** Request from processor to quiesce system (nap mode) | |
| $\overline{\text{RI}}$ | 1 | In | **Manufacturing test use only** | — |
| SPARE1 | 1 | In/Out | | 6 |
| SPARE2 | 1 | In/Out | | 6 |
| $\overline{\text{CP0\_SRESET}}$ | 1 | In | **System:** Soft reset - core0 | — |
| $\overline{\text{CP1\_SRESET}}$ | 1 | In | **System:** Soft reset - core1 | — |
| SRIN(0:1) | 2 | In | **System: PI** Snoop response in | — |
| $\overline{\text{SRIN}}$(0:1) | 2 | In | **System: PI Inverse** of Snoop response in | — |
| SROUT(0:1) | 2 | Out | **System: PI** Snoop Response out | — |
| $\overline{\text{SROUT}}$(0:1) | 2 | Out | **System:PI** Inverse of Snoop Response out | — |
| $\overline{\text{SYNC\_ENABLE}}$ | 1 | In | **Manufacturing test use only** | — |
| SYSCLK | 1 | In | System Reference clock (differential input) | — |
| $\overline{\text{SYSCLK}}$ | 1 | In | System Reference clock (differential input) | — |
| TBEN | 1 | In | **System:** Time base enable | — |
| TCK | 1 | In | **JTAG:** Test Clock which is separate from system clock tree. Controls all Test Access Port functions | — |
| TDI | 1 | In | **JTAG:** Serial input used to feed test data and Test Access Port instructions. | — |

**Notes:**

1. Bus ratios 8:1 and 24:1 are not supported for Processor Input (PI) functionality
2. BiDi = Bidirectional. OD = Open Drain.
3. Using the 4:1 or 12:1 ratio with multiplier of 12 will limit the use of the PowerTune to (freq)/2.
4. The PLL_MULT may be overwritten by JTAG commands. Refer to the *PowerPC 970MP System Design Manual or PowerPC 970MP Users Manual* for more details.
5. For a 970MP, MASTERSEL should be controlled by the service processor in order to easily read the fuse string for each core. The fuse string is not to be read during normal operation. During normal operation of a 970MP, MASTERSEL must always be set to low (including during the entire power up sequence)
6. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.

*Table 5-9. Input/Output Signal Descriptions (Continued)*

| Pin Name | Width | In/Out | System/Debug Function | Notes |
|---|---|---|---|---|
| TDO | 1 | Out | **JTAG:** Serial output used to extract data from the chip under test control. | — |
| TMS | 1 | In | **JTAG:** Select used to control the operation of the JTAG state machine | — |
| TRIGGEROUT | 1 | Out | Signal to indicate internal trace collection has begun. | — |
| $\overline{\text{TRST}}$ | 1 | In | **JTAG:** Asynchronous Reset for the JTAG state machine. | — |

**Notes:**

1. Bus ratios 8:1 and 24:1 are not supported for Processor Input (PI) functionality
2. BiDi = Bidirectional. OD = Open Drain.
3. Using the 4:1 or 12:1 ratio with multiplier of 12 will limit the use of the PowerTune to (freq)/2.
4. The PLL_MULT may be overwritten by JTAG commands. Refer to the *PowerPC 970MP System Design Manual or PowerPC 970MP Users Manual* for more details.
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6. Refer to *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only*.

## 5.8 Thermal Management Information

### 5.8.1 Thermal Management Pins

Each PPC970MP processor features on-die temperature sensing diodes. A schematic of the thermal diode is shown in *Figure 5-3*. PU0's diode is connected to pins CP0_DIODE_NEG (Y4) and CP0_DIODE_POS (Y3). PU1's diode is connected to pins CP1_DIODE_NEG (AC24) and CP1_DIODE_POS (AB24). Each diode is tested at 70°C with no power applied ($V_{DD}$ = 0V); a current of 100µA is forced through each diode and the voltage drop is verified between 0.60V and 0.80V. External circuitry should force a controlled 100µA current through the diode and monitor voltage to determine on-chip temperature. Accuracy of this technique is application dependent and is likely to require some calibration to ensure best performance.

Other temperature sensors or monitoring hardware should also be implemented with the PowerPC PPC970MP and mounted as close to the PowerPC PPC970MP as practical. If the external temperature-sensing hardware determines that an unsafe operating temperature has been reached, initiate power management or shutdown the system.

**Note:** The alert operating temperature setting is application dependent.

*Figure 5-3. Thermal Diode Schematic*

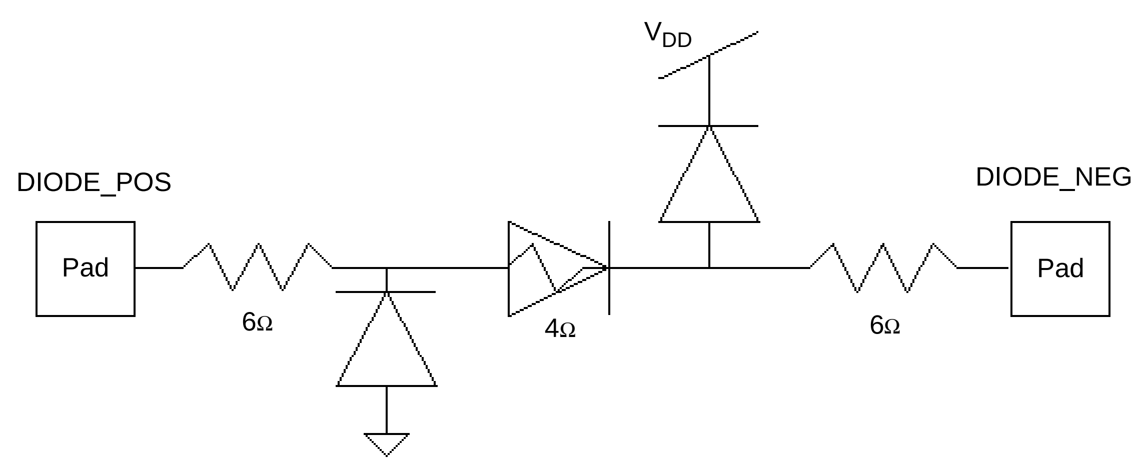
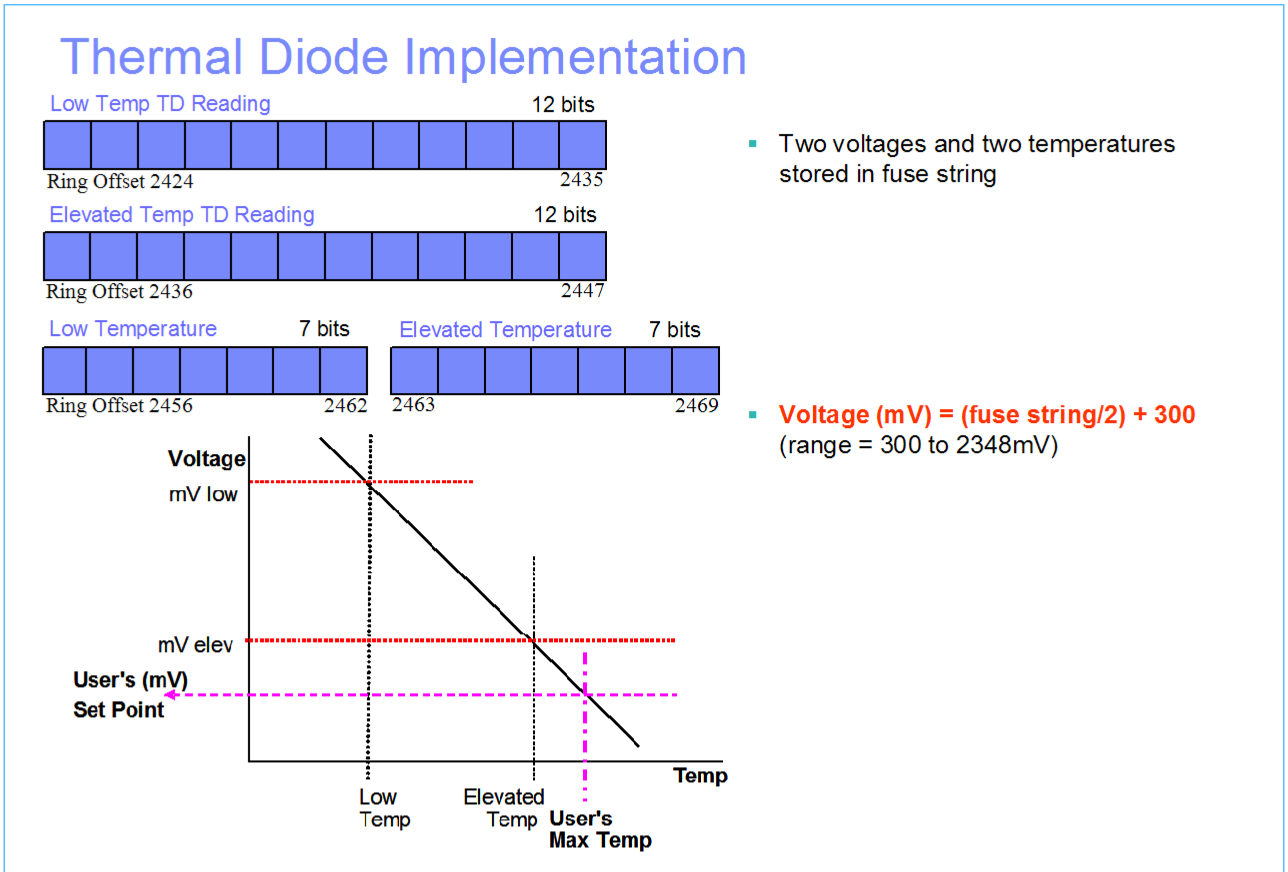


*Figure 5-4* provides a description of the PPC970MP Processor Thermal Diode Implementation.

*Figure 5-4. PowerPC PPC970MP Processor Thermal Diode Implementation*




## 5.9 Scanning Thermal Diode Calibration and $V_{DD}$ Fuse Code Data

### 5.9.1 Reading Thermal Diode Calibration and $V_{DD}$ Fuse Code data

**Note:** For correct fuse operation, make sure the SPARE1 and SPARE_2 pins are tied to GND.

In order to access the Thermal Diode Calibration data stored in each processor, a sequence of JTAG or $I^2C$ commands must be issued. By using JTAG or $I^2C$ commands, the desired data will appear serially on the PPC970MP TDO pin or can be read using $I^2C$. For the PPC970MP, this data must be read for each core.

This is a one-time only procedure. It is assumed the Thermal Diode Calibration and $V_{DD}$ Fuse Code, VFC, data stored in each processor will be captured and stored in system ROM for subsequent use. This procedure is not meant to be run at every system startup; since reading out this calibration data leaves the processor in an unusable state, until it is restarted.

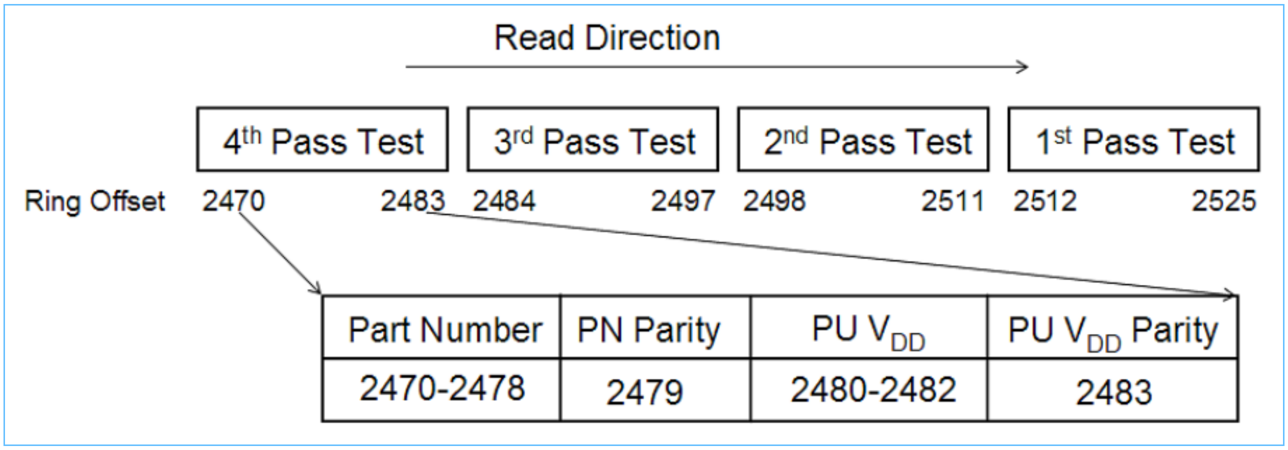
During the power-on reset (POR) sequence, the processor comes to a WAIT state to allow the service processor to scan the MODE ring facility. It is during this WAIT state that the thermal diode data can be scanned out. Scanning the MODE ring is not necessary. Much more detail about reading the fuse data is described in the PowerPC 970MP Power On Reset Application Note.

### 5.9.2 VFC Fusing Implementation

Processing Unit 0 and Processing Unit 1 are fused separately. The part number is represented by 9 fused bits plus 1 parity bit. The voltage for the processing unit is represented by 3 fused bits plus 1 parity bit. While there is VFC data for each processing unit the values are the same on a per part basis

There are four possible locations for the VFC data. All fourteen bits in the 4th Pass Test location should be read first. If 0, then proceed to read all fourteen bits in the 3rd Pass Test location. If 0, then read all fourteen bits in the 2nd Pass Test location. If 0, then read all fourteen bits in the 1st Pass Test location. If 0, the processor was not fused with VFC data and you should notify your IBM product representative. The first test location with non-zero data should be decoded and no further test locations should be read. Refer to Figure 5-5 for more details on the PPC970MP VFC data implementation.

*Figure 5-5. PowerPC PPC970MP VFC Implementation*




### 5.9.3 Booting Voltage

The maximum voltage for the specified processor frequency per tables *Table 3-7 970MP V0 and V1, VDD* and *Table 3-9 970MP V0 and V1, VDD* must be used to boot the processor until the VFC data is read. This means that reading VFC data and setting the voltage regulator should be done as soon as possible.

## 5.10 Heatsink Attachment and Mounting Forces

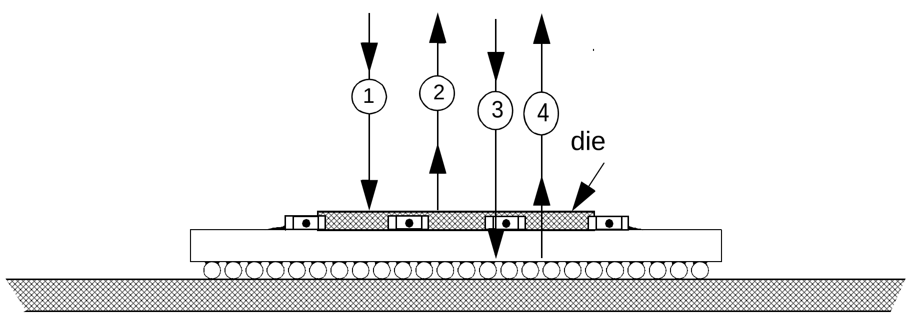
*Table 5-10* and *Figure 5-6* describe the allowable forces for the PowerPC 970MP package. Heatsink design should not exceed these static or dynamic forces.

*Table 5-10. Allowable Forces on the PowerPC 970MP Package*

| Call Out Number | Characteristic | | Symbol | Maximum | Unit[1] | Note |
|---|---|---|---|---|---|---|
| 1 | Compressive force on the die | Static | $F_C$ | 133.5 | N | 2 |
| | | Dynamic | | 133.5 | N | 2 |
| 2 | Tensile force on the die | Static | $F_T$ | 530 | N | 2 |
| | | Dynamic | | 530 | N | 2 |
| 3 | Compressive force on the BGA balls | Static | $F_{BGA}$ | 90.3 | N | |
| | | Dynamic | | 113.0 | N | 3 |
| 4 | Tensile force on the BGA balls | Static | $F_T$ | 0 | N | |
| | | Dynamic | | 17.6 | N | |

**Note:**
1. One newton = 0.2248089 pound-force.
2. May be limited by the BGA limit
3. The maximum force value for call-out item 3 must include the force value for call-out item 1.

*Figure 5-6. Force Diagram for the PowerPC 970MP Package*




**Note:**
1. The legend for this figure is provided by call out number in *Table 5-10* on page 68.

## 5.11 Operational and Design Considerations.

### 5.11.1 I$^2$C Addressing of PowerPC 970MP

The I$^2$C address of PowerPC 970MP processor is specified by the binary value 0b1000ppc where pp = the setting of the Processor ID bits PROCID(0:1), and c identifies the core, c=0 for PU0 and c=1 for PU1. For example, if the PROCID bits are both set to 0, the address for PU0 is 0b1000000, and the address for PU1 is 0b1000001. If the PROCID bits are set to 0b01, the address for PU0 is 0b1000010, and the address for PU1 is 0b1000011, and so forth.

# Revision Log

| Revision | Modification |
|---|---|
| July 31, 2006 | Update for General Availability:<br>• Declassified<br>• Updated power and part number tables. |