1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-10-12

SCHEM,FLYING_DUTCHMAN,MLB,K91F

REV B RELEASE, 01/31/11

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8620	1	SCHEM,MLB,K91	SCH	CRITICAL	
820-2915	1	PCBF,MLB,K91	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Jan 31 12:49:37 2011

DRAWING TITLE: SCHEM,MLB,K91

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

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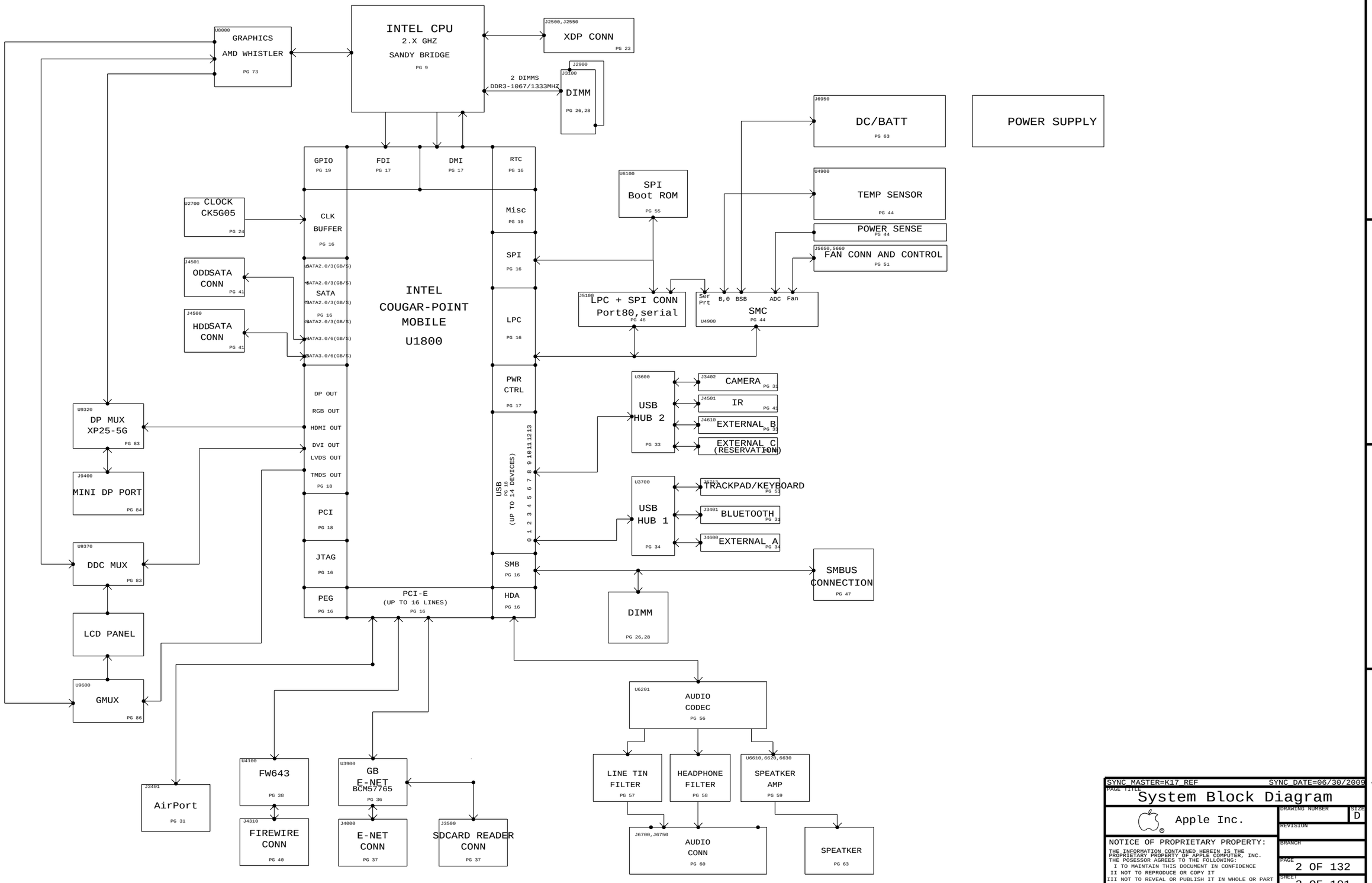

SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE
System Block Diagram

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K91 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN — DCIN(16.5V) — F6905 6A FUSE — SMC_DCIN_ISENSE — R7020 — U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64) — SMC_RESET_L — R7050 — SMC_BATT_ISENSE

PP18V5_DCIN_CONN — R6990 — D6990 — PPBUS_G3H — F7040 8A FUSE — PPVBAT_G3H

SMC_PBUS_VSENSE — Q5315 — ENABLE 3.425V G3HOT PM6640 U6990 (PAGE 62) — PP3V42_G3H

SMC PWRGD NCP303LSN U5000 (PAGE 45) — SMC_RESET_L

SMC AVREF SUPPLY REF3333 (PAGE 45) — PP3V3_S5_AVREF_SMC — PP3V3_S5_SMC

SMC_TPAD_RST_L, SMC_ONOFF_L — U5001

PP5V_S3_GFXIMVP6_VDD — GPU VCORE ISL6263C U8900 (PAGE 82) — R5388/U5388 — GPUVCORE_EN — GPUVCORE_PGOOD

SMC_GPU_VSENSE — U5410 SMC_GPU_ISENSE — PPVCORE_GPU

PP5V_S0_CPUVTTS0 — 1.05V ISL95870 U7600 (PAGE 70) — CPUVTTS0_EN — CPUVTTS0_PGOOD

R7640 — PPCPUVTT_S0 — SMC_CPU_FSB_ISENSE — TPS22924 U4202 (PAGE 39) — PP1V0_FW_FWPHY — FW_PWR_EN

J6950 — 3S2P (9 TO 12.6V) — PPVBATT_G3H_CONN — Q7055 — CHGR_BGATE — PPVBAT_G3H_CHGR_R

SMC_CPU_HI_ISENSE — CPU VCORE ISL95831 U7400 (PAGE 67) — CPUIMVP7_VR_ON — CPUIMVP7_AXG_PGOOD

SMC_CPU_VSENSE — SMC_CPU_ISENSE — PPVCORE_S0_CPU

GMUX U9600 XP25-5 (PAGE 86)

PB16B	EG_RAIL1_EN	P1V1GPU_EN
PB17A	EG_RAIL2_EN	P3V3GPU_EN
PB17B	EG_RAIL3_EN	GPUVCORE_EN
PB18A	EG_RAIL4_EN	
PL32A	PM_ALL_GPU_PGOOD	

SMC U4900 (PAGE 44) — P60 — SMC_PM_G2_EN — RC DELAY — P3V3S5_EN

COUGAR-POINT MOBILE U1800 (PAGE 16~21)

SLP_S5#(E4)	PM_SLP_S5_L
RC DELAY	P5VS3_EN
RC DELAY	DDRREG_EN
—	P3V3S3_EN
SLP_S4#(H7)	PM_SLP_S4_L
SLP_S3#(P12)	PM_SLP_S3_L

R7978 — PM_SLP_S3_L_R

RC DELAY: P1V8S0_EN, P1V2S0_EN, CPUVTTS0_EN, P1V5CPU_EN → P5VS0_EN, P3V3S0_EN, PBUSVSENS_EN

PP5V_S3_DDRREG — P1V0GPU_EN — P1V5FB_EN — EN1 1.003V(L/H) EN2 1.503V(R/H) ISL6236 U9500 (PAGE 85) — R5413 — PP1V5_GPU_REG — SMC_GPU_1V8_ISENSE — P1V0GPU_PGOOD — P1V5FB_PGOOD

DDRREG_EN, DDRVTT_EN — S5 1.5V / S3 0.75V TPS51116 U7300 (PAGE 66) — PPDDR_S3_REG — PPVTT_S0_DDR_LDO — DDRREG_PGOOD

SMC_DDR_ISENSE — R7350 — U5440 SMC_CPU_DDR_VSENSE — PP1V5_S3

4.5V VIN MAX8840 EN U6200 — PP3V3_S0 — PP4V5_AUDIO_ANALOG

P1V5CPU_EN — SLG5AP020 U7801 — PP1V5_S3 — Q7801 — PP1V5_S3RS0 — P1V5S0FET_GATE

Q7860 — PP5V_S0 — P5VS0_EN

P5VS3_EN, P3V3S5_EN — VREG5 5V (L/H) 3.3V (R/H) TPS51125 U7201 (PAGE 65) — PP5V_S3 — PP3V3_S5

Q9806 — BKLT_PLT_RST_L && LCD_BKLT_NO — BKLT_EN — VIN LP8550 U9701 (PAGE 87) — PPVOUT_S0_LCDBKLT — P5V3V3_PGOOD

Q4260 — PFWBOOST — SMC_ADAPTER_EN&&PM_SLP_S3_L

Q7870 — PP3V3_S0GPU — P3V3GPU_EN

Q7810 — PP3V3_S3 — P3V3S3_EN

Q7830 — PP3V3_S0_FET — P3V3S0_EN

TPS22924 U4201 (PAGE 39) — PP3V3_FW_FWPHY — FW_PWR_EN

Q7922 — PP3V3_ENET — PM_SLP_S3_L&&WOL_EN||SMC_ADAPTER_EN

P1V8FB_EN — SLG5AP020 U7880 — PP1V8_S0 — Q7880 — PP1V8_GPUIFPX — P1V8GPUIFPXFET_GATE

U7980 — PM_ALL_GPU_PGOOD — ALL_SYS_PWRGD — RSMRST_PWRGD — SMC_ONOFF_L — 99ms DLY — PP3V3_S0_PWRCTL — P1V8S0_PGOOD — P5V3V3_PGOOD — S0PGOOD_PWROK

P1V8S0_EN — ISL8014A U7720 (PAGE 70) — PP1V8_S0 — P1V8S0_PGOOD

P1V2ENET_EN — ISL8014A U7760 (PAGE 70) — PP1V2_ENET — P1V2ENET_PGOOD — Q7850 — PP1V2_S0 — P1V2S0_EN

PP3V3_S0 — U7971 ISL88042IRTJJZ (PAGE 72) — PP1V5_S0 — PP1V05_S0 — TRST = 200mS

PM_PCH_PWRGD — U2850

COUGAR_POINT U1800 (PAGE 16~21)

PWRBTN	PM_PWRBTN_L
SYS_RESET	
RSMRST	
ACPRESENT	
PLTRST	PLT_RERST_L
PROCPWRGD	CPU_PWRGD
DRAMPWROK	PM_MEM_PWRGD

CPU U1000 (PAGE 9~14) — SM_DRAMPWROK — VCCCPUPWRGD — RESET#

SMC U4900 (PAGE 45)

PWRGD(P12)	SMC_ADAPTER_EN
RSMRST_IN(P13)	PM_RSMRST_L
RSMRST_OUT(P14)	
PWR_BUTTON(P90)	CPUIMVP_VR_ON
IMVP_VR_ON(P16)	
SYSRST(P93)	PM_SYSRST_L
P17(BTN_OUT)	PM_PWRBTN_L
RES*	SMC_RESET_L
SLP_S5_L(P95)	PM_SLP_S5_L
SLP_S4_L(P94)	PM_SLP_S4_L
SLP_S3_L(P93)	PM_SLP_S3_L

H8S2117

SYNC_MASTER=K17_REF — SYNC_DATE=06/30/2009

PAGE TITLE: Power Block Diagram

Apple Inc.

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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1468	PCBA,MLB,K91F,DG64	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG64
639-1972	PCBA,MLB,K91F,DL83	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL83
639-1971	PCBA,MLB,K91F,DL82	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL82
639-1469	PCBA,MLB,K91F,DG65	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG65
639-1970	PCBA,MLB,K91F,DL86	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL86
639-1956	PCBA,MLB,K91F,DL7W	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7W
639-1470	PCBA,MLB,K91F,DG66	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG66
639-1974	PCBA,MLB,K91F,DL87	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL87
639-1976	PCBA,MLB,K91F,DL88	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL88
639-1471	PCBA,MLB,K91F,DG67	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG67
639-1973	PCBA,MLB,K91F,DL81	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL81
639-1954	PCBA,MLB,K91F,DL7T	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7T
639-1573	PCBA,MLB,K91,DHMV	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DHMV
639-1945	PCBA,MLB,K91,DL7Q	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7Q
639-1953	PCBA,MLB,K91,DL7R	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7R
639-1574	PCBA,MLB,K91,DHMW	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DHMW
639-1959	PCBA,MLB,K91,DL80	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL80
639-1960	PCBA,MLB,K91,DL7Y	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL7Y
085-1901	K91/K91F DEVELOPMENT BOM	K91_DEVEL:ENG

K91 BOM GROUPS

BOM GROUP	BOM OPTIONS
K91_COMMON	ALTERNATE,COMMON,K91_COMMON1,K91_COMMON2,K91_PROGPARTS,K91_PROGPARTS1,UVGLUE_K91_K91F,K91_PVT
K91_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_2NONREM,USBHUB_2513B
K91_COMMON2	GPUVID_1P11V,KB_BL,T29:YES,ENET_SD:B0,T29BST:Y,SDRV_PD,SDRVI2C:MCU,T29_DP_HPD:ALL_OR
K91_PVT	BMON:PROD,VREFMRGN_NOT,XDP,XDP_CPU_BPM,BKLT:PROD,ISNS_ON:NO,LPCPLUS_R:YES
K91_PROGPARTS	GMUX_PROG,IR_PROG,TPAD_PROG:PVT,ENETROM_PROG:PVT,T29ROM:PROG,T29MCU:PROG
K91_PROGPARTS1	SMC_PROG:PVT,BOOTROM_PROG:PVT
K91_DEVEL:ENG	SNB_CPT_XDP,BMON:ENG,GMUX_JTAG_CONN,VREFMRGN,LPCPLUS_CONN:YES,LPCPLUS_R:YES,BKLT:ENG,S0PGOOD_ISL,CPURIPPLE_ENG,IMVPISNS_ENG,ISNS_ON:YES,DEBUG_ADC,DIGI_MIC
K91_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS_CONN:YES,LPCPLUS_R:YES
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4031	1	IC,CPU,SNB,SR030,PRQ,D2,2.0,45W,4+2,1.20,6M,BGA	U1000	CRITICAL	CPU:2_0GHZ
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ,D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT,SLH9D,PRQ,BD82HM65	U1800	CRITICAL	
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	GPU:WHISTLER
337S3979	1	IC,GPU,AMD,SEYMOUR,M2 LP,ES1,962BGA	U8000	CRITICAL	GPU:SEYMOUR
338S0945	1	IC,ASSP,LIGHTRIDGE,S LHAJ,PRQ,FCBGA,15X15MM	U3600	CRITICAL	T29:YES
343S0534	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN8X8,B0	U3900	CRITICAL	ENET_SD:B0
343S0494	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN8X8,A0	U3900	CRITICAL	ENET_SD:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
333S0543	2	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8500,U8550	CRITICAL	FB_256_SAMSUNG
333S0564	2	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8500,U8550	CRITICAL	FB_256_HYNIX
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
725-1479	1	MLB LOCTITE UV EB CPU,PCH,T29,GPU,K91	UV_GLUE_K91_K91F	CRITICAL	UVGLUE_K91_K91F
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID

ETHERNET ROM

335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET,1MBITFLASH,CIV REV01,K74/K75,K40	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S2973	1	IC,ENET,1MBITFLASH,CIV REV01,K60/K62	U3990	CRITICAL	ENETROM_PROG:B0_SD
341S3026	1	IC,ENET,1MBITFLASH,CIV REV01,K901/K91/K92	U3990	CRITICAL	ENETROM_PROG:EVT
341S3096	1	IC,ENET ROM,1MBIT,DVT,PVT,K901/K91x	U3990	CRITICAL	ENETROM_PROG:PVT

Alternate Parts

(Alternate) (Primary)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
353S2805	353S2603		ALL	Fairchild wafer option
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
353S3085	353S1658		ALL	ST Micro alt to LT
376S0972	376S0612		ALL	ROHM alt to Toshiba N-FET
376S0855	376S0613		ALL	Diodes alt to Toshiba dual N-FET
138S0676	138S0691		ALL	Murata alt to Samsung cap
138S0652	138S0648		ALL	Samsung / Murata alt for Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt for Samsung
152S0685	152S0796		ALL	Sale/Vishay/TDK alt for Cyntec
376S0977	376S0859		ALL	Diodes alt for Rohm
353S2592	353S3199		ALL	1024x1 24BIT CBRIC OLD REV 3C ULTRAWIN FOR NEW REV
335S0550	335S0777		ALL	add 4K byte as alternative to 2K
371S0679	371S0652		ALL	NXP alternate for pin diodes
138S0671	138S0673		ALL	Taiyo Yuden alt for Murata 10 uF caps

EFI ROM

335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO0, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO2, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

PSOC

341S2902	1	IC,TP PSOC,K9x,PROTO0	U5701	CRITICAL	TPAD_PROG:PROTO0
341S2940	1	IC,TP PSOC,K9x,PROTO1	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3001	1	IC,TP PSOC,K9x,PROTO2	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,K9x,EVT	U5701	CRITICAL	TPAD_PROG:EVT
341S3099	1	IC,TP PSOC,K9x,DVT,PVT	U5701	CRITICAL	TPAD_PROG:PVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DDKG]	CRITICAL	EEEE:DDKG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG63]	CRITICAL	EEEE:DG63
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG64]	CRITICAL	EEEE:DG64
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG65]	CRITICAL	EEEE:DG65
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG66]	CRITICAL	EEEE:DG66
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG67]	CRITICAL	EEEE:DG67
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMV]	CRITICAL	EEEE:DHMV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMW]	CRITICAL	EEEE:DHMW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL81]	CRITICAL	EEEE:DL81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL82]	CRITICAL	EEEE:DL82
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL83]	CRITICAL	EEEE:DL83
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL84]	CRITICAL	EEEE:DL84
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL85]	CRITICAL	EEEE:DL85
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL86]	CRITICAL	EEEE:DL86
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL87]	CRITICAL	EEEE:DL87
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL88]	CRITICAL	EEEE:DL88
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL89]	CRITICAL	EEEE:DL89
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Q]	CRITICAL	EEEE:DL7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7R]	CRITICAL	EEEE:DL7R
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7T]	CRITICAL	EEEE:DL7T
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7V]	CRITICAL	EEEE:DL7V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7W]	CRITICAL	EEEE:DL7W
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Y]	CRITICAL	EEEE:DL7Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL80]	CRITICAL	EEEE:DL80

Programmables - All Builds

341S2830	1	IC,CPLD,LATTICE,GMUX,K91/K91F	U9600	CRITICAL	GMUX_PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2384	1	IR,ENCORE II,CY7C63833-LFXC	U4800	CRITICAL	IR_PROG
341S3129	1	IC,T29 EEPROM,PVT,K9x	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S3128	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,PVT,HVQFN25	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92,PROG	U8701	CRITICAL	GPUROM:PROG
335S0724	1	IC,GPU ROM,K91/F,K92,BLANK	U8701	CRITICAL	GPUROM:BLANK

SMC

338S0895	1	IC,SMC,HSB/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2854	1	IC,SMC,DEVELOPMENT-PROTO0,K91	U4900	CRITICAL	SMC_PROG:PROTO0
341S2935	1	IC,SMC,DEVELOPMENT-PROTO1,K91	U4900	CRITICAL	SMC_PROG:PROTO1
341S2994	1	IC,SMC,DEVELOPMENT-PROTO2,K91	U4900	CRITICAL	SMC_PROG:PROTO2
341S2861	1	IC,SMC,DEVELOPMENT-EVT,K91	U4900	CRITICAL	SMC_PROG:EVT
341S2864	1	IC,SMC,DEVELOPMENT-DVT,K91	U4900	CRITICAL	SMC_PROG:DVT
341S2867	1	IC,SMC,DEVELOPMENT-PVT,K91	U4900	CRITICAL	SMC_PROG:PVT

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST
- TRUE PP5V S0
- TRUE FAN LT PWM
- TRUE FAN LT TACH

3 TPs per Fan

J5660 (RIGHT FAN CONN)
- TRUE PP5V S0
- TRUE FAN RT PWM
- TRUE FAN RT TACH
- TRUE GND

2 TPs

5 TPs per Fan

J6780 (MIC CONN)
- TRUE BI MIC N
- TRUE BI MIC SHIELD
- TRUE BI MIC P

USB PORTS
- TRUE PP5V S3 RTUSB A F
- TRUE USB2 LT1 N
- TRUE USB2 LT1 P
- TRUE GND
- TRUE PP5V S3 RTUSB B F
- TRUE USB LT2 N
- TRUE USB LT2 P
- TRUE GND

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)
- TRUE PCIE AP D2R P
- TRUE PCIE AP D2R N
- TRUE PCIE AP R2D P
- TRUE PCIE AP R2D N
- TRUE PCIE CLK100M AP CONN_P
- TRUE PCIE CLK100M AP CONN_N
- TRUE AP CLKREQ Q L
- TRUE PCIE WAKE L
- TRUE WIFI EVENT L
- TRUE AP RESET CONN L
- TRUE PP3V3 WLAN
- TRUE PP5V S3 ALSCAMERA F
- TRUE SMBUS SMC A S3 SDA
- TRUE SMBUS SMC A S3 SCL
- TRUE USB CAMERA CONN P
- TRUE USB CAMERA CONN N
- TRUE CONN USB2 BT P
- TRUE CONN USB2 BT N
- TRUE SMBUS SMC 0 S0 SCL
- TRUE SMBUS SMC 0 S0 SDA

J5713 (KEY BOARD CONN)
- TRUE PP3V3 S3
- TRUE PP3V42 G3H
- TRUE WS KBD1
- TRUE WS KBD2
- TRUE WS KBD3
- TRUE WS KBD4
- TRUE WS KBD5
- TRUE WS KBD6
- TRUE WS KBD7
- TRUE WS KBD8
- TRUE WS KBD9
- TRUE WS KBD10
- TRUE WS KBD11
- TRUE WS KBD12
- TRUE WS KBD13
- TRUE WS KBD14
- TRUE WS KBD15 CAP
- TRUE WS KBD16 NUM
- TRUE WS KBD17
- TRUE WS KBD18
- TRUE WS KBD19
- TRUE WS KBD20
- TRUE WS KBD21
- TRUE WS KBD22
- TRUE WS KBD23
- TRUE WS KBD ONOFF L
- TRUE WS LEFT SHIFT KBD
- TRUE WS LEFT OPTION KBD
- TRUE WS CONTROL KBD

FUNC_TEST
- TRUE BKLT EN
- TRUE TP ISSP SCLK P1 1
- TRUE TP ISSP SDATA P1 0
- TRUE LCD BKLT PWM
- TRUE LPCPLUS GPIO
- TRUE LPCPLUS RESET L
- TRUE LPC AD<0..3>
- TRUE LPC CLK33M LPCPLUS
- TRUE LPC FRAME L
- TRUE LPC PWRDWN L
- TRUE LPC SERIRQ
- TRUE PM CLKRUN L
- TRUE PM SYSRST L
- TRUE SMC MD1
- TRUE SMC NMI
- TRUE SMC ONOFF L
- TRUE SMC RESET L
- TRUE SMC RX L
- TRUE SMC TCK
- TRUE SMC TDI
- TRUE SMC TDO
- TRUE SMC TMS
- TRUE SMC TRST L
- TRUE SMC TX L
- TRUE SPIROM USE MLB
- TRUE SPI ALT CLK
- TRUE SPI ALT CS L
- TRUE SPI ALT MISO
- TRUE SPI ALT MOSI
- TRUE SYS LED ANODE R

J6781 & J6782 (SPEAKERS CONN)
- TRUE SPKRCONN L OUT P
- TRUE SPKRCONN L OUT N
- TRUE SPKRCONN R OUT P
- TRUE SPKRCONN R OUT N
- TRUE SPKRCONN S OUT P
- TRUE SPKRCONN S OUT N

J9000 (LVDS CONN)
- TRUE PP3V3 SW LCD
- TRUE PP3V3 S0
- TRUE PPVOUT S0 LCDBKLT
- TRUE LVDS DDC CLK
- TRUE LVDS DDC DATA
- TRUE LVDS CONN A DATA P<0>
- TRUE LVDS CONN A DATA N<0>
- TRUE LVDS CONN A DATA P<1>
- TRUE LVDS CONN A DATA N<1>
- TRUE LVDS CONN A DATA P<2>
- TRUE LVDS CONN A DATA N<2>
- TRUE LVDS CONN A CLK F P
- TRUE LVDS CONN A CLK F N
- TRUE LVDS CONN B DATA P<0>
- TRUE LVDS CONN B DATA N<0>
- TRUE LVDS CONN B DATA P<1>
- TRUE LVDS CONN B DATA N<1>
- TRUE LVDS CONN B DATA P<2>
- TRUE LVDS CONN B DATA N<2>
- TRUE LVDS CONN B CLK F P
- TRUE LVDS CONN B CLK F N
- TRUE LED RETURN 1
- TRUE LED RETURN 2
- TRUE LED RETURN 3
- TRUE LED RETURN 4
- TRUE LED RETURN 5
- TRUE LED RETURN 6
- TRUE GND

2 TP needed

4 TPs

J4500 (SATA ODD CONN)
- TRUE PP5V SW ODD
- TRUE SMC ODD DETECT
- TRUE SATA ODD D2R C P
- TRUE SATA ODD D2R C N
- TRUE SATA ODD R2D P
- TRUE SATA ODD R2D N
- TRUE SATA ODD D2R UF P
- TRUE SATA ODD D2R UF N
- TRUE GND

3 TPs

J4501 (SATA HDD CONN)
- TRUE PP5V S0 HDD FLT
- TRUE SATA HDD R2D P
- TRUE SATA HDD R2D N
- TRUE SATA HDD D2R C N
- TRUE SATA HDD D2R C P
- TRUE GND

5 TPs

J5815 (KBD BACKLIGHT CONN)
- TRUE KBDLED ANODE
- TRUE SMC KDBLED PRESENT L
- TRUE GND

FUNC_TEST
- TRUE GND
- TRUE GND

6 TPs

J6950 (BAT CONN)
- TRUE SYS DETECT L

J6950 (BIL CABLE CONN)
- TRUE PP5V S3 IR R
- TRUE SMC LID R
- TRUE IR RX OUT
- TRUE SYS LED ANODE
- TRUE GND

J5800 (IPD FLEX CONN)
- TRUE PP18V5 S4
- TRUE Z2 HOST INTN
- TRUE Z2 MOSI
- TRUE Z2 CS L
- TRUE Z2 DEBUG3
- TRUE Z2 MISO
- TRUE Z2 BOOST EN
- TRUE Z2 SCLK
- TRUE Z2 CLKIN
- TRUE Z2 KEY ACT L
- TRUE Z2 RESET
- TRUE PSOC F CS L
- TRUE PICKB L
- TRUE PSOC MISO
- TRUE PSOC MOSI
- TRUE PSOC SCLK
- TRUE SMBUS SMC A S3 SCL
- TRUE SMBUS SMC A S3 SDA

J6900 (DC POWER CONN)
- TRUE ADAPTER SENSE
- TRUE PP18V5 DCIN FUSE
- TRUE GND

J6950 (MAIN BATT CONN)
- TRUE PPVBAT G3H CONN
- TRUE SMBUS SMC BSA SCL
- TRUE SMBUS SMC BSA SDA
- TRUE NC SMC BS ALRT L
- TRUE GND

J6995 (BAT LED CONN)
- TRUE PP3V42 G3H
- TRUE SMBUS SMC BSA SDA
- TRUE SMBUS SMC BSA SCL
- TRUE SMC BIL BUTTON L
- TRUE GND

POWER RAILS

FUNC_TEST
- TRUE PM SLP S3 L
- TRUE PP0V75 S0 DDRVTT
- TRUE PP18V5 S3
- TRUE PP1V05 S0
- TRUE PP1V05 S0GPU
- TRUE PP1V05 S5
- TRUE PP1V0 FW FWPHY
- TRUE PP1V2 ENET
- TRUE PP1V2 S0
- TRUE PP1V5 S3
- TRUE PP1V5_S3RS0
- TRUE PP1V8R1V55_S0GPU_ISNS
- TRUE PP1V8R1V55_S0GPU_ISNS_R
- TRUE PP1V8 GPUIFPX
- TRUE PP1V8 S0
- TRUE PP3V3 ENET
- TRUE PP3V3 FW FWPHY
- TRUE PP3V3 S0
- TRUE PP3V3 S0GPU
- TRUE PP3V3 S3
- TRUE PP3V3 S5 AVREF SMC
- TRUE PP3V42 G3H
- TRUE PP5V S0
- TRUE PP5V S3
- TRUE PP5V S5
- TRUE PPBUS G3H
- TRUE PPDCIN G3H
- TRUE PPVCORE GPU
- TRUE PPVCORE S0 CPU
- TRUE PPVCORE S0 GFX
- TRUE PPVP FW
- TRUE PPVTTDDR S3

NC NO_TESTS

NO_TEST
- TRUE TP FW643 NAND TREE
- TRUE TP FW643 OCR10 CTL
- TRUE TP FW643 SCIFCLK
- TRUE TP FW643 SCIFDAIN
- TRUE TP FW643 SCIFDOUT
- TRUE TP FW643 SCIFMC
- TRUE TP FW643 SDA
- TRUE TP FW643 SE
- TRUE TP FW643 SM
- TRUE TP FW643 FW620 L
- TRUE TP FW643 JASI EN
- TRUE DMI S2N N<1>
- TRUE DMI S2N P<1>
- TRUE FDI DATA N<1>
- TRUE FDI DATA P<1>
- TRUE FDI FSYNC<1..0>
- TRUE FDI LSYNC<1..0>
- TRUE FDI INT
- TRUE TP FW643 VAUX ENABLE
- TRUE TP FW643 VBUF
- TRUE TP FW643 TCK
- TRUE TP FW643 TDO
- TRUE TP FW643 TMS
- TRUE TP SMC P10
- TRUE TP P7 7
- TRUE TP PSOC SCL
- TRUE TP PSOC SDA
- TRUE TP SMC P24
- TRUE DC TEST BH1 BG2
- TRUE DC TEST BH3 BJ2
- TRUE TP USB HUB1 OCS1
- TRUE TP USB HUB1 PRTPWR1
- TRUE TP USB HUB2 OCS1
- TRUE TP USB HUB2 PRTPWR1
- TRUE TP DC TEST A62
- TRUE TP DC TEST D65
- TRUE TP SMC PF5

NO_TEST=TRUE

NO_TEST
- TRUE T29 D2R P<1..0>
- TRUE T29 D2R N<1..0>
- TRUE T29 D2R C P<1..0>
- TRUE T29 D2R C N<1..0>
- TRUE T29 R2D C N<1..0>
- TRUE T29 R2D P<1..0>
- TRUE T29 R2D N<1..0>
- TRUE T29DPA ML P<3..0>
- TRUE T29DPA ML N<3..0>
- TRUE DP T29SNK0 AUXCH C P
- TRUE DP T29SNK0 AUXCH C N
- TRUE DP T29SNK0 AUXCH P
- TRUE DP T29SNK0 AUXCH N
- TRUE DP T29SNK0 ML C P<3..0>
- TRUE DP T29SNK0 ML C N<3..0>
- TRUE DP T29SNK0 ML P<3..0>
- TRUE DP T29SNK0 ML N<3..0>
- TRUE DP T29SNK1 AUXCH C P
- TRUE DP T29SNK1 AUXCH C N
- TRUE DP T29SNK1 AUXCH P
- TRUE DP T29SNK1 AUXCH N
- TRUE DP T29SNK1 ML C P<3..0>
- TRUE DP T29SNK1 ML C N<3..0>
- TRUE DP T29SNK1 ML P<3..0>
- TRUE DP T29SNK1 ML N<3..0>
- TRUE TP DP T29SRC AUXCH CN
- TRUE TP DP T29SRC AUXCH CP
- TRUE TP DP T29SRC ML CP<3..0>
- TRUE TP DP T29SRC ML CN<3..0>
- TRUE DP SDRVA ML C P<0>
- TRUE DP SDRVA ML C N<0>
- TRUE DP SDRVA ML C P<2>
- TRUE DP SDRVA ML C N<2>
- TRUE DP SDRVA ML P<0>
- TRUE DP SDRVA ML N<0>
- TRUE DP SDRVA ML P<2>
- TRUE DP SDRVA ML N<2>
- TRUE TP T29 PCIE RESET0 L
- TRUE TP T29 PCIE RESET1 L
- TRUE TP T29 PCIE RESET2 L
- TRUE TP T29 PCIE RESET3 L
- TRUE T29DPA D2R1 AUXCH N
- TRUE T29DPA D2R1 AUXCH P
- TRUE T29 D2R1 BIAS

ICT Test Points

CPU NO_TESTS

NO_TEST
- TP CPU RSVD<65..62> — TRUE — NC TP CPU RSVD<65..62>
- TP CPU RSVD<58..45> — TRUE — NC TP CPU RSVD<58..45>
- TP CPU RSVD<43..32> — TRUE — NC TP CPU RSVD<43..32>
- TP CPU RSVD<27..26> — TRUE — NC TP CPU RSVD<27..26>
- TP CPU RSVD<24..15> — TRUE — NC TP CPU RSVD<24..15>
- TP CPU RSVD<2..1> — TRUE — NC TP CPU RSVD<2..1>
- TP CPU RSVD NCTF<8..5> — TRUE — NC TP CPU RSVD NCTF<8..5>

(all: MAKE_BASE=TRUE)

NC NO_TESTS

NO_TEST
- NC CRT IG BLUE — TRUE — NC CRT IG BLUE
- NC CRT IG GREEN — TRUE — NC CRT IG GREEN
- NC CRT IG RED — TRUE — NC CRT IG RED
- NC CRT IG DDC CLK — TRUE — NC CRT IG DDC CLK
- NC CRT IG DDC DATA — TRUE — NC CRT IG DDC DATA
- NC CRT IG HSYNC — TRUE — NC CRT IG HSYNC
- NC CRT IG VSYNC — TRUE — NC CRT IG VSYNC
- NC LVDS IG CTRL CLK — TRUE — NC LVDS IG CTRL CLK
- NC LVDS IG CTRL DATA — TRUE — NC LVDS IG CTRL DATA
- NC PCH LVDS VBG — TRUE — NC PCH LVDS VBG
- NC HDA SDIN1 — TRUE — NC HDA SDIN1
- NC HDA SDIN2 — TRUE — NC HDA SDIN2
- NC HDA SDIN3 — TRUE — NC HDA SDIN3

(all: MAKE_BASE=TRUE)

NC NO_TESTS

NO_TEST
- TP AUD GPIO 2
- TP AUD GPIO 1
- TP AUD LO1 L N
- TP AUD LO1 L P
- TP BKL FAULT
- TP SPI DESCRIPTOR OVERRIDE L
- TP XDPPCH HOOK2
- TP XDPPCH HOOK3
- TP GMUX PL6B
- TP PM RSMRST L
- TP CPUIMVP BOOT1
- TP CPUIMVP BOOT2
- TP CPUIMVP UGATE2
- TP 1V05 S0 PCH VCCAPLLEXP

NC NO_TESTS

NO_TEST
- NC FW643 AVREG — TRUE — NC FW643 AVREG
- NC FW643 TDI — TRUE — NC FW643 TDI
- NC DP IG C HPD — TRUE — NC DP IG C HPD
- NC DP IG C CTRL CLK — TRUE — NC DP IG C CTRL CLK
- NC DP IG C CTRL DATA — TRUE — NC DP IG C CTRL DATA
- TP DP IG C MLP<3..0> — TRUE — NC DP IG C MLP<3..0>
- TP DP IG C MLN<3..0> — TRUE — NC DP IG C MLN<3..0>
- NC DP IG C AUXP — TRUE — NC DP IG C AUXP
- NC DP IG C AUXN — TRUE — NC DP IG C AUXN
- NC DP IG D HPD — TRUE — NC DP IG D HPD
- NC DP IG D CTRL CLK — TRUE — NC DP IG D CTRL CLK
- NC DP IG D CTRL DATA — TRUE — NC DP IG D CTRL DATA
- TP DP IG D MLP<3..0> — TRUE — NC DP IG D MLP<3..0>
- TP DP IG D MLN<3..0> — TRUE — NC DP IG D MLN<3..0>
- NC DP IG D AUXP — TRUE — NC DP IG D AUXP
- NC DP IG D AUXN — TRUE — NC DP IG D AUXN
- NC SDVO TVCLKINN — TRUE — NC SDVO TVCLKINN
- NC SDVO TVCLKINP — TRUE — NC SDVO TVCLKINP
- NC SDVO STALLN — TRUE — NC SDVO STALLN
- NC SDVO STALLP — TRUE — NC SDVO STALLP
- NC SDVO INTN — TRUE — NC SDVO INTN
- NC SDVO INTP — TRUE — NC SDVO INTP
- NC GPU BUFRST L — TRUE — NC GPU BUFRST L
- TP GPU GSTATE<0> — TRUE — NC GPU GSTATE<0>
- NC GPU GSTATE<1> — TRUE — NC GPU GSTATE<1>
- TP GPU MIOA D<9..0> — TRUE — NC GPU MIOA D<9..0>
- NC GPU MIOA DE — TRUE — NC GPU MIOA DE
- NC LVDS EG BKL PWM — TRUE — NC LVDS EG BKL PWM
- TP LVDS IG B CLKN — TRUE — NC LVDS IG B CLKN
- TP LVDS IG B CLKP — TRUE — NC LVDS IG B CLKP
- TP LVDS IG BKL PWM — TRUE — NC LVDS IG BKL PWM
- NC SMC BS ALRT L — TRUE — NC SMC BS ALRT L
- NC PCI PME L — TRUE — NC PCI PME L
- NC PCI CLK33M OUT3 — TRUE — NC PCI CLK33M OUT3
- NC PCIE CLK100M PE4N — TRUE — NC PCIE CLK100M PE4N
- NC PCIE CLK100M PE4P — TRUE — NC PCIE CLK100M PE4P
- NC PCIE CLK100M PE5N — TRUE — NC PCIE CLK100M PE5N
- NC PCIE CLK100M PE5P — TRUE — NC PCIE CLK100M PE5P
- NC PCIE CLK100M PE6N — TRUE — NC PCIE CLK100M PE6N
- NC PCIE CLK100M PE6P — TRUE — NC PCIE CLK100M PE6P
- NC PCIE CLK100M PE7N — TRUE — NC PCIE CLK100M PE7N
- NC PCIE CLK100M PE7P — TRUE — NC PCIE CLK100M PE7P
- NC PSOC P1 3 — TRUE — NC PSOC P1 3
- NC SATA B D2RN — TRUE — NC SATA B D2RN
- NC SATA B D2RP — TRUE — NC SATA B D2RP
- NC SATA B R2D CN — TRUE — NC SATA B R2D CN
- NC SATA B R2D CP — TRUE — NC SATA B R2D CP
- NC SATA D D2RN — TRUE — NC SATA D D2RN
- NC SATA D D2RP — TRUE — NC SATA D D2RP
- NC SATA D R2D CN — TRUE — NC SATA D R2D CN
- NC SATA D R2D CP — TRUE — NC SATA D R2D CP
- NC SATA E D2RN — TRUE — NC SATA E D2RN
- NC SATA E D2RP — TRUE — NC SATA E D2RP
- NC SATA E R2D CN — TRUE — NC SATA E R2D CN
- NC SATA E R2D CP — TRUE — NC SATA E R2D CP
- NC SATA F D2RN — TRUE — NC SATA F D2RN
- NC SATA F D2RP — TRUE — NC SATA F D2RP
- NC SATA F R2D CN — TRUE — NC SATA F R2D CN
- NC SATA F R2D CP — TRUE — NC SATA F R2D CP

(all: MAKE_BASE=TRUE)

NC NO_TESTS

NO_TEST
- MEM A BA<2..0>
- MEM A CKE<1..0>
- MEM A CLK N<1..0>
- MEM A CLK P<1..0>
- MEM A CS L<1..0>
- MEM A ODT<1..0>
- MEM A SA<1..0>
- MEM A DQ<63..0>
- MEM A DQS N<7..0>
- MEM A DQS P<7..0>
- FB A0 DQ<31..0>
- FB A0 A<8..0>
- FB A0 ABI L
- FB A0 EDC<3..0>
- FB A0 WCLK N<1..0>
- FB A0 WCLK P<1..0>
- FB A0 DBI L<3..0>
- FB A1 DQ<31..0>
- FB A1 A<8..0>
- FB A1 ABI L
- FB A1 EDC<3..0>
- FB A1 WCLK N<1..0>
- FB A1 WCLK P<1..0>
- FB A1 DBI L<3..0>
- MEM A A<15..0>
- MEM A CAS L
- MEM A RAS L
- MEM A WE L
- MEM B A<15..0>
- MEM B CAS L
- MEM B RAS L
- MEM B WE L
- MEM B BA<2..0>
- MEM B CKE<1..0>
- MEM B CLK N<1..0>
- MEM B CLK P<1..0>
- MEM B CS L<1..0>
- MEM B ODT<1..0>
- MEM B SA<1..0>
- MEM B DQ<63..0>
- MEM B DQS N<7..0>
- MEM B DQS P<7..0>
- FB B0 DQ<31..0>
- FB B0 A<8..0>
- FB B0 ABI L
- FB B0 EDC<3..0>
- FB B0 WCLK N<1..0>
- FB B0 WCLK P<1..0>
- FB B0 DBI L<3..0>
- FB B1 DQ<31..0>
- FB B1 A<8..0>
- FB B1 ABI L
- FB B1 EDC<3..0>
- FB B1 WCLK N<1..0>
- FB B1 WCLK P<1..0>
- FB B1 DBI L<3..0>

(all: TRUE — MAKE_BASE=TRUE)

NC NO_TESTS

NO_TEST
- NC FW643 TACH — TRUE — NC SMC FAN 3 TACH
- NC SMC FAN 3 CTL — TRUE — NC SMC FAN 3 CTL
- NC SMC FAN 2 TACH — TRUE — NC SMC FAN 2 TACH
- NC SMC FAN 2 CTL — TRUE — NC SMC FAN 2 CTL
- NC FW2 TPBP — TRUE — NC FW2 TPBP
- NC FW2 TPBN — TRUE — NC FW2 TPBN
- NC FW2 TPBIAS — TRUE — NC FW2 TPBIAS
- NC FW2 TPAP — TRUE — NC FW2 TPAP
- NC FW2 TPAN — TRUE — NC FW2 TPAN
- NC FW0 TPBP — TRUE — NC FW0 TPBP
- NC FW0 TPBN — TRUE — NC FW0 TPBN
- NC FW0 TPAP — TRUE — NC FW0 TPAP
- NC ESTARLDO EN — TRUE — NC ESTARLDO EN
- NC ALS GAIN — TRUE — NC ALS GAIN

(all: MAKE_BASE=TRUE)

PCH ALIASES

- TP SMC P41 — TRUE — NC SMC P41
- NC LPC DREQ0 0 L — NC LPC DREQ0 L
- NC CLINK CLK — TRUE — NC CLINK CLK
- NC CLINK DATA — TRUE — NC CLINK DATA
- NC CLINK RESET L — TRUE — NC CLINK RESET L
- NC PCIE CLK100M PEBN — TRUE — NC PCIE CLK100M PEBN
- NC PCIE CLK100M PEBP — TRUE — NC PCIE CLK100M PEBP

(all: MAKE_BASE=TRUE)

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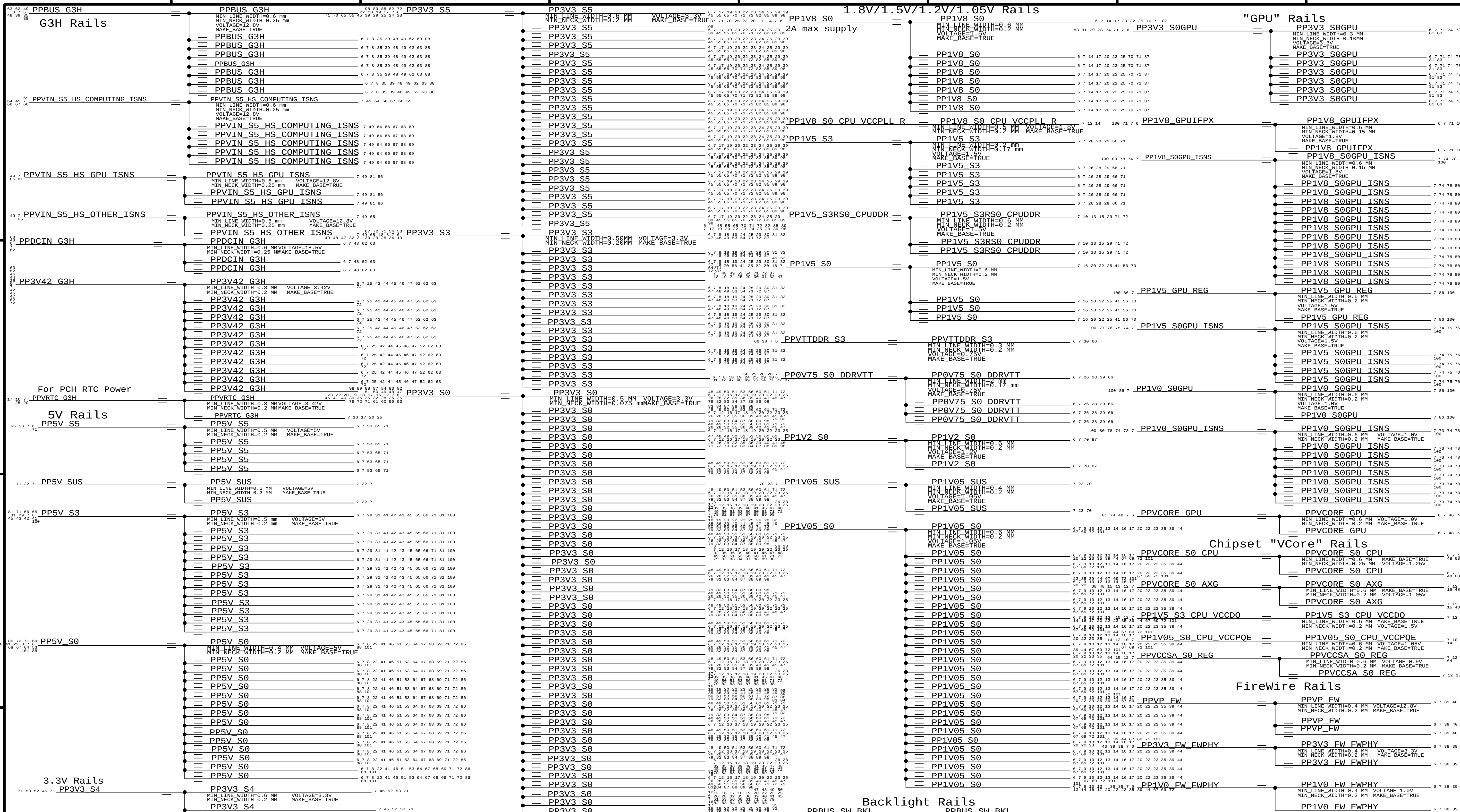

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Thermal Module Holes

ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH

Fan Holes

ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND
ZT0940 3R2P5 — GND
ZT0950 TH — GND — SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 — GND
ZT0990 3R2P5 — GND

Left Speaker Holes

ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH

Keyboard / IPD Conn Protect

ZT0952 4.0OD1.85H-M1.6X0.35
ZT0953 4.0OD1.85H-M1.6X0.35

Tall EMI pogo pins

SH0902 POGO-2.0OD-3.5H-K86-K87
SH0900 POGO-2.0OD-3.5H-K86-K87
SH0903 POGO-2.0OD-3.5H-K86-K87
SH0916 POGO-2.0OD-3.5H-K86-K87
SH0904 POGO-2.0OD-3.5H-K86-K87

Short (IO Row) EMI pogo pins

SH0911 1.4DIA-SHORT-SILVER-K99
SH0910 1.4DIA-SHORT-SILVER-K99
SH0913 1.4DIA-SHORT-SILVER-K99
SH0912 1.4DIA-SHORT-SILVER-K99
SH0917 1.4DIA-SHORT-SILVER-K99
SH0901 1.4DIA-SHORT-SILVER-K99
SH0914 1.4DIA-SHORT-SILVER-K99 — GND_CHASSIS_AUDIO_JACK

Heat spreader mounting boss for T29 router

SH0920 STDOFF-4.0OD1.85H-SM
SH0923 STDOFF-4.0OD1.85H-SM

Heat spreader mounting boss for PCH

SH0921 STDOFF-4.0OD2.23H-SM
SH0922 STDOFF-4.0OD2.23H-SM

T29 / GMUX JTAG Signals

JTAG_ISP_TCK — JTAG_ISP_TCK
JTAG_ISP_TDI — JTAG_ISP_TDI
JTAG_ISP_TDO — JTAG_ISP_TDO
T29_LSEO_LSOE3 — T29_LSEO_LSOE3
T29_LSEO_LSOE2 — T29_LSEO_LSOE2

GMUX ALIASES

PM_ALL_GPU_PGOOD — PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG — TP_LVDS_MUX_SEL_EG
EG_RESET_L — EG_RESET_L
LVDS_IG_BKL_ON — LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR — LVDS_IG_PANEL_PWR
PPVOUT_S0_LCDBKLT — PPVOUT_S0_LCDBKLT
GMUX_VSYNC — GMUX_VSYNC
PEX_CLKREQ_L — PEX_CLKREQ_L
PEG_CLKREQ_L — PEG_CLKREQ_L
PM_ENET_EN — PM_ENET_EN

FW_PLUG_DET_L — FW_PLUG_DET_L
FW643_WAKE_L — FW643_WAKE_L
TP_SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN
NC_PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2R_N
NC_PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2R_P
NC_PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_C_N
NC_PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_C_P

R0921 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_P0 — C0901 0.01UF 10% 10V X5R 201
R0922 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_N0 — C0902 0.01UF 10% 10V X5R 201
R0923 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_P1 — C0903 0.01UF 10% 10V X5R 201
R0924 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_N1 — C0904 0.01UF 10% 10V X5R 201

NC_PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARD_P
NC_PEG_B_CLKRQ_L_GPIO56 — NC_PEG_B_CLKRQ_L_GPIO56
NC_PCIECLKRQ4_L_GPIO26 — NC_PCIECLKRQ4_L_GPIO26
TP_ISSP_SCLK_P1_1 — TP_ISSP_SCLK_P1_1
TP_ISSP_SDATA_P1_0 — TP_ISSP_SDATA_P1_0

GND
GND
GND
GND
GND

NC_PCH_CLKOUT_DPN — NC_PCH_CLKOUT_DPN
NC_PCH_CLKOUT_DPP — NC_PCH_CLKOUT_DPP
NC_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3

NC_FSB_CLK133M_PCHP — NC_FSB_CLK133M_PCHP
NC_FSB_CLK133M_PCHN — NC_FSB_CLK133M_PCHN
NC_LT_GAIN_TP — NC_LT_GAIN_TP
NC_RT_GAIN_TP — NC_RT_GAIN_TP
NC_SW_GAIN_TP — NC_SW_GAIN_TP

PP5V_S0 — XW0901 — PP5V_S0_AUDIO — XW0902 — PP5V_S0_AUDIO_AMP_L — XW0903 — PP5V_S0_AUDIO_AMP_R

CPU signals

CPU_VID<0..6> — CPUIMVP_VID<0..6>
GFX_VID<0..6> — GFXIMVP_VID<0..6>
MEMVTT_EN — MEMVTT_EN

Unused PEG signals

NC_PEG_D2R_P<15..12> — =PEG_D2R_P<15..12>
NC_PEG_D2R_N<15..12> — =PEG_D2R_N<15..12>
NC_PEG_R2D_C_P<15..12> — =PEG_R2D_C_P<15..12>
NC_PEG_R2D_C_N<15..12> — =PEG_R2D_C_N<15..12>

T29 Signals Through PEG

PCIE_T29_D2R_P<3..0> — =PEG_D2R_P<11..8>
PCIE_T29_D2R_N<3..0> — =PEG_D2R_N<11..8>
PCIE_T29_R2D_C_P<3..0> — =PEG_R2D_C_P<11..8>
PCIE_T29_R2D_C_N<3..0> — =PEG_R2D_C_N<11..8>

GPU signals

PEG_D2R_P<7..0> — =PEG_D2R_P<7..0>
PEG_D2R_N<7..0> — =PEG_D2R_N<7..0>
PEG_R2D_C_P<7..0> — =PEG_R2D_C_P<7..0>
PEG_R2D_C_N<7..0> — =PEG_R2D_C_N<7..0>

Unused T29 Ports

T29_D2R_P<3..2> — NC_T29_D2RP<3..2>
T29_D2R_N<3..2> — NC_T29_D2RN<3..2>
T29_R2D_C_P<3..2> — NC_T29_R2D_CP<3..2>
T29_R2D_C_N<3..2> — NC_T29_R2D_CN<3..2>

DP_EG_AUXCH_N — DP_EG_AUXCH_N
DP_EG_AUXCH_P — DP_EG_AUXCH_P
NC_DPB_EG_AUX_CHN — NC_DPB_EG_AUX_CHN
NC_DPB_EG_AUX_CHP — NC_DPB_EG_AUX_CHP
NC_DPB_EG_DDC_CLK — NC_DPB_EG_DDC_CLK
NC_DPB_EG_DDC_DATA — NC_DPB_EG_DDC_DATA
NC_DPB_EG_MLN<3..0> — DPB_EG_ML_N<3..0>
NC_DPB_EG_MLP<3..0> — DPB_EG_ML_P<3..0>

LCD_BKLT_EN — R0901 4.7K 5% 1/16W MF-LF 402

T29BST:N — R0950 0 5% 1/8W MF-LF 805 — PPBUS_G3H — PP15V_T29

TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM — TP_LVDS_IG_BKL_PWM
NC_GPU_XTALOUT — NC_GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3>

NC_USB_HUB1_OCS4 — NC_USB_HUB1_OCS4
NC_USB_HUB2_OCS4 — NC_USB_HUB2_OCS4

PP3V3_S3
NOSTUFF R0903 10K 5% 1/16W MF-LF 402 — R0904 10K 5% 1/16W MF-LF 402 — USB_EXTC_N — USB_EXTC_P

PP3V3_S3
NOSTUFF R0913 10K 5% 1/16W MF-LF 402 — R0914 10K 5% 1/16W MF-LF 402 — USB_SDCARD_P — USB_SDCARD_N

PP3V3_S3
R0915 10K 5% 1/16W MF-LF 402 — R0916 10K 5% 1/16W MF-LF 402 — USB_T29A_N — USB_T29A_P

R0926 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_D2R_P1 — C0906 0.01UF 10% 10V X5R 201
R0927 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_D2R_N1 — C0907 0.01UF 10% 10V X5R 201

DP_A_BIAS2 — C0905 0.01UF 10% 10V X5R 201
DP_A_BIAS0 — C0908 0.01UF 10% 10V X5R 201

NC_DP_IG_MLP<3..0> — TP_DP_IG_B_MLP<3..0>
NC_DP_IG_MLN<3..0> — TP_DP_IG_B_MLN<3..0>
DP_IG_AUX_CH_P — DP_IG_AUX_CH_P
DP_IG_AUX_CH_N — DP_IG_AUX_CH_N
DP_IG_DDC_CLK — DP_IG_DDC_CLK
DP_IG_DDC_DATA — DP_IG_DDC_DATA
DP_IG_HPD — DP_IG_HPD

GND — MIN_LINE_WIDTH=0.6 mm — MIN_NECK_WIDTH=0.095 mm — VOLTAGE=0V

Digital Ground

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: Signal Aliases

Apple Inc.

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BRANCH:
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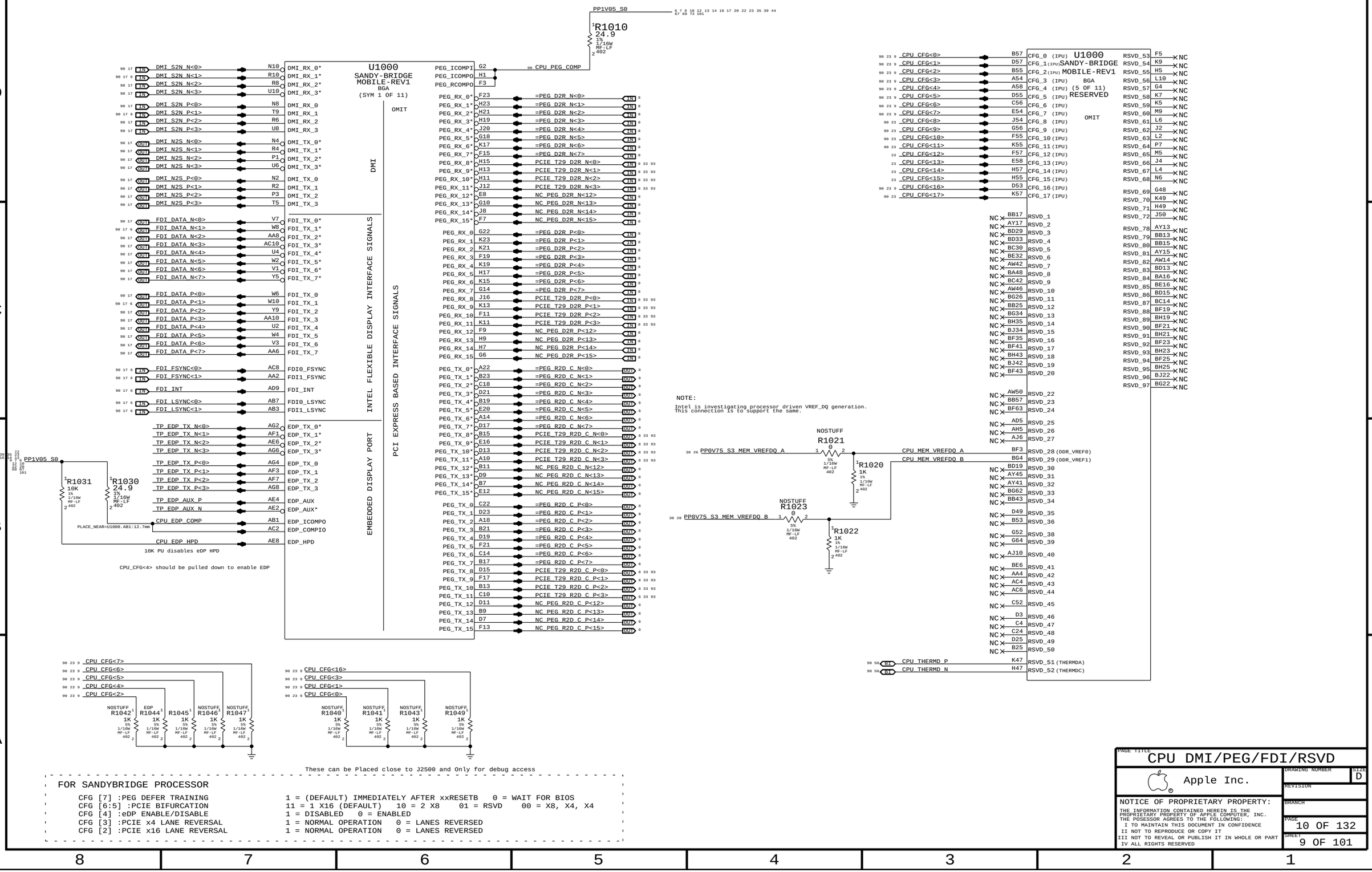
U1000
SANDY-BRIDGE
MOBILE-REV1
BGA
(SYM 1 OF 11)
OMIT
DMI
INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS
PCI EXPRESS BASED INTERFACE SIGNALS
EMBEDDED DISPLAY PORT
DMI_RX_0* N10
DMI_RX_1* R10
DMI_RX_2* R8
DMI_RX_3* U10
DMI_TX_0* N4
DMI_TX_1* R4
DMI_TX_2* P1
DMI_TX_3* U6
FDI_TX_0* V7
FDI_TX_1* W8
FDI_TX_2* AA8
FDI_TX_3* AC10
FDI_TX_4* U4
FDI_TX_5* W2
FDI_TX_6* V1
FDI_TX_7* Y5
FDI_TX_0 W6
FDI_TX_1 W10
FDI_TX_2 Y9
FDI_TX_3 AA10
FDI_TX_4 U2
FDI_TX_5 W4
FDI_TX_6 V3
FDI_TX_7 AA6
FDI0_FSYNC AC8
FDI1_FSYNC AA2
FDI_INT AD9
FDI0_LSYNC AB7
FDI1_LSYNC AB3
EDP_TX_0* AG2
EDP_TX_1* AF1
EDP_TX_2* AE6
EDP_TX_3* AG6
EDP_TX_0 AG4
EDP_TX_1 AF3
EDP_TX_2 AF7
EDP_TX_3 AG8
EDP_AUX AE4
EDP_AUX* AE2
EDP_ICOMPO AB1
EDP_COMPIO AC2
EDP_HPD AE8
PEG_ICOMPI G2
PEG_ICOMPO H1
PEG_RCOMPO F3
PEG_RX_0* F23
PEG_RX_1* H23
PEG_RX_2* H21
PEG_RX_3* H19
PEG_RX_4* J20
PEG_RX_5* G18
PEG_RX_6* K17
PEG_RX_7* F15
PEG_RX_8* H15
PEG_RX_9* H13
PEG_RX_10* H11
PEG_RX_11* J12
PEG_RX_12* E8
PEG_RX_13* G10
PEG_RX_14* J8
PEG_RX_15* F7
PEG_RX_0 G22
PEG_RX_1 K23
PEG_RX_2 K21
PEG_RX_3 F19
PEG_RX_4 K19
PEG_RX_5 H17
PEG_RX_6 K15
PEG_RX_7 G14
PEG_RX_8 J16
PEG_RX_9 K13
PEG_RX_10 F11
PEG_RX_11 K11
PEG_RX_12 F9
PEG_RX_13 H9
PEG_RX_14 H7
PEG_RX_15 G6
PEG_TX_0* A22
PEG_TX_1* B23
PEG_TX_2* C18
PEG_TX_3* D21
PEG_TX_4* B19
PEG_TX_5* E20
PEG_TX_6* A14
PEG_TX_7* D17
PEG_TX_8* B15
PEG_TX_9* E16
PEG_TX_10* D13
PEG_TX_11* A10
PEG_TX_12* B11
PEG_TX_13* D9
PEG_TX_14* B7
PEG_TX_15* E12
PEG_TX_0 C22
PEG_TX_1 D23
PEG_TX_2 A18
PEG_TX_3 B21
PEG_TX_4 D19
PEG_TX_5 F21
PEG_TX_6 C14
PEG_TX_7 B17
PEG_TX_8 D15
PEG_TX_9 F17
PEG_TX_10 B13
PEG_TX_11 C10
PEG_TX_12 D11
PEG_TX_13 B9
PEG_TX_14 D7
PEG_TX_15 F13
PP1V05_S0
R1010 24.9 1% 1/10W MF-LF 402
CPU_PEG_COMP
=PEG_D2R_N<0>
=PEG_D2R_N<1>
=PEG_D2R_N<2>
=PEG_D2R_N<3>
=PEG_D2R_N<4>
=PEG_D2R_N<5>
=PEG_D2R_N<6>
=PEG_D2R_N<7>
PCIE_T29_D2R_N<0>
PCIE_T29_D2R_N<1>
PCIE_T29_D2R_N<2>
PCIE_T29_D2R_N<3>
NC_PEG_D2R_N<12>
NC_PEG_D2R_N<13>
NC_PEG_D2R_N<14>
NC_PEG_D2R_N<15>
=PEG_D2R_P<0>
=PEG_D2R_P<1>
=PEG_D2R_P<2>
=PEG_D2R_P<3>
=PEG_D2R_P<4>
=PEG_D2R_P<5>
=PEG_D2R_P<6>
=PEG_D2R_P<7>
PCIE_T29_D2R_P<0>
PCIE_T29_D2R_P<1>
PCIE_T29_D2R_P<2>
PCIE_T29_D2R_P<3>
NC_PEG_D2R_P<12>
NC_PEG_D2R_P<13>
NC_PEG_D2R_P<14>
NC_PEG_D2R_P<15>
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=PEG_R2D_C_N<4>
=PEG_R2D_C_N<5>
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PCIE_T29_R2D_C_N<0>
PCIE_T29_R2D_C_N<1>
PCIE_T29_R2D_C_N<2>
PCIE_T29_R2D_C_N<3>
NC_PEG_R2D_C_N<12>
NC_PEG_R2D_C_N<13>
NC_PEG_R2D_C_N<14>
NC_PEG_R2D_C_N<15>
=PEG_R2D_C_P<0>
=PEG_R2D_C_P<1>
=PEG_R2D_C_P<2>
=PEG_R2D_C_P<3>
=PEG_R2D_C_P<4>
=PEG_R2D_C_P<5>
=PEG_R2D_C_P<6>
=PEG_R2D_C_P<7>
PCIE_T29_R2D_C_P<0>
PCIE_T29_R2D_C_P<1>
PCIE_T29_R2D_C_P<2>
PCIE_T29_R2D_C_P<3>
NC_PEG_R2D_C_P<12>
NC_PEG_R2D_C_P<13>
NC_PEG_R2D_C_P<14>
NC_PEG_R2D_C_P<15>
NOTE:
Intel is investigating processor driven VREF_DQ generation.
This connection is to support the same.
NOSTUFF R1021 0 5% 1/16W MF-LF 402
R1020 1K 1% 1/16W MF-LF 402
NOSTUFF R1023 0 5% 1/16W MF-LF 402
R1022 1K 1% 1/16W MF-LF 402
PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFDQ_B
CPU_MEM_VREFDQ_A
CPU_MEM_VREFDQ_B
U1000
SANDY-BRIDGE
MOBILE-REV1
BGA
(5 OF 11)
RESERVED
OMIT
CFG_0 (IPU) B57
CFG_1 (IPU) D57
CFG_2 (IPU) B55
CFG_3 (IPU) A54
CFG_4 (IPU) A58
CFG_5 (IPU) D55
CFG_6 (IPU) C56
CFG_7 (IPU) E54
CFG_8 (IPU) J54
CFG_9 (IPU) G56
CFG_10 (IPU) F55
CFG_11 (IPU) K55
CFG_12 (IPU) F57
CFG_13 (IPU) E58
CFG_14 (IPU) H57
CFG_15 (IPU) H55
CFG_16 (IPU) D53
CFG_17 (IPU) K57
RSVD_1 BB17
RSVD_2 AY17
RSVD_3 BD29
RSVD_4 BD33
RSVD_5 BC30
RSVD_6 BE32
RSVD_7 AW42
RSVD_8 BA48
RSVD_9 BC42
RSVD_10 AW46
RSVD_11 BG26
RSVD_12 BB25
RSVD_13 BG34
RSVD_14 BH35
RSVD_15 BJ34
RSVD_16 BF35
RSVD_17 BF41
RSVD_18 BH43
RSVD_19 BJ42
RSVD_20 BF43
RSVD_22 AW50
RSVD_23 BB57
RSVD_24 BF63
RSVD_25 AD5
RSVD_26 AH5
RSVD_27 AJ6
RSVD_28 (DDR_VREF0) BF3
RSVD_29 (DDR_VREF1) BG4
RSVD_30 BD19
RSVD_31 AY45
RSVD_32 AY41
RSVD_33 BG62
RSVD_34 BB43
RSVD_35 D49
RSVD_36 B53
RSVD_38 G52
RSVD_39 G64
RSVD_40 AJ10
RSVD_41 BE6
RSVD_42 AA4
RSVD_43 AC4
RSVD_44 AC6
RSVD_45 C52
RSVD_46 D3
RSVD_47 C4
RSVD_48 C24
RSVD_49 D25
RSVD_50 B25
RSVD_51 (THERMDA) K47
RSVD_52 (THERMDC) H47
RSVD_53 F5
RSVD_54 K9
RSVD_55 H5
RSVD_56 L10
RSVD_57 G4
RSVD_58 K7
RSVD_59 K5
RSVD_60 M9
RSVD_61 L6
RSVD_62 J2
RSVD_63 L2
RSVD_64 P7
RSVD_65 M5
RSVD_66 J4
RSVD_67 L4
RSVD_68 N6
RSVD_69 G48
RSVD_70 K49
RSVD_71 H49
RSVD_72 J50
RSVD_78 AY13
RSVD_79 BB13
RSVD_80 BB15
RSVD_81 AY15
RSVD_82 AW14
RSVD_83 BD13
RSVD_84 BA16
RSVD_85 BE16
RSVD_86 BD15
RSVD_87 BC14
RSVD_88 BF19
RSVD_89 BH19
RSVD_90 BF21
RSVD_91 BH21
RSVD_92 BF23
RSVD_93 BH23
RSVD_94 BF25
RSVD_95 BH25
RSVD_96 BJ22
RSVD_97 BG22
PP1V05_S0
R1031 10K 1% 1/16W MF-LF 402
R1030 24.9 1% 1/16W MF-LF 402
PLACE_NEAR=U1000.AB1:12.7mm
10K PU disables eDP HPD
CPU_EDP_HPD
CPU_CFG<4> should be pulled down to enable EDP
CPU_CFG<7>
CPU_CFG<6>
CPU_CFG<5>
CPU_CFG<4>
CPU_CFG<2>
NOSTUFF R1042 1K
EDP R1044 1K
R1045 1K
NOSTUFF R1046 1K
NOSTUFF R1047 1K
CPU_CFG<16>
CPU_CFG<3>
CPU_CFG<1>
CPU_CFG<0>
NOSTUFF R1040 1K
NOSTUFF R1041 1K
NOSTUFF R1043 1K
NOSTUFF R1049 1K
These can be Placed close to J2500 and Only for debug access
FOR SANDYBRIDGE PROCESSOR
CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
PAGE TITLE
CPU DMI/PEG/FDI/RSVD
Apple Inc.
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SIZE D
REVISION
BRANCH
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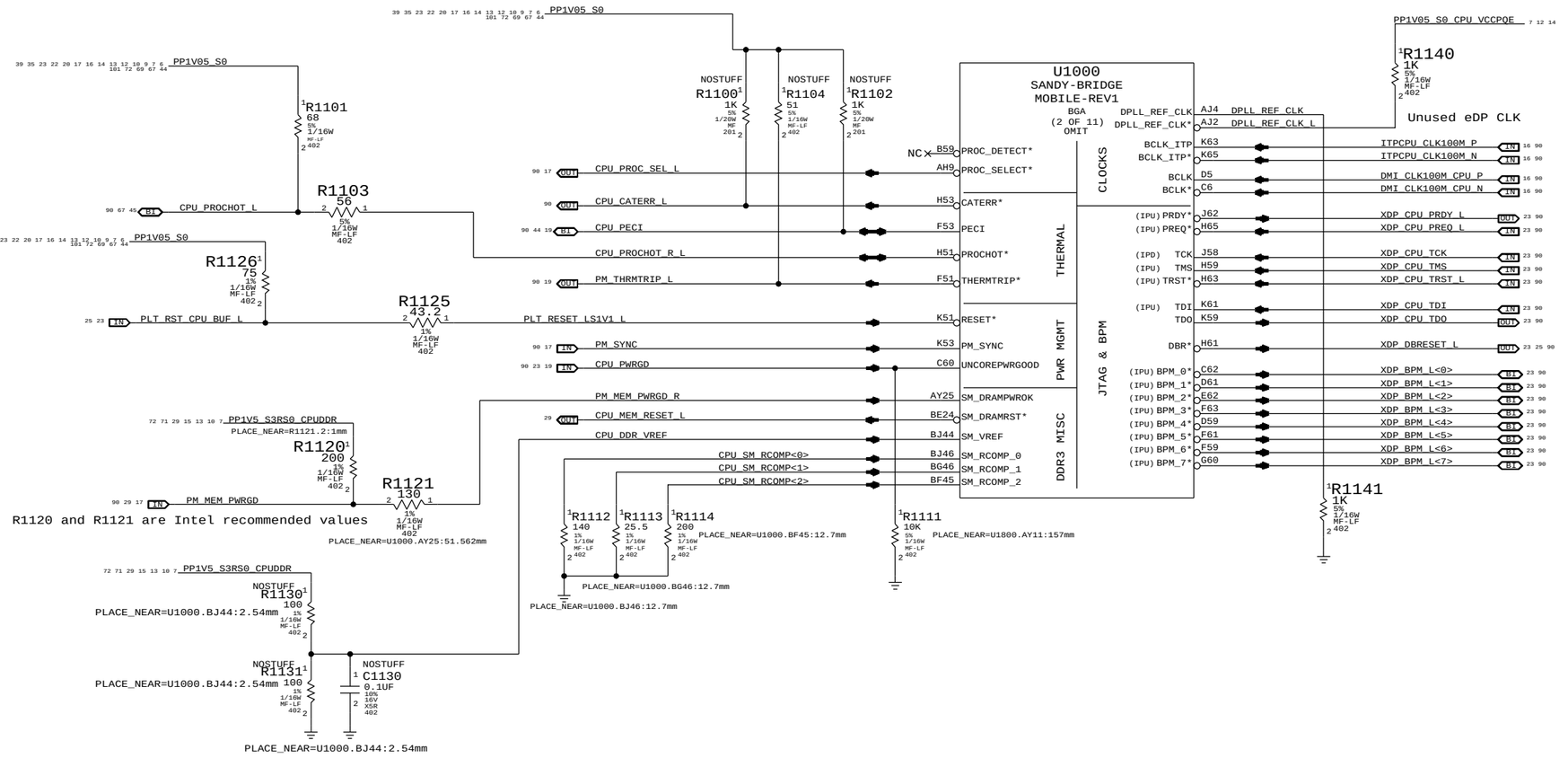

PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

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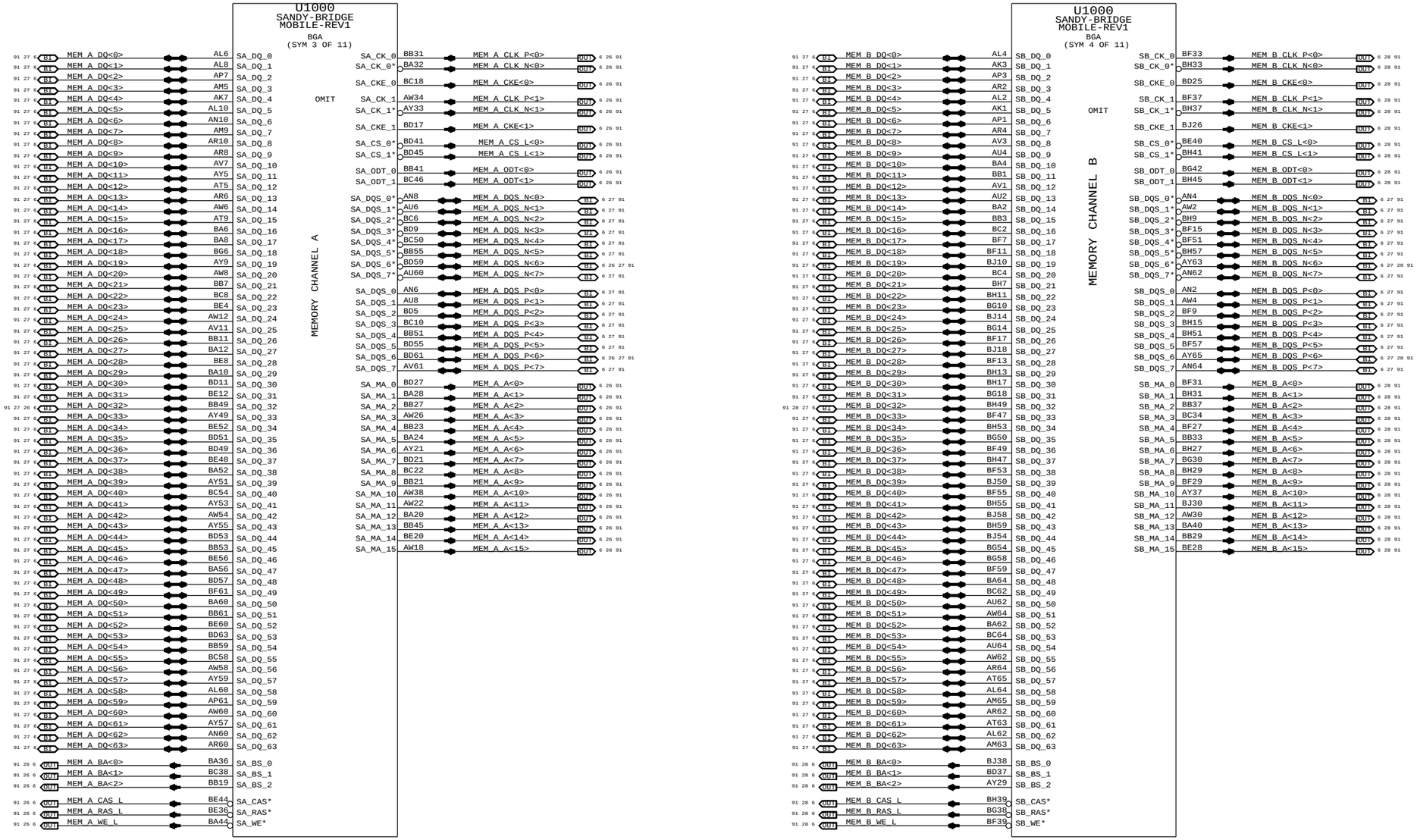

SYNC_DATE=06/15/2010

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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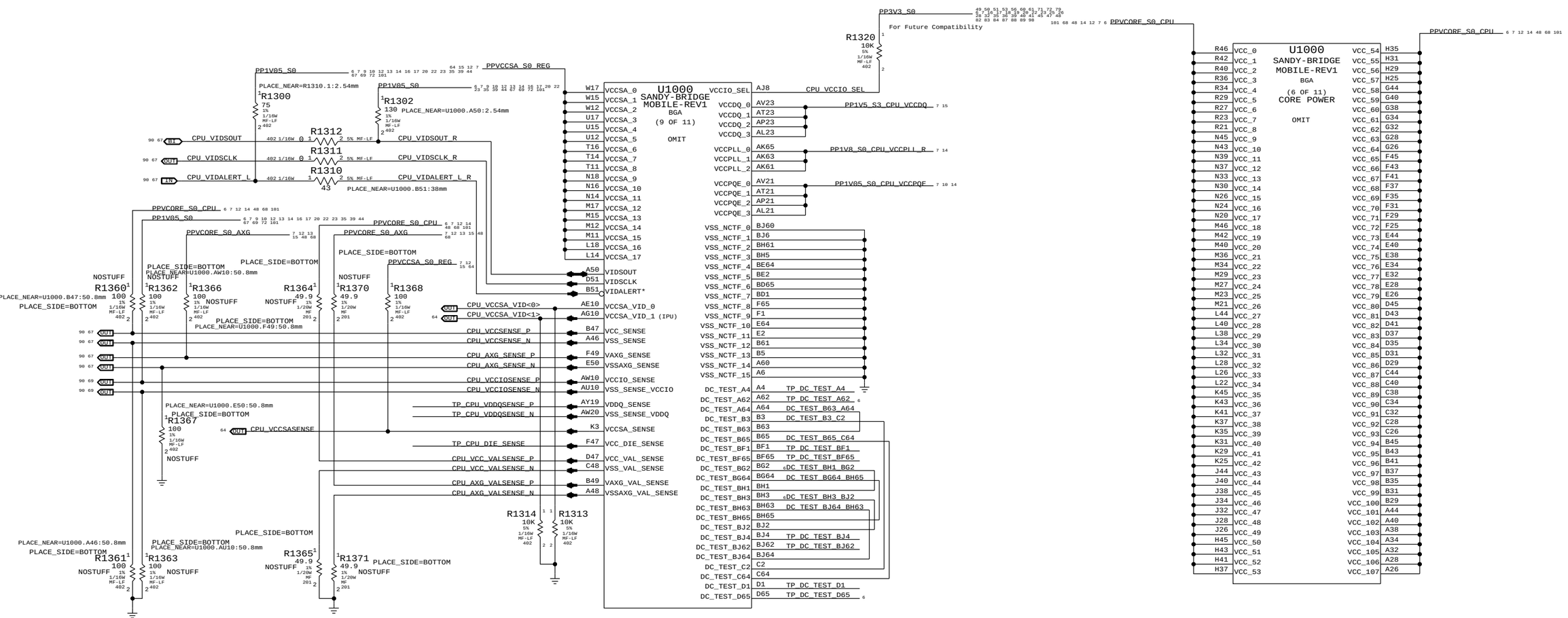

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K92_MLB SYNC_DATE=08/03/2010

PAGE TITLE: CPU POWER

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REVISION

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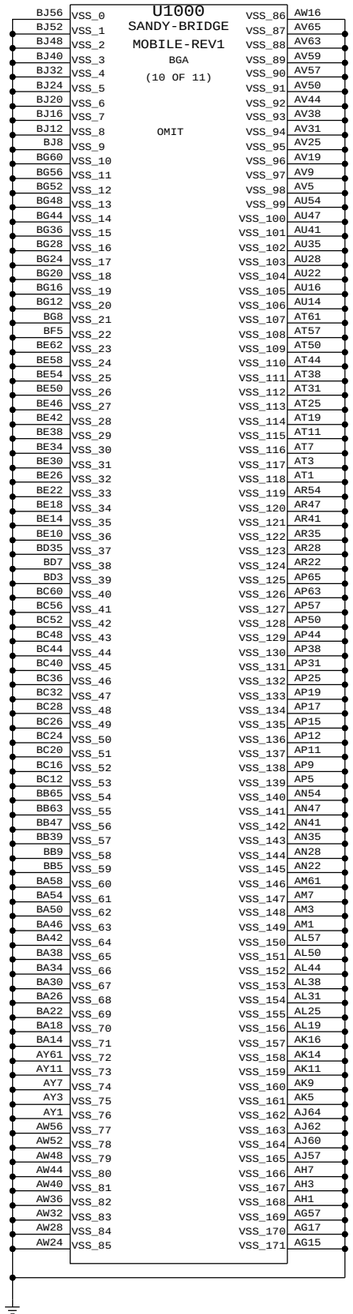
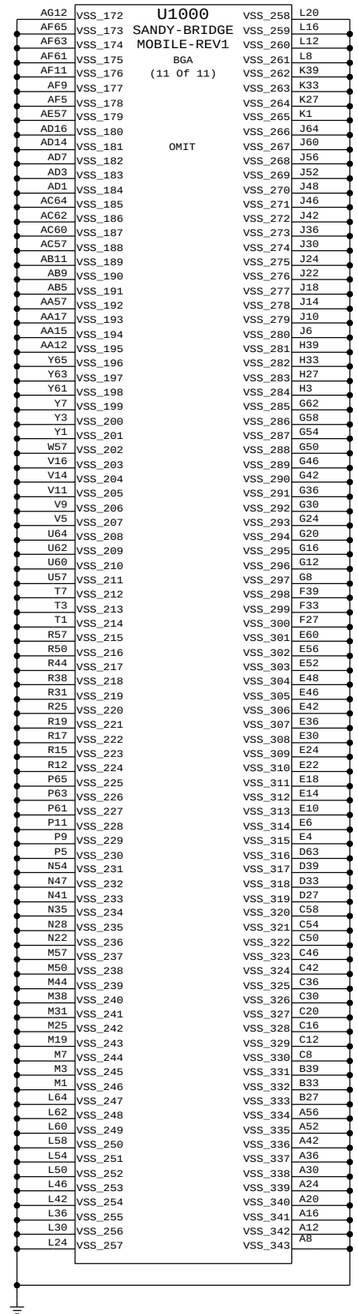
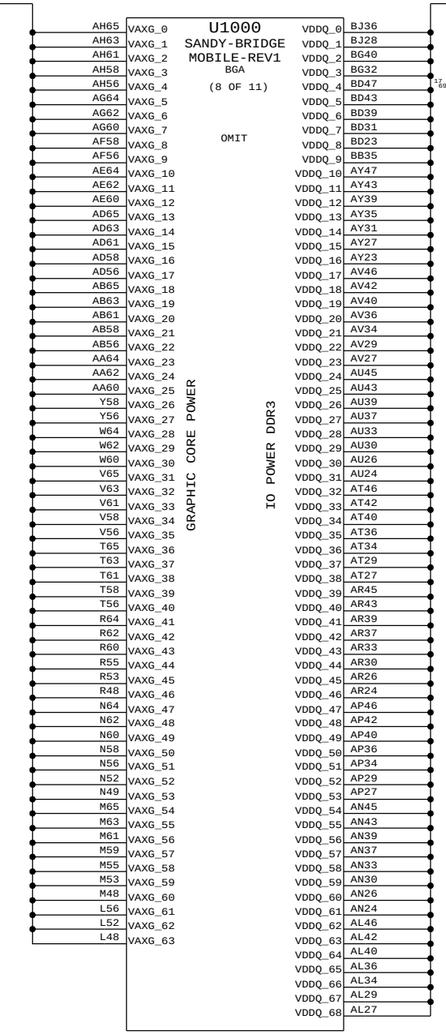


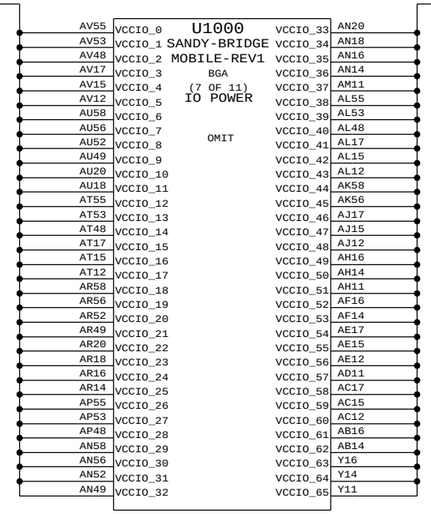


68 48 15 12 7 PPVCORE_S0_AXG



PP1V5_S3RS0_CPUDDR 7 10 15 29 71 72

PP1V05_S0 17 16 14 13 12 11 9 8 72 69 67 44 39 35 23 22 20



PP1V05_S0 67 69 72 101 17 20 25 33 38 39 44

PP1V05_S0 PP1V05_S0

PAGE TITLE	CPU POWER AND GND
Apple Inc.	DRAWING NUMBER: SIZE: D
	REVISION:
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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

101 68 48 12 7 6 PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 20% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

CRITICAL C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side. Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5R 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
22UF 20% 6.3V X5R 0603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

CRITICAL C1640 C1641 C1642 C1643
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NOSTUFF C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

39 35 23 16 1 PP1V05_S0

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X5R 402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

CRITICAL C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL C1682 C1683
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601
0.010
1% 1/4W MF 0603

PP1V05_S0_CPU_VCCPQE 7 10 12

C1684
1UF 10% 10V X5R 402

CPU VCCPLL DECOUPLING

87 71 70 25 22 20 17 7 6 PP1V8_S0

R1600
0
5% 1/16W MF-LF 402

PP1V8_S0_CPU_VCCPLL_R 7 12

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C1685
1UF 10% 10V X5R 402

C1686
1UF 10% 10V X5R 402

CRITICAL C1687
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

PAGE TITLE
CPU DECOUPLING-I

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VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

68 48 13 12 7 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
NOSTUFF C1709 1UF 10% 10V X5R 402
NOSTUFF C1710 1UF 10% 10V X5R 402
NOSTUFF C1711 1UF 10% 10V X5R 402
NOSTUFF C1712 1UF 10% 10V X5R 402
NOSTUFF C1713 1UF 10% 10V X5R 402
NOSTUFF C1714 1UF 10% 10V X5R 402
NOSTUFF C1715 1UF 10% 10V X5R 402
NOSTUFF C1716 1UF 10% 10V X5R 402
NOSTUFF C1717 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 6.3V CERM-X5R 0402-1
C1719 10UF 20% 6.3V CERM-X5R 0402-1
C1720 10UF 20% 6.3V CERM-X5R 0402-1
C1721 10UF 20% 6.3V CERM-X5R 0402-1
C1722 10UF 20% 6.3V CERM-X5R 0402-1
C1723 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1724 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1725 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 6.3V X5R-CERM1 0603
C1727 22UF 20% 6.3V X5R-CERM1 0603
C1728 22UF 20% 6.3V X5R-CERM1 0603
C1729 22UF 20% 6.3V X5R-CERM1 0603
C1730 22UF 20% 6.3V X5R-CERM1 0603
C1731 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1732 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1733 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.

C1734 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1735 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
NOSTUFF C1737 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

PLACEMENT_NOTE (C1738-C1747):

72 71 29 13 10 7 PP1V5_S3RS0_CPUDDR

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V X5R 603
C1749 10UF 20% 6.3V X5R 603
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V X5R 603
C1752 10UF 20% 6.3V X5R 603
C1753 10UF 20% 6.3V X5R 603
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V X5R 603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

PLACEMENT_NOTE (C1758-C1762):

64 12 7 PPVCCSA_S0_REG

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V X5R 603
C1764 10UF 20% 6.3V X5R 603
C1765 10UF 20% 6.3V X5R 603
C1766 10UF 20% 6.3V X5R 603
C1767 10UF 20% 6.3V X5R 603

C1768 270UF 20% 2V TANT CASE-B4-SM

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

PAGE TITLE: CPU DECOUPLING-II

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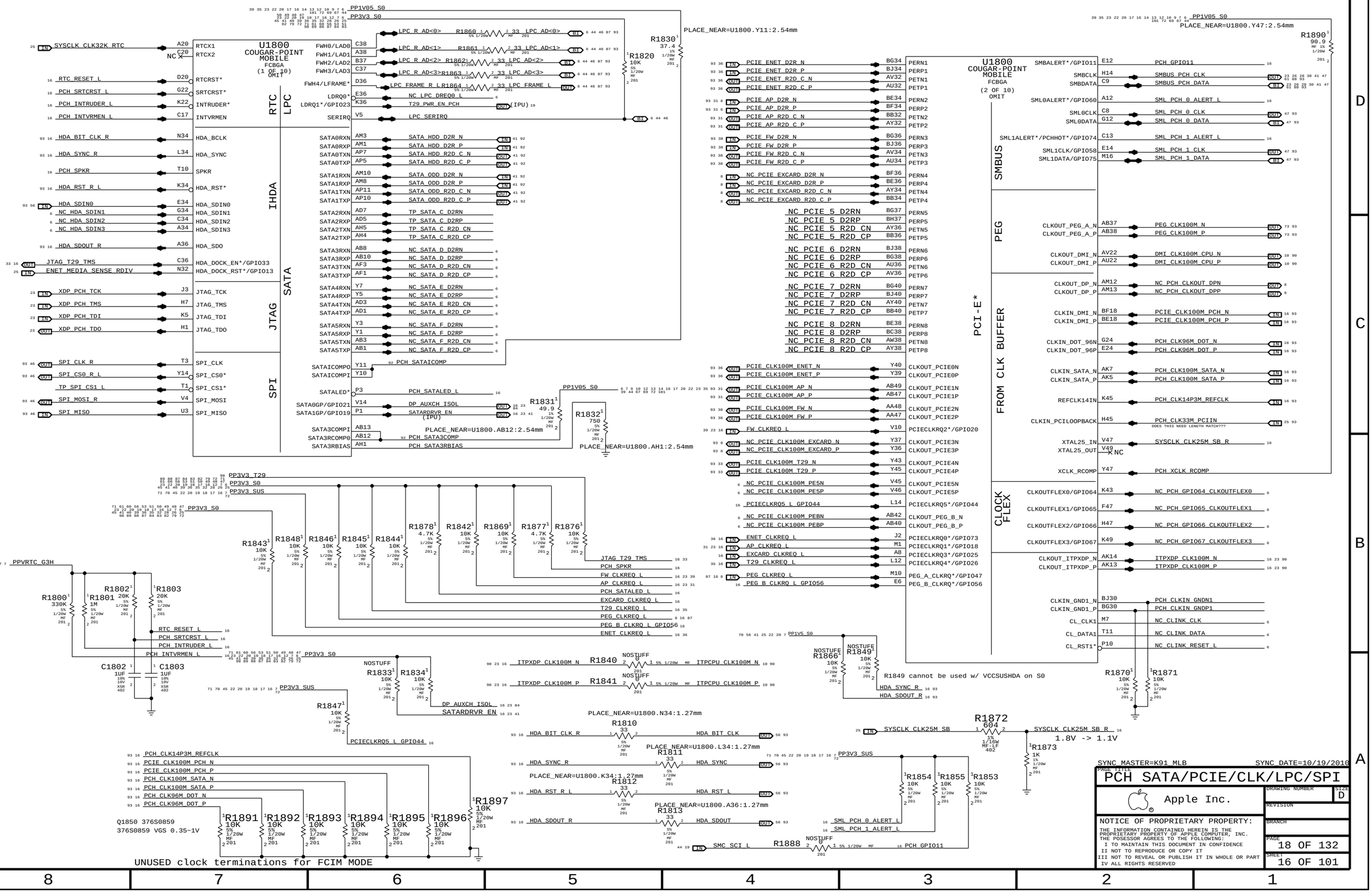
U1800
COUGAR-POINT MOBILE
FCBGA
(1 OF 10)
OMIT
LPC
RTC
SPI
SATA
JTAG
IHDA
SYSCLK_CLK32K_RTC
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
NC_HDA_SDIN1
NC_HDA_SDIN2
NC_HDA_SDIN3
HDA_SDOUT_R
JTAG_T29_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
PP1V05_S0
PP3V3_S0
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LPC_FRAME_R_L
LPC_SERIRQ
R1860
R1861
R1862
R1863
R1864
33_LPC_AD<0>
33_LPC_AD<1>
33_LPC_AD<2>
33_LPC_AD<3>
33_LPC_FRAME_L
R1830 37.4
R1820 10K
NC_LPC_DREQ0_L
T29_PWR_EN_PCH
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
NC_SATA_D_D2RN
NC_SATA_D_D2RP
NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP
NC_SATA_E_D2RN
NC_SATA_E_D2RP
NC_SATA_E_R2D_CN
NC_SATA_E_R2D_CP
NC_SATA_F_D2RN
NC_SATA_F_D2RP
NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP
PCH_SATAICOMP
PCH_SATALED_L
DP_AUXCH_ISOL
SATARDRVR_EN
(IPU)
R1831 49.9
R1832 750
PLACE_NEAR=U1800.AB12:2.54mm
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AH1:2.54mm
PLACE_NEAR=U1800.Y11:2.54mm
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
NC_PCIE_EXCARD_D2R_N
NC_PCIE_EXCARD_D2R_P
NC_PCIE_EXCARD_R2D_C_N
NC_PCIE_EXCARD_R2D_C_P
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
NC_PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_EXCARD_P
PCIE_CLK100M_T29_N
PCIE_CLK100M_T29_P
NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P
PCIECLKRQ5_L_GPIO44
NC_PCIE_CLK100M_PEBN
NC_PCIE_CLK100M_PEBP
ENET_CLKREQ_L
AP_CLKREQ_L
EXCARD_CLKREQ_L
T29_CLKREQ_L
PEG_CLKREQ_L
PEG_B_CLKRQ_L_GPIO56
PCIE-E*
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PCIECLKRQ0*/GPIO73
PCIECLKRQ1*/GPIO18
PCIECLKRQ3*/GPIO25
PCIECLKRQ4*/GPIO26
PEG_A_CLKRQ*/GPIO47
PEG_B_CLKRQ*/GPIO56
SMBUS
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
PCH_GPIO11
SMBUS_PCH_CLK
SMBUS_PCH_DATA
SML_PCH_0_ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
SML_PCH_1_ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
PEG
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
PEG_CLK100M_N
PEG_CLK100M_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
FROM CLK BUFFER
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
NC_PCH_CLKOUT_DPN
NC_PCH_CLKOUT_DPP
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
DOES THIS NEED LENGTH MATCH???
SYSCLK_CLK25M_SB_R
PCH_XCLK_RCOMP
CLOCK FLEX
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
CLKIN_GND1_N
CLKIN_GND1_P
CL_CLK1
CL_DATA1
CL_RST1*
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
NC_CLINK_CLK
NC_CLINK_DATA
NC_CLINK_RESET_L
R1840
R1841
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
R1866 10K
R1849 10K
R1849 cannot be used w/ VCCSUSHDA on S0
R1870 10K
R1871 10K
R1847 10K
R1833 10K
R1834 10K
PCIECLKRQ5_L_GPIO44
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1UF
C1803 1UF
R1843 10K
R1848 10K
R1846 10K
R1845 10K
R1844 10K
R1878 4.7K
R1842 10K
R1869 10K
R1877 4.7K
R1876 10K
JTAG_T29_TMS
PCH_SPKR
FW_CLKREQ_L
AP_CLKREQ_L
PCH_SATALED_L
EXCARD_CLKREQ_L
T29_CLKREQ_L
PEG_CLKREQ_L
PEG_B_CLKRQ_L_GPIO56
ENET_CLKREQ_L
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
R1810 33
R1811 33
R1812 33
R1813 33
PLACE_NEAR=U1800.N34:1.27mm
PLACE_NEAR=U1800.L34:1.27mm
PLACE_NEAR=U1800.K34:1.27mm
PLACE_NEAR=U1800.A36:1.27mm
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
HDA_SDOUT_R
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
HDA_SDOUT
R1872 604
SYSCLK_CLK25M_SB
SYSCLK_CLK25M_SB_R
1.8V -> 1.1V
R1873 1K
R1854 10K
R1855 10K
R1853 10K
SML_PCH_0_ALERT_L
SML_PCH_1_ALERT_L
R1888
SMC_SCI_L
PCH_GPIO11
R1897 10K
R1891 10K
R1892 10K
R1893 10K
R1894 10K
R1895 10K
R1896 10K
Q1850 376S0859
376S0859 VGS 0.35~1V
UNUSED clock terminations for FCIM MODE
SYNC_MASTER=K91_MLB
SYNC_DATE=10/19/2010
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
Apple Inc.
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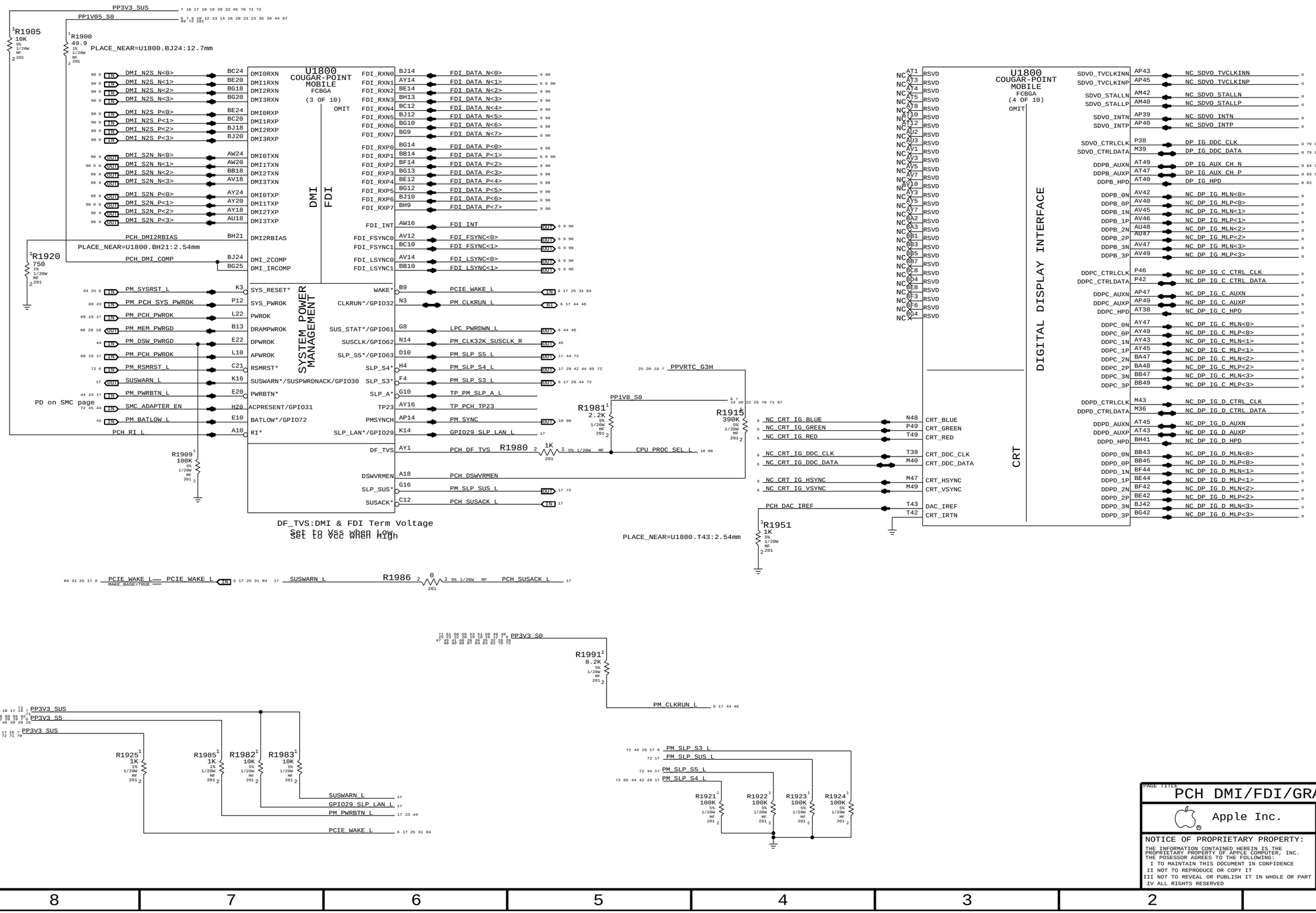
PP3V3_SUS
PP1V05_S0
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201
PLACE_NEAR=U1800.BJ24:12.7mm
U1800
COUGAR-POINT
MOBILE
FCBGA
(3 OF 10)
OMIT
DMI
FDI
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
PCH_DMI2RBIAS
PLACE_NEAR=U1800.BH21:2.54mm
R1920 750 1% 1/20W MF 201
PCH_DMI_COMP
FDI_DATA_N<0>
FDI_DATA_N<1>
FDI_DATA_N<2>
FDI_DATA_N<3>
FDI_DATA_N<4>
FDI_DATA_N<5>
FDI_DATA_N<6>
FDI_DATA_N<7>
FDI_DATA_P<0>
FDI_DATA_P<1>
FDI_DATA_P<2>
FDI_DATA_P<3>
FDI_DATA_P<4>
FDI_DATA_P<5>
FDI_DATA_P<6>
FDI_DATA_P<7>
FDI_INT
FDI_FSYNC<0>
FDI_FSYNC<1>
FDI_LSYNC<0>
FDI_LSYNC<1>
SYSTEM POWER MANAGEMENT
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_MEM_PWRGD
PM_DSW_PWRGD
PM_RSMRST_L
SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
PD on SMC page
R1909 100K 5% 1/20W MF 201
WAKE*
CLKRUN*/GPIO32
SUS_STAT*/GPIO61
SUSCLK/GPIO62
SLP_S5*/GPIO63
SLP_S4*
SLP_S3*
SLP_A*
TP23
PMSYNCH
SLP_LAN*/GPIO29
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
TP_PCH_TP23
PM_SYNC
GPIO29_SLP_LAN_L
PPVRTC_G3H
R1981 2.2K 5% 1/20W MF 201
PP1V8_S0
R1915 390K 5% 1/20W MF 201
R1980 1K 5% 1/20W MF 201
CPU_PROC_SEL_L
DF_TVS
PCH_DF_TVS
DSWVRMEN
PCH_DSWVRMEN
SLP_SUS*
PM_SLP_SUS_L
SUSACK*
PCH_SUSACK_L
DF_TVS:DMI & FDI Term Voltage
Set to Vss when low
Set to Vcc when high
PLACE_NEAR=U1800.T43:2.54mm
R1951 1K 5% 1/20W MF 201
PCH_DAC_IREF
PCIE_WAKE_L
MAKE_BASE=TRUE
R1986 0 5% 1/20W MF 201
SUSWARN_L
PCH_SUSACK_L
R1991 8.2K 5% 1/20W MF 201
PP3V3_S0
PM_CLKRUN_L
PP3V3_SUS
PP3V3_S5
R1925 1K 1% 1/20W MF 201
R1985 1K 1% 1/20W MF 201
R1982 10K 5% 1/20W MF 201
R1983 10K 5% 1/20W MF 201
SUSWARN_L
GPIO29_SLP_LAN_L
PM_PWRBTN_L
PCIE_WAKE_L
R1921 100K 5% 1/20W MF 201
R1922 100K 5% 1/20W MF 201
R1923 100K 5% 1/20W MF 201
R1924 100K 5% 1/20W MF 201
U1800
COUGAR-POINT
MOBILE
FCBGA
(4 OF 10)
OMIT
DIGITAL DISPLAY INTERFACE
CRT
NC_CRT_IG_BLUE
NC_CRT_IG_GREEN
NC_CRT_IG_RED
NC_CRT_IG_DDC_CLK
NC_CRT_IG_DDC_DATA
NC_CRT_IG_HSYNC
NC_CRT_IG_VSYNC
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN
SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP
SDVO_CTRLCLK
SDVO_CTRLDATA
DDPB_AUXN
DDPB_AUXP
DDPB_HPD
DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPC_AUXN
DDPC_AUXP
DDPC_HPD
DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P
DDPD_CTRLCLK
DDPD_CTRLDATA
DDPD_AUXN
DDPD_AUXP
DDPD_HPD
DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P
NC_SDVO_TVCLKINN
NC_SDVO_TVCLKINP
NC_SDVO_STALLN
NC_SDVO_STALLP
NC_SDVO_INTN
NC_SDVO_INTP
DP_IG_DDC_CLK
DP_IG_DDC_DATA
DP_IG_AUX_CH_N
DP_IG_AUX_CH_P
DP_IG_HPD
NC_DP_IG_MLN<0>
NC_DP_IG_MLP<0>
NC_DP_IG_MLN<1>
NC_DP_IG_MLP<1>
NC_DP_IG_MLN<2>
NC_DP_IG_MLP<2>
NC_DP_IG_MLN<3>
NC_DP_IG_MLP<3>
NC_DP_IG_C_CTRL_CLK
NC_DP_IG_C_CTRL_DATA
NC_DP_IG_C_AUXN
NC_DP_IG_C_AUXP
NC_DP_IG_C_HPD
NC_DP_IG_C_MLN<0>
NC_DP_IG_C_MLP<0>
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NC_DP_IG_C_MLN<3>
NC_DP_IG_C_MLP<3>
NC_DP_IG_D_CTRL_CLK
NC_DP_IG_D_CTRL_DATA
NC_DP_IG_D_AUXN
NC_DP_IG_D_AUXP
NC_DP_IG_D_HPD
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NC_DP_IG_D_MLP<0>
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NC_DP_IG_D_MLP<1>
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NC_DP_IG_D_MLP<2>
NC_DP_IG_D_MLN<3>
NC_DP_IG_D_MLP<3>
PAGE TITLE
PCH DMI/FDI/GRAPHICS
Apple Inc.
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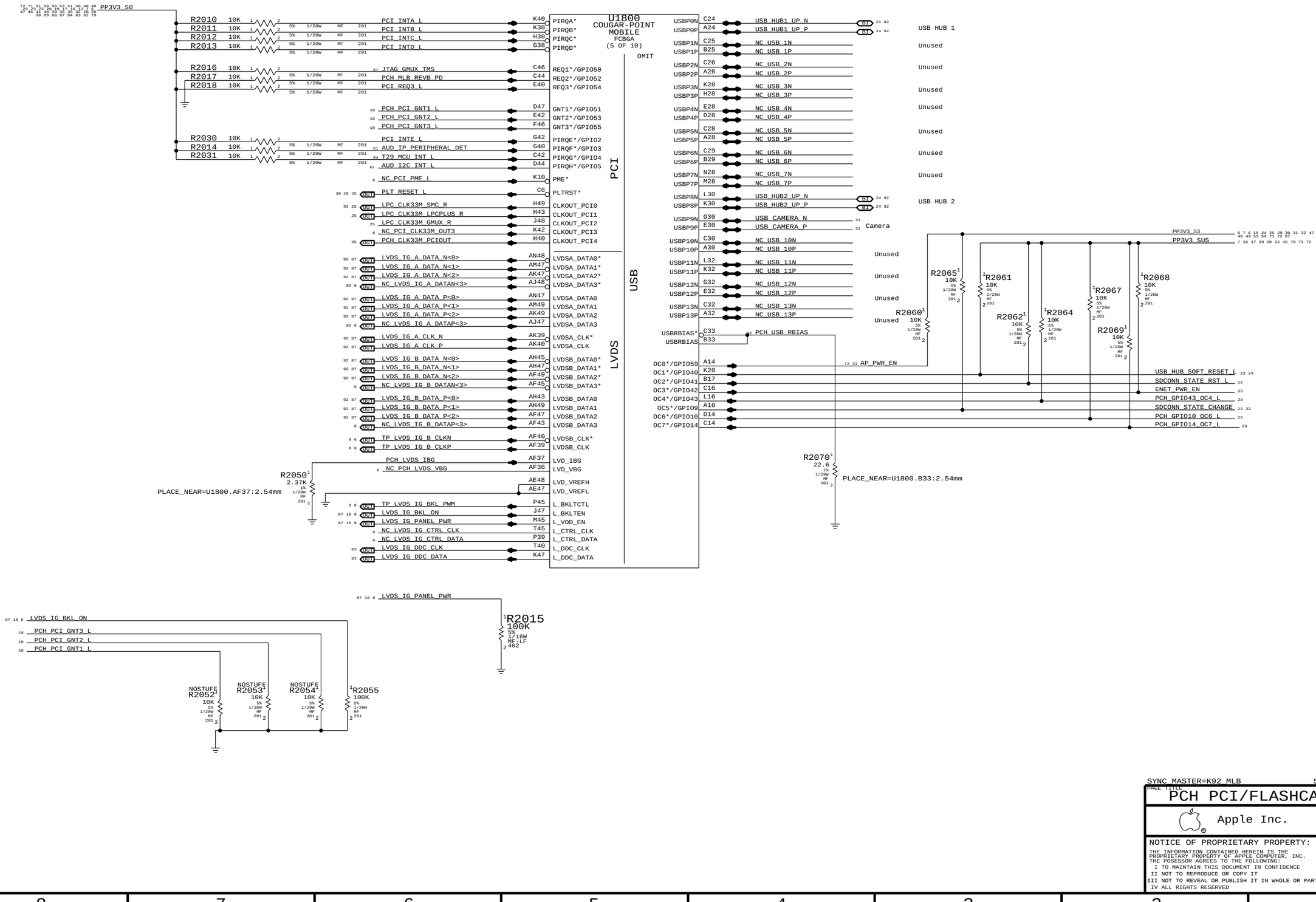

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE
PCH PCI/FLASHCACHE/USB

Apple Inc.

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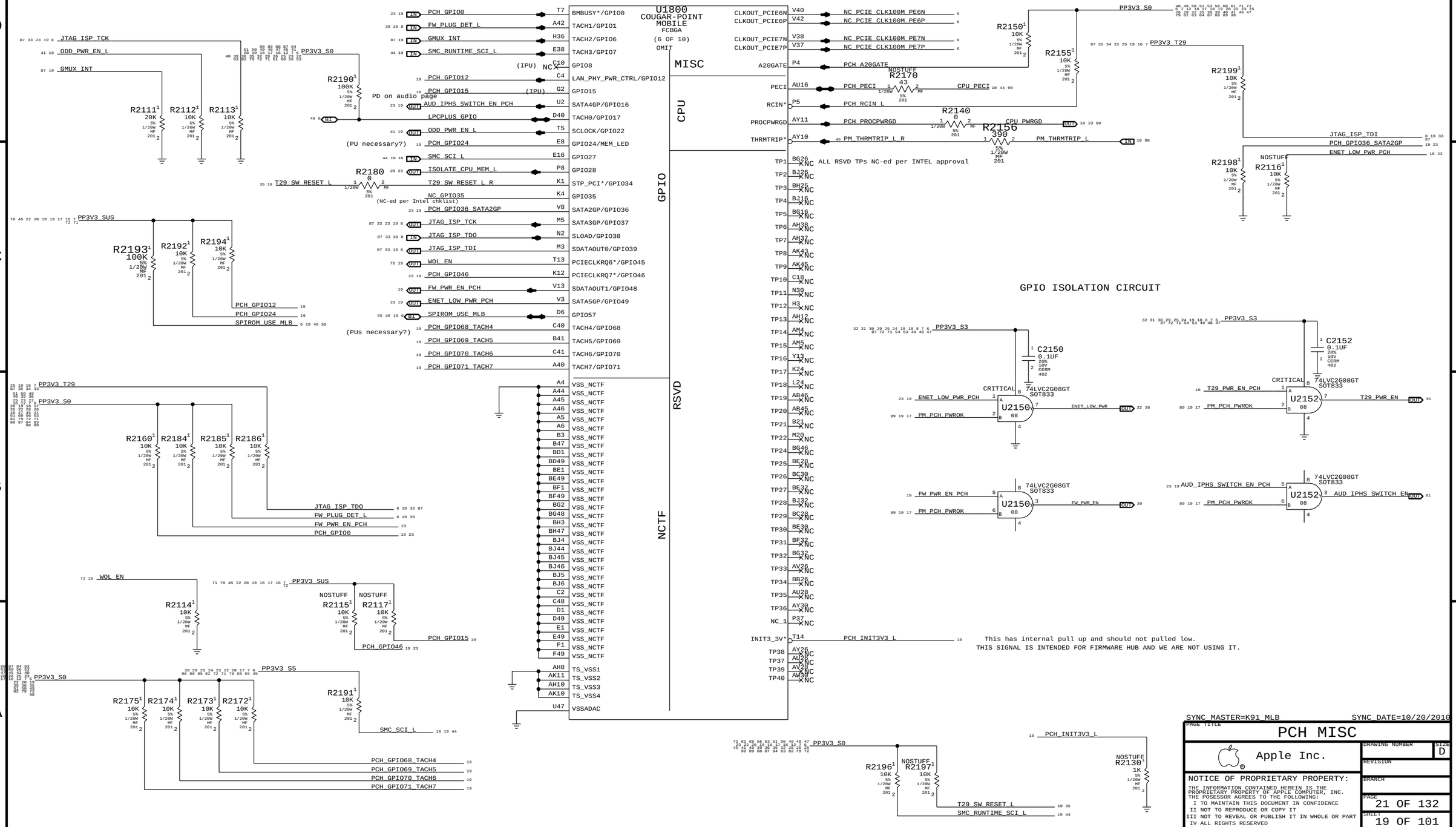

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE

PCH MISC

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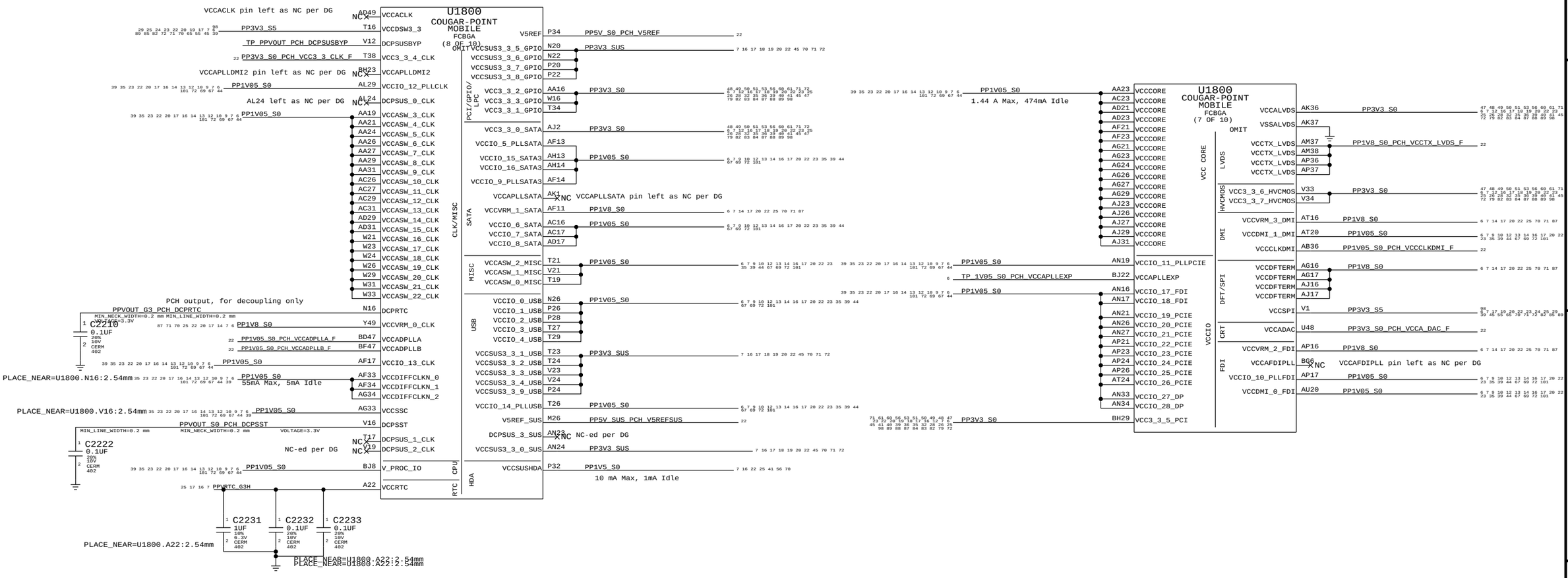

PAGE TITLE

PCH POWER

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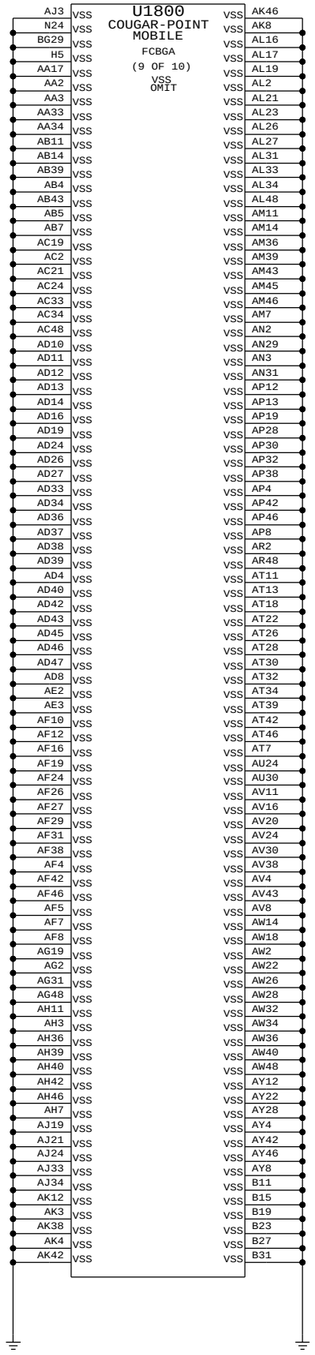

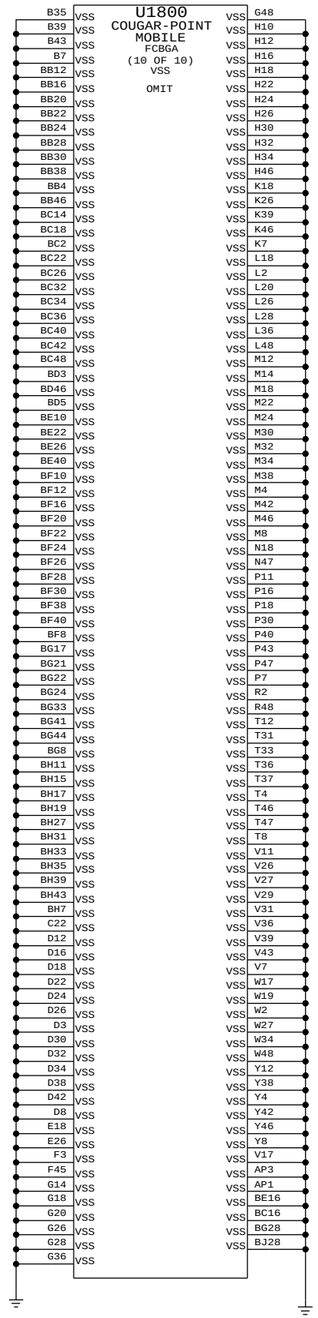

SYNC_MASTER=K92_MLB SYNC_DATE=04/30/2010

PAGE TITLE

PCH GROUNDS

Apple Inc.

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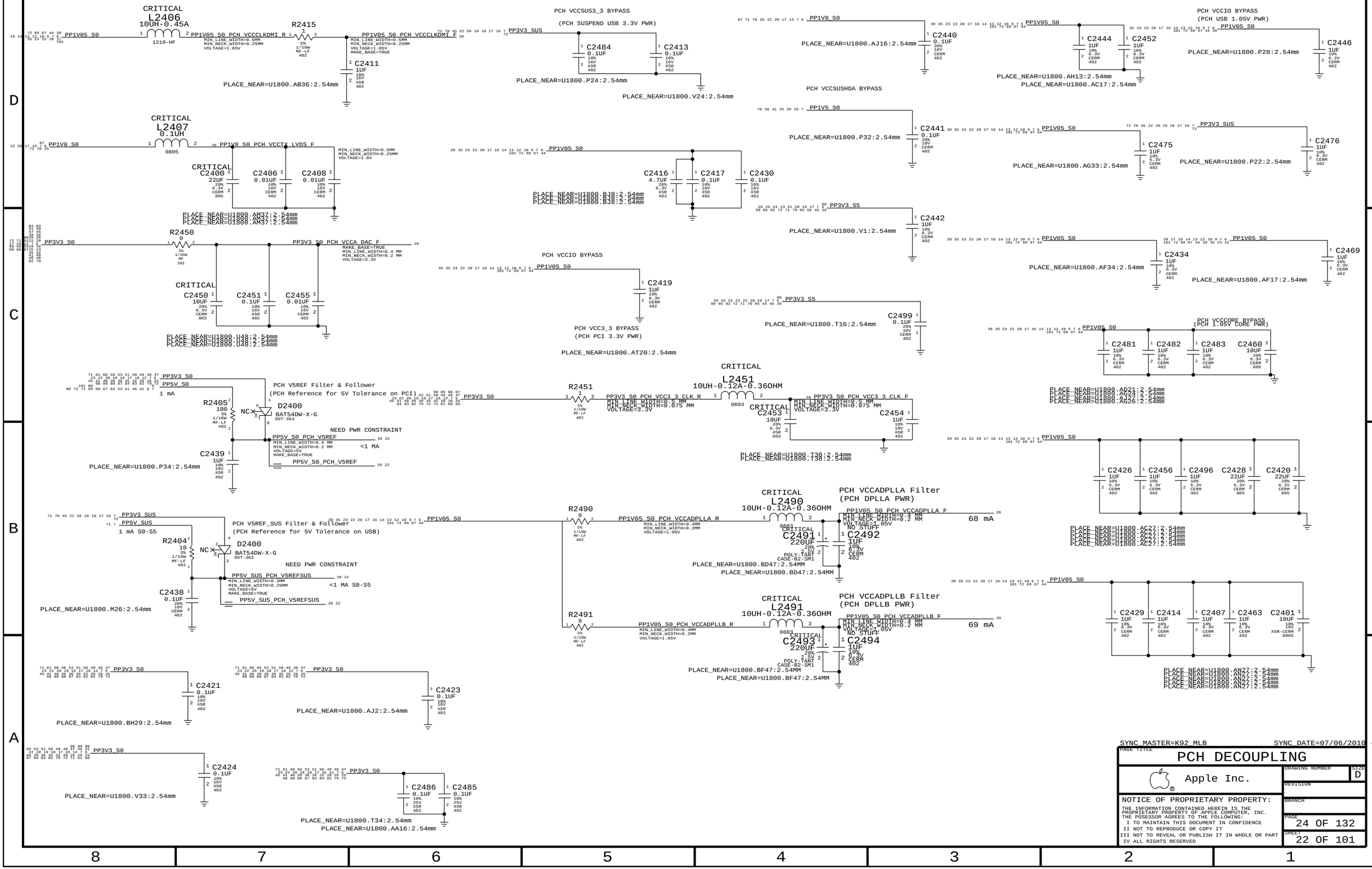

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE

PCH DECOUPLING

Apple Inc.

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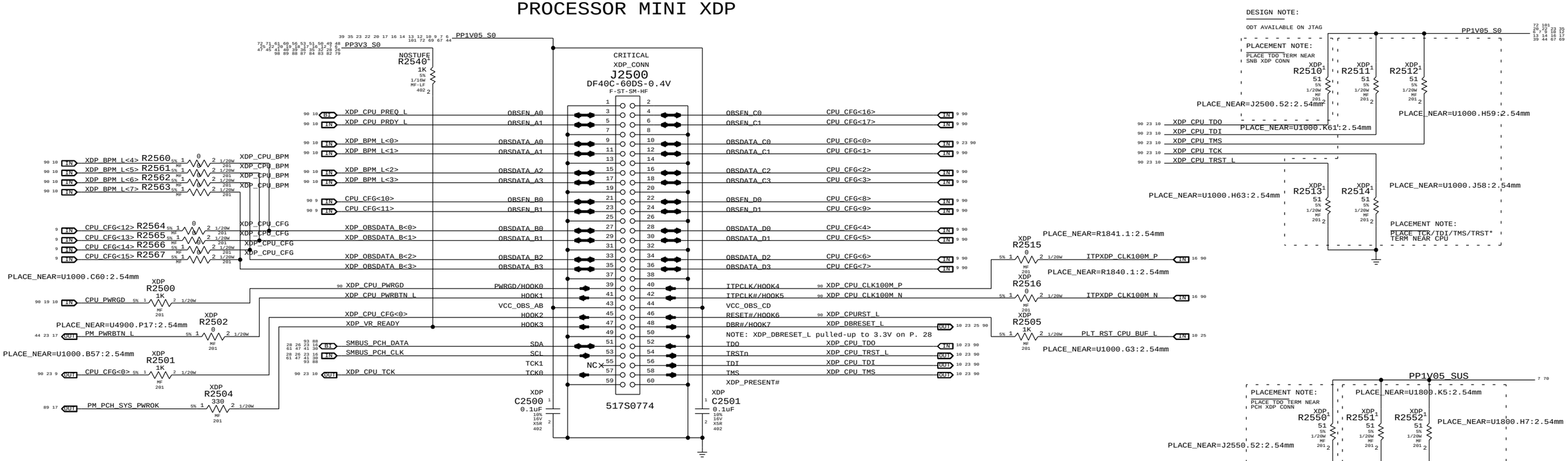
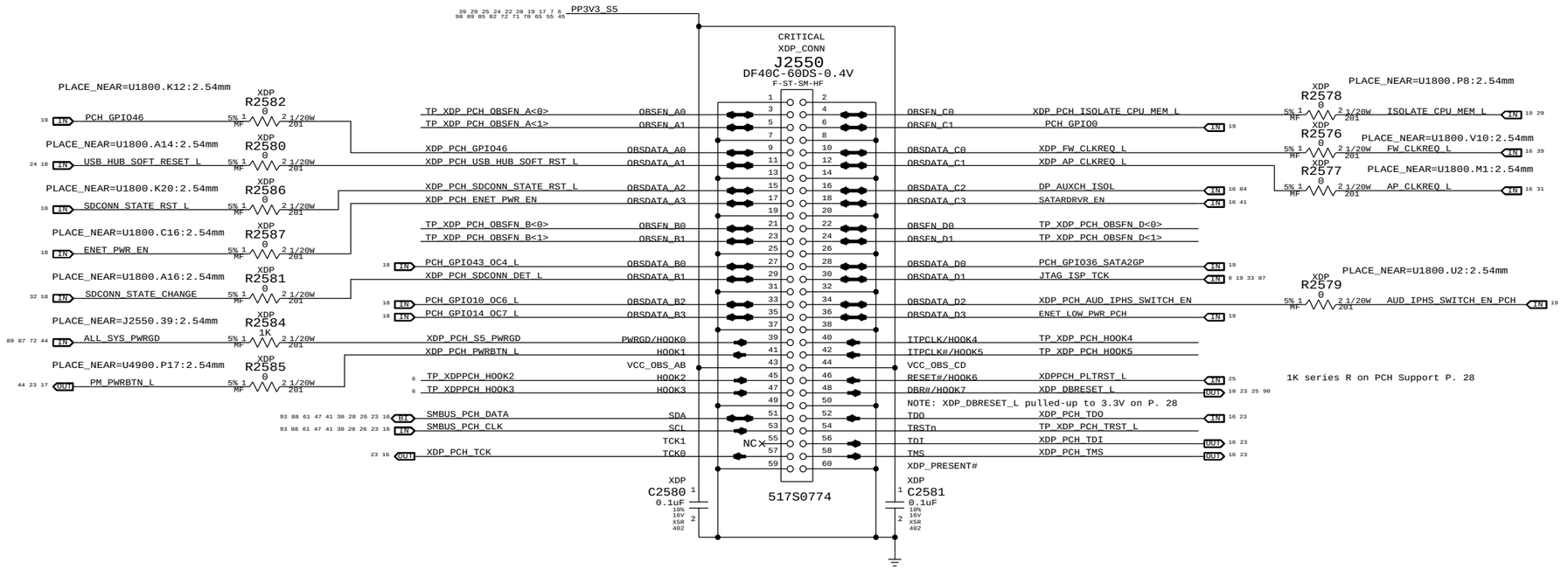
PROCESSOR MINI XDP



PCH MINI XDP



SYNC_MASTER=K91_MLB SYNC_DATE=10/17/2010

PAGE TITLE: CPU & PCH XDP

Apple Inc.

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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

T29 - no longer used, pulled up to 3V3 S0

IR Receiver

External B

External C

Bluetooth

Trackpad/Keyboard

External A

SD Card/Express Card

SYNC MASTER=K91_ERIC SYNC DATE=10/08/2010

PAGE TITLE: USB HUBS

Apple Inc.

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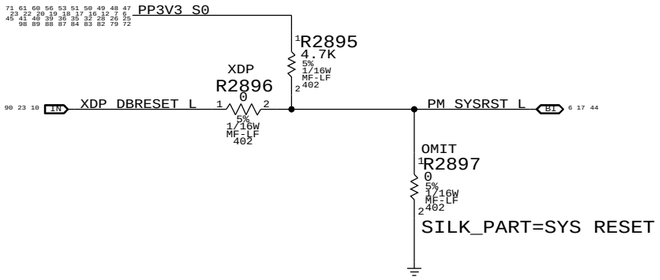
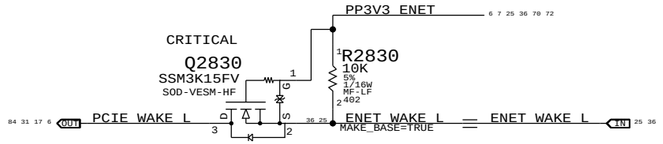
PCH Reset Button

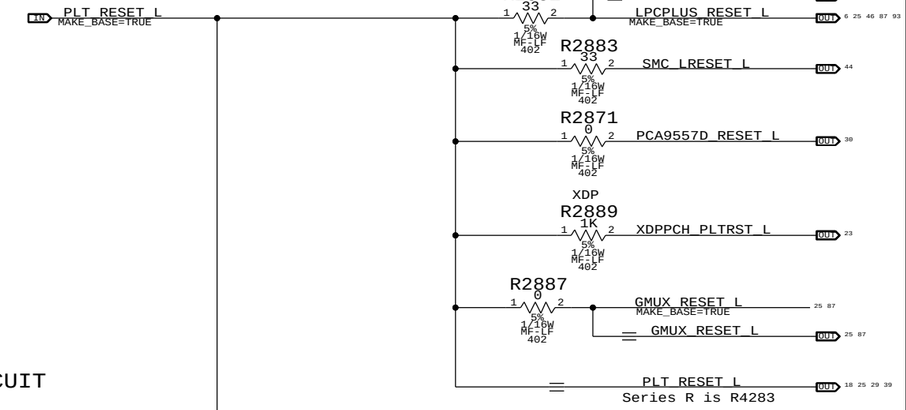


Ethernet WAKE# Isolation



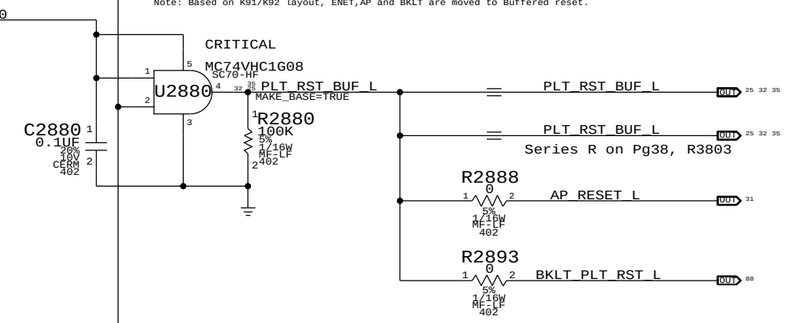
Platform Reset Connections

Unbuffered

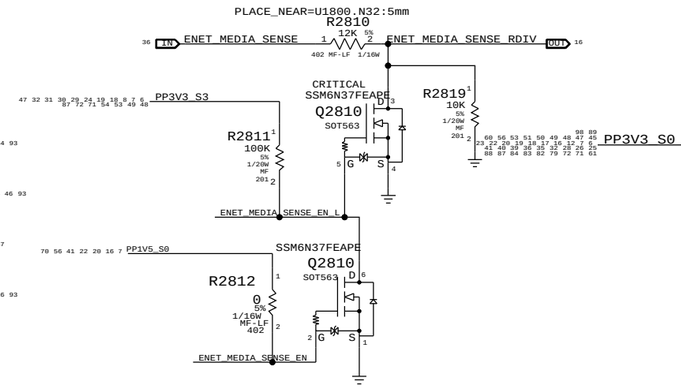


Buffered

Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.



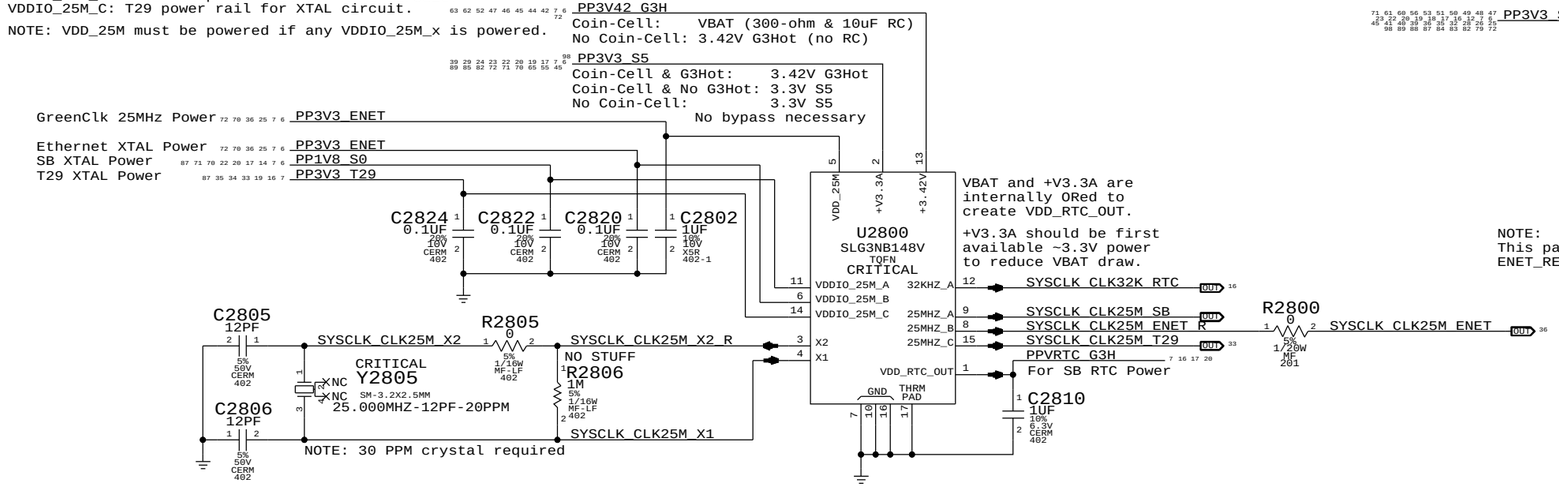
ENET_MEDIA_SENSE ISOLATION CIRCUIT



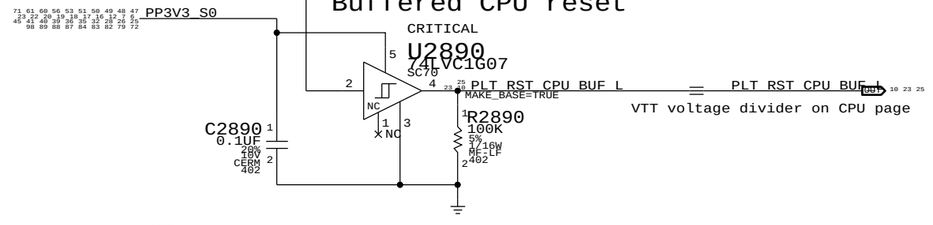
System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



Buffered CPU reset



NOTE:
This page is different for K92.
ENET_RESET_L hooked up differently on both the projects.

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE: Chipset Support

Apple Inc.

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_A_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2900 10UF 20% 6.3V X6S 603 — PLACE_NEAR=J2900.75:2.54mm
C2901 10UF 20% 6.3V X6S 603 — PLACE_NEAR=J2900.75:2.54mm

C2910 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2911 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2912 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2913 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2914 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2915 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2916 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2917 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2918 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2919 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2920 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2921 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2922 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2923 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

PP0V75_S0_DDRVTT

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

J2900 — DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2) — F-RT-THB — OMIT_TABLE

73	CKE0	MEM_A_CKE<0>	74	CKE1	MEM_A_CKE<1>
75	VDD		76	VDD	
77	NC	NC	78	A15	MEM_A_A<15>
79	BA2	MEM_A_BA<2>	80	A14	MEM_A_A<14>
81	VDD		82	VDD	
83	A12/BC*	MEM_A_A<12>	84	A11	MEM_A_A<11>
85	A9	MEM_A_A<9>	86	A7	MEM_A_A<7>
87	VDD		88	VDD	
89	A8	MEM_A_A<8>	90	A6	MEM_A_A<6>
91	A5	MEM_A_A<5>	92	A4	MEM_A_A<4>
93	VDD		94	VDD	
95	A3	MEM_A_A<3>	96	A2	MEM_A_A<2>
97	A1	MEM_A_A<1>	98	A0	MEM_A_A<0>
99	VDD		100	VDD	
101	CK0	MEM_A_CLK_P<0>	102	CK1	MEM_A_CLK_P<1>
103	CK0*	MEM_A_CLK_N<0>	104	CK1*	MEM_A_CLK_N<1>
105	VDD		106	VDD	
107	A10/AP	MEM_A_A<10>	108	BA1	MEM_A_BA<1>
109	BA0	MEM_A_BA<0>	110	RAS*	MEM_A_RAS_L
111	VDD		112	VDD	
113	WE*	MEM_A_WE_L	114	S0*	MEM_A_CS_L<0>
115	CAS*	MEM_A_CAS_L	116	ODT0	MEM_A_ODT<0>
117	VDD		118	VDD	
119	A13	MEM_A_A<13>	120	ODT1	MEM_A_ODT<1>
121	S1*	MEM_A_CS_L<1>	122	NC	NC
123	VDD		124	VDD	
125	TEST	NC	126	VREFCA	
127	VSS		128	VSS	
129	DQ32	=MEM_A_DQ<32>	130	DQ36	MEM_A_DQ<32>
131	DQ33	=MEM_A_DQ<33>	132	DQ37	=MEM_A_DQ<37>
133	VSS		134	VSS	
135	DQS4*	=MEM_A_DQS_N<4>	136	DM4	
137	DQS4	=MEM_A_DQS_P<4>	138	VSS	
139	VSS		140	DQ38	=MEM_A_DQ<38>
141	DQ34	=MEM_A_DQ<34>	142	DQ39	=MEM_A_DQ<39>
143	DQ35	=MEM_A_DQ<35>	144	VSS	
145	VSS		146	DQ44	=MEM_A_DQ<44>
147	DQ40	=MEM_A_DQ<40>	148	DQ45	=MEM_A_DQ<45>
149	DQ41	=MEM_A_DQ<41>	150	VSS	
151	VSS		152	DQS5*	=MEM_A_DQS_N<5>
153	DM5		154	DQS5	=MEM_A_DQS_P<5>
155	VSS		156	VSS	
157	DQ42	=MEM_A_DQ<42>	158	DQ46	=MEM_A_DQ<46>
159	DQ43	=MEM_A_DQ<43>	160	DQ47	=MEM_A_DQ<47>
161	VSS		162	VSS	
163	DQ48	=MEM_A_DQ<48>	164	DQ52	=MEM_A_DQ<52>
165	DQ49	=MEM_A_DQ<49>	166	DQ53	=MEM_A_DQ<53>
167	VSS		168	VSS	
169	DQS6*	MEM_A_DQS_N<6>	170	DM6	
171	DQS6	MEM_A_DQS_P<6>	172	VSS	
173	VSS		174	DQ54	=MEM_A_DQ<54>
175	DQ50	=MEM_A_DQ<50>	176	DQ55	=MEM_A_DQ<55>
177	DQ51	=MEM_A_DQ<51>	178	VSS	
179	VSS		180	DQ60	=MEM_A_DQ<60>
181	DQ56	=MEM_A_DQ<56>	182	DQ61	=MEM_A_DQ<61>
183	DQ57	=MEM_A_DQ<57>	184	VSS	
185	VSS		186	DQS7*	=MEM_A_DQS_N<7>
187	DM7		188	DQS7	=MEM_A_DQS_P<7>
189	VSS		190	VSS	
191	DQ58	=MEM_A_DQ<58>	192	DQ62	=MEM_A_DQ<62>
193	DQ59	=MEM_A_DQ<59>	194	DQ63	=MEM_A_DQ<63>
195	VSS		196	VSS	
197	SA0	MEM_A_SA<0>	198	EVENT*	MEM_EVENT_L
199	VDDSPD		200	SDA	SMBUS_PCH_DATA
201	SA1	MEM_A_SA<1>	202	SCL	SMBUS_PCH_CLK
203	VTT		204	VTT	

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

J2900 — DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) — F-RT-THB — CRITICAL — OMIT_TABLE

1	VREFDQ		2	VSS	
3	VSS		4	DQ4	=MEM_A_DQ<4>
5	DQ0	=MEM_A_DQ<0>	6	DQ5	=MEM_A_DQ<5>
7	DQ1	=MEM_A_DQ<1>	8	VSS	
9	VSS		10	DQS0*	=MEM_A_DQS_N<0>
11	DM0		12	DQS0	=MEM_A_DQS_P<0>
13	VSS		14	VSS	
15	DQ2	=MEM_A_DQ<2>	16	DQ6	=MEM_A_DQ<6>
17	DQ3	=MEM_A_DQ<3>	18	DQ7	=MEM_A_DQ<7>
19	VSS		20	VSS	
21	DQ8	=MEM_A_DQ<8>	22	DQ12	=MEM_A_DQ<12>
23	DQ9	=MEM_A_DQ<9>	24	DQ13	=MEM_A_DQ<13>
25	VSS		26	VSS	
27	DQS1*	=MEM_A_DQS_N<1>	28	DM1	
29	DQS1	=MEM_A_DQS_P<1>	30	RESET*	MEM_RESET_L
31	VSS		32	VSS	
33	DQ10	=MEM_A_DQ<10>	34	DQ14	=MEM_A_DQ<14>
35	DQ11	=MEM_A_DQ<11>	36	DQ15	=MEM_A_DQ<15>
37	VSS		38	VSS	
39	DQ16	=MEM_A_DQ<16>	40	DQ20	=MEM_A_DQ<20>
41	DQ17	=MEM_A_DQ<17>	42	DQ21	=MEM_A_DQ<21>
43	VSS		44	VSS	
45	DQS2*	=MEM_A_DQS_N<2>	46	DM2	
47	DQS2	=MEM_A_DQS_P<2>	48	VSS	
49	VSS		50	DQ22	=MEM_A_DQ<22>
51	DQ18	=MEM_A_DQ<18>	52	DQ23	=MEM_A_DQ<23>
53	DQ19	=MEM_A_DQ<19>	54	VSS	
55	VSS		56	DQ28	=MEM_A_DQ<28>
57	DQ24	=MEM_A_DQ<24>	58	DQ29	=MEM_A_DQ<29>
59	DQ25	=MEM_A_DQ<25>	60	VSS	
61	VSS		62	DQS3*	=MEM_A_DQS_N<3>
63	DM3		64	DQS3	=MEM_A_DQS_P<3>
65	VSS		66	VSS	
67	DQ26	=MEM_A_DQ<26>	68	DQ30	=MEM_A_DQ<30>
69	DQ27	=MEM_A_DQ<27>	70	DQ31	=MEM_A_DQ<31>
71	VSS		72	VSS	

See CSA05 BOM table

"Factory" (top) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

91 11 6	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	26
91 11 6	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	26
		MAKE_BASE=TRUE		
91 11 6	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	26
91 11 6	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	26
91 11 6	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	26
91 11 6	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	26
91 11 6	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	26
91 11 6	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	26
91 11 6	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	26
91 11 6	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	26
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

91 11 6	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	26
91 11 6	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	26
		MAKE_BASE=TRUE		
91 11 6	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	26
91 11 6	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	26
91 11 6	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	26
91 11 6	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	26
91 11 6	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	26
91 11 6	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	26
91 11 6	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	26
91 11 6	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	26
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

91 11 6	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	26
91 11 6	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	26
		MAKE_BASE=TRUE		
91 11 6	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	26
91 11 6	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	26
91 11 6	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	26
91 11 6	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	26
91 11 6	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	26
91 11 6	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	26
91 11 6	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	26
91 11 6	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	26
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

91 11 6	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	26
91 11 6	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	26
		MAKE_BASE=TRUE		
91 11 6	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	26
91 11 6	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	26
91 11 6	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	26
91 11 6	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	26
91 11 6	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	26
91 11 6	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	26
91 11 6	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	26
91 11 6	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	26
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

91 11 6	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	26
91 11 6	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	26
		MAKE_BASE=TRUE		
91 11 6	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	26
91 11 6	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	26
91 11 6	MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	26
91 11 6	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	26
91 11 6	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	26
91 11 6	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	26
91 11 6	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	26
91 27 26 11 6	MEM_A_DQ<32>	MAKE_BASE=TRUE	MEM_A_DQ<32>	6 11 26 27 91

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

91 11 6	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	26
91 11 6	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	26
		MAKE_BASE=TRUE		
91 11 6	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	26
91 11 6	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	26
91 11 6	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	26
91 11 6	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	26
91 11 6	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	26
91 11 6	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	26
91 11 6	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	26
91 11 6	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	26
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

91 27 26 11 6	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	MEM_A_DQS_N<6>	6 11 26 27 91
91 27 26 11 6	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	MEM_A_DQS_P<6>	6 11 26 27 91
		MAKE_BASE=TRUE		
91 11 6	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	26
91 11 6	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	26
91 11 6	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	26
91 11 6	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	26
91 11 6	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	26
91 11 6	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	26
91 11 6	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	26
91 11 6	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	26
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

91 11 6	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	26
91 11 6	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	26
		MAKE_BASE=TRUE		
91 11 6	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	26
91 11 6	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	26
91 11 6	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	26
91 11 6	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	26
91 11 6	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	26
91 11 6	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	26
91 11 6	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	26
91 11 6	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	26
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

91 11 6	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	28
91 11 6	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	28
		MAKE_BASE=TRUE		
91 11 6	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	28
91 11 6	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	28
91 11 6	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	28
91 11 6	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	28
91 11 6	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	28
91 11 6	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	28
91 11 6	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	28
91 11 6	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	28
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

91 11 6	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	28
91 11 6	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	28
		MAKE_BASE=TRUE		
91 11 6	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	28
91 11 6	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	28
91 11 6	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	28
91 11 6	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	28
91 11 6	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	28
91 11 6	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	28
91 11 6	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	28
91 11 6	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	28
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

91 11 6	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	28
91 11 6	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	28
		MAKE_BASE=TRUE		
91 11 6	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	28
91 11 6	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	28
91 11 6	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	28
91 11 6	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	28
91 11 6	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	28
91 11 6	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	28
91 11 6	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	28
91 11 6	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	28
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

91 11 6	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	28
91 11 6	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	28
		MAKE_BASE=TRUE		
91 11 6	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	28
91 11 6	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	28
91 11 6	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	28
91 11 6	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	28
91 11 6	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	28
91 11 6	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	28
91 11 6	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	28
91 11 6	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	28
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

91 11 6	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	28
91 11 6	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	28
		MAKE_BASE=TRUE		
91 11 6	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	28
91 11 6	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	28
91 11 6	MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	28
91 11 6	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	28
91 11 6	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	28
91 11 6	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	28
91 11 6	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	28
27 11 6 91 28	MEM_B_DQ<32>	MAKE_BASE=TRUE	MEM_B_DQ<32>	6 11 27 28 91

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

91 11 6	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	28
91 11 6	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	28
		MAKE_BASE=TRUE		
91 11 6	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	28
91 11 6	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	28
91 11 6	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	28
91 11 6	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	28
91 11 6	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	28
91 11 6	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	28
91 11 6	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	28
91 11 6	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	28
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

27 11 6 91 28	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	MEM_B_DQS_N<6>	6 11 27 28 91
27 11 6 91 28	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	MEM_B_DQS_P<6>	6 11 27 28 91
		MAKE_BASE=TRUE		
91 11 6	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	28
91 11 6	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	28
91 11 6	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	28
91 11 6	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	28
91 11 6	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	28
91 11 6	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	28
91 11 6	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	28
91 11 6	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	28
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

91 11 6	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	28
91 11 6	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	28
		MAKE_BASE=TRUE		
91 11 6	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	28
91 11 6	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	28
91 11 6	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	28
91 11 6	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	28
91 11 6	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	28
91 11 6	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	28
91 11 6	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	28
91 11 6	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	28
		MAKE_BASE=TRUE		

SYNC_MASTER=K92_SUMA SYNC_DATE=05/10/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C3100 10UF 20% 6.3V X6S CERM 603
C3101 10UF 20% 6.3V X6S CERM 603
PLACE_NEAR=J3100.75:2.54mm

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123
0.1UF 20% 10V CERM 402
PLACE_NEAR=J3100.75:2.54mm
PLACE_NEAR=J3100.75:2.54mm

PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_B

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

PP3V3_S0

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

PP0V75_S0_DDRVTT

C3150 C3151 C3152 C3153
1UF 10% 10V X5R 402

J3100 DDR3-SODIMM (2 OF 2)

OMIT_TABLE

73	CKE0		CKE1	74	MEM_B_CKE<1>
75	VDD		VDD	76	
77	NC		A15	78	MEM_B_A<15>
79	BA2		A14	80	MEM_B_A<14>
81	VDD		VDD	82	
83	A12/BC*		A11	84	MEM_B_A<11>
85	A9		A7	86	MEM_B_A<7>
87	VDD		VDD	88	
89	A8		A6	90	MEM_B_A<6>
91	A5		A4	92	MEM_B_A<4>
93	VDD		VDD	94	
95	A3		A2	96	MEM_B_A<2>
97	A1		A0	98	MEM_B_A<0>
99	VDD		VDD	100	
101	CK0		CK1	102	MEM_B_CLK_P<1>
103	CK0*		CK1*	104	MEM_B_CLK_N<1>
105	VDD		VDD	106	
107	A10/AP		BA1	108	MEM_B_BA<1>
109	BA0		RAS*	110	MEM_B_RAS_L
111	VDD		VDD	112	
113	WE*		S0*	114	MEM_B_CS_L<0>
115	CAS*		ODT0	116	MEM_B_ODT<0>
117	VDD		VDD	118	
119	A13		ODT1	120	MEM_B_ODT<1>
121	S1*		NC	122	NC
123	VDD		VDD	124	
125	TEST		VREFCA	126	
127	VSS		VSS	128	
129	DQ32		DQ36	130	=MEM_B_DQ<36>
131	DQ33		DQ37	132	=MEM_B_DQ<37>
133	VSS		VSS	134	
135	DQS4*		DM4	136	
137	DQS4		VSS	138	
139	VSS		DQ38	140	=MEM_B_DQ<38>
141	DQ34		DQ39	142	=MEM_B_DQ<39>
143	DQ35		VSS	144	
145	VSS		DQ44	146	=MEM_B_DQ<44>
147	DQ40		DQ45	148	=MEM_B_DQ<45>
149	DQ41		VSS	150	
151	VSS		DQS5*	152	=MEM_B_DQS_N<5>
153	DM5		DQS5	154	=MEM_B_DQS_P<5>
155	VSS		VSS	156	
157	DQ42		DQ46	158	=MEM_B_DQ<46>
159	DQ43		DQ47	160	=MEM_B_DQ<47>
161	VSS		VSS	162	
163	DQ48		DQ52	164	=MEM_B_DQ<52>
165	DQ49		DQ53	166	=MEM_B_DQ<53>
167	VSS		VSS	168	
169	DQS6*		DM6	170	
171	DQS6		VSS	172	
173	VSS		DQ54	174	=MEM_B_DQ<54>
175	DQ50		DQ55	176	=MEM_B_DQ<55>
177	DQ51		VSS	178	
179	VSS		DQ60	180	=MEM_B_DQ<60>
181	DQ56		DQ61	182	=MEM_B_DQ<61>
183	DQ57		VSS	184	
185	VSS		DQS7*	186	=MEM_B_DQS_N<7>
187	DM7		DQS7	188	=MEM_B_DQS_P<7>
189	VSS		VSS	190	
191	DQ58		DQ62	192	=MEM_B_DQ<62>
193	DQ59		DQ63	194	=MEM_B_DQ<63>
195	VSS		VSS	196	
197	SA0		EVENT*	198	MEM_EVENT_L
199	VDDSPD		SDA	200	SMBUS_PCH_DATA
201	SA1		SCL	202	SMBUS_PCH_CLK
203	VTT		VTT	204	
205	MTG PIN		MTG PIN	206	
207	MTG PIN		MTG PIN	208	
209	MTG PIN		MTG PIN	210	
211	MTG PIN		MTG PIN	212	

MTG PINS

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

J3100 DDR3-SODIMM (1 OF 2)

OMIT_TABLE
CRITICAL

1	VREFDQ		VSS	2	
3	VSS		DQ4	4	=MEM_B_DQ<4>
5	DQ0		DQ5	6	=MEM_B_DQ<5>
7	DQ1		VSS	8	
9	VSS		DQS0*	10	=MEM_B_DQS_N<0>
11	DM0		DQS0	12	=MEM_B_DQS_P<0>
13	VSS		VSS	14	
15	DQ2		DQ6	16	=MEM_B_DQ<6>
17	DQ3		DQ7	18	=MEM_B_DQ<7>
19	VSS		VSS	20	
21	DQ8		DQ12	22	=MEM_B_DQ<12>
23	DQ9		DQ13	24	=MEM_B_DQ<13>
25	VSS		VSS	26	
27	DQS1*		DM1	28	
29	DQS1		RESET*	30	MEM_RESET_L
31	VSS		VSS	32	
33	DQ10		DQ14	34	=MEM_B_DQ<14>
35	DQ11		DQ15	36	=MEM_B_DQ<15>
37	VSS		VSS	38	
39	DQ16		DQ20	40	=MEM_B_DQ<20>
41	DQ17		DQ21	42	=MEM_B_DQ<21>
43	VSS		VSS	44	
45	DQS2*		DM2	46	
47	DQS2		VSS	48	
49	VSS		DQ22	50	=MEM_B_DQ<22>
51	DQ18		DQ23	52	=MEM_B_DQ<23>
53	DQ19		VSS	54	
55	VSS		DQ28	56	=MEM_B_DQ<28>
57	DQ24		DQ29	58	=MEM_B_DQ<29>
59	DQ25		VSS	60	
61	VSS		DQS3*	62	=MEM_B_DQS_N<3>
63	DM3		DQS3	64	=MEM_B_DQS_P<3>
65	VSS		VSS	66	
67	DQ26		DQ30	68	=MEM_B_DQ<30>
69	DQ27		DQ31	70	=MEM_B_DQ<31>
71	VSS		VSS	72	

516S0806

"Expansion" (bottom) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE
DDR3 SO-DIMM Connector B

Apple Inc.

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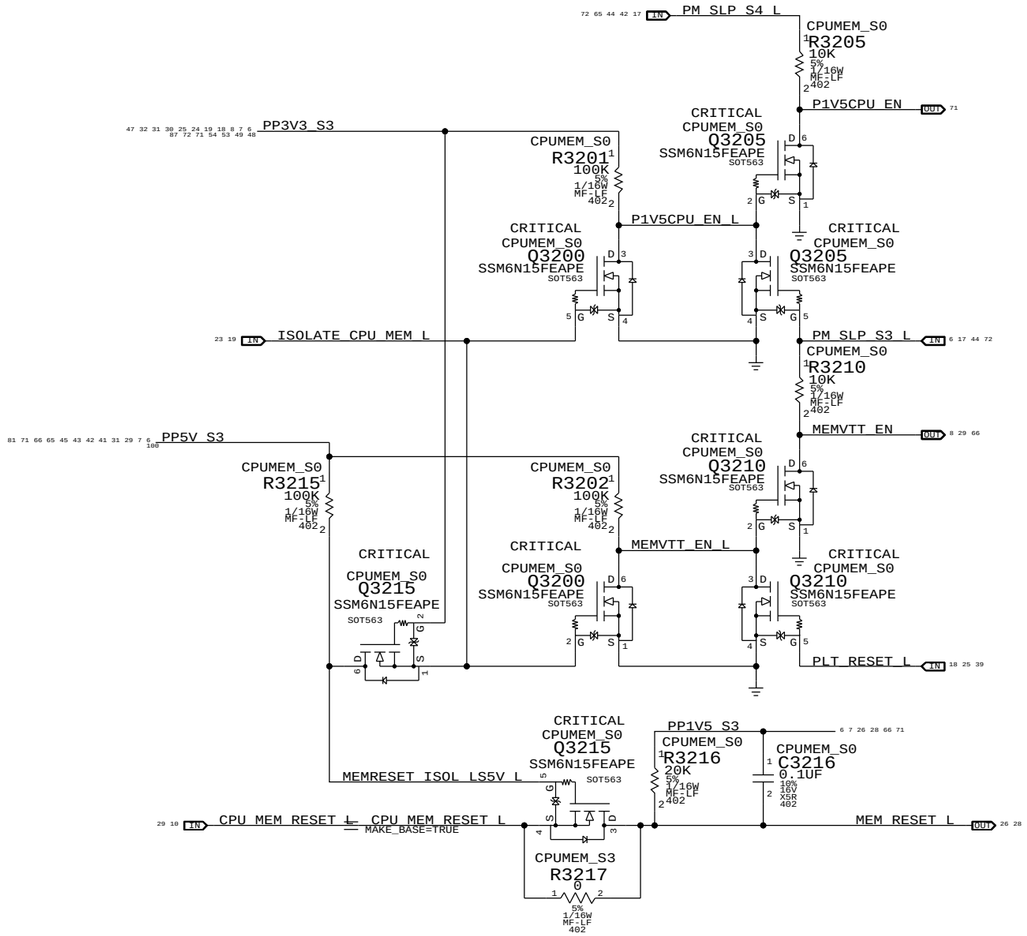
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

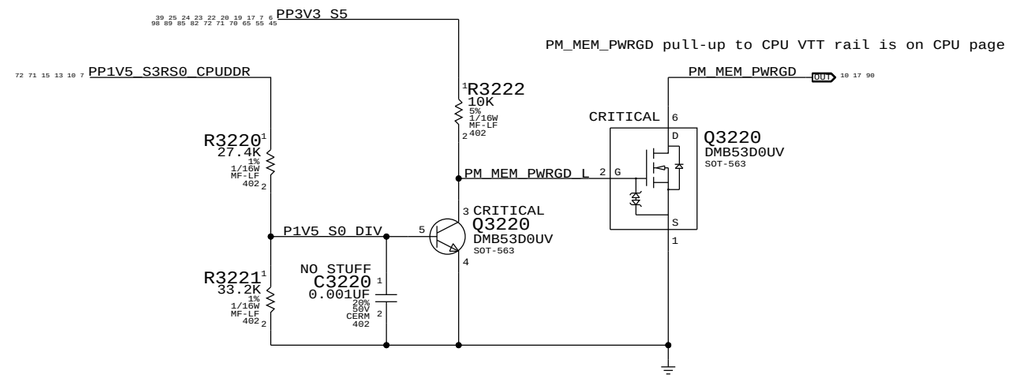


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

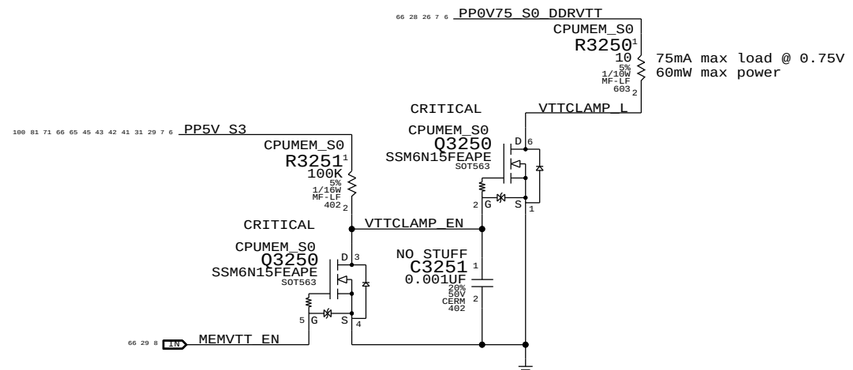
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

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Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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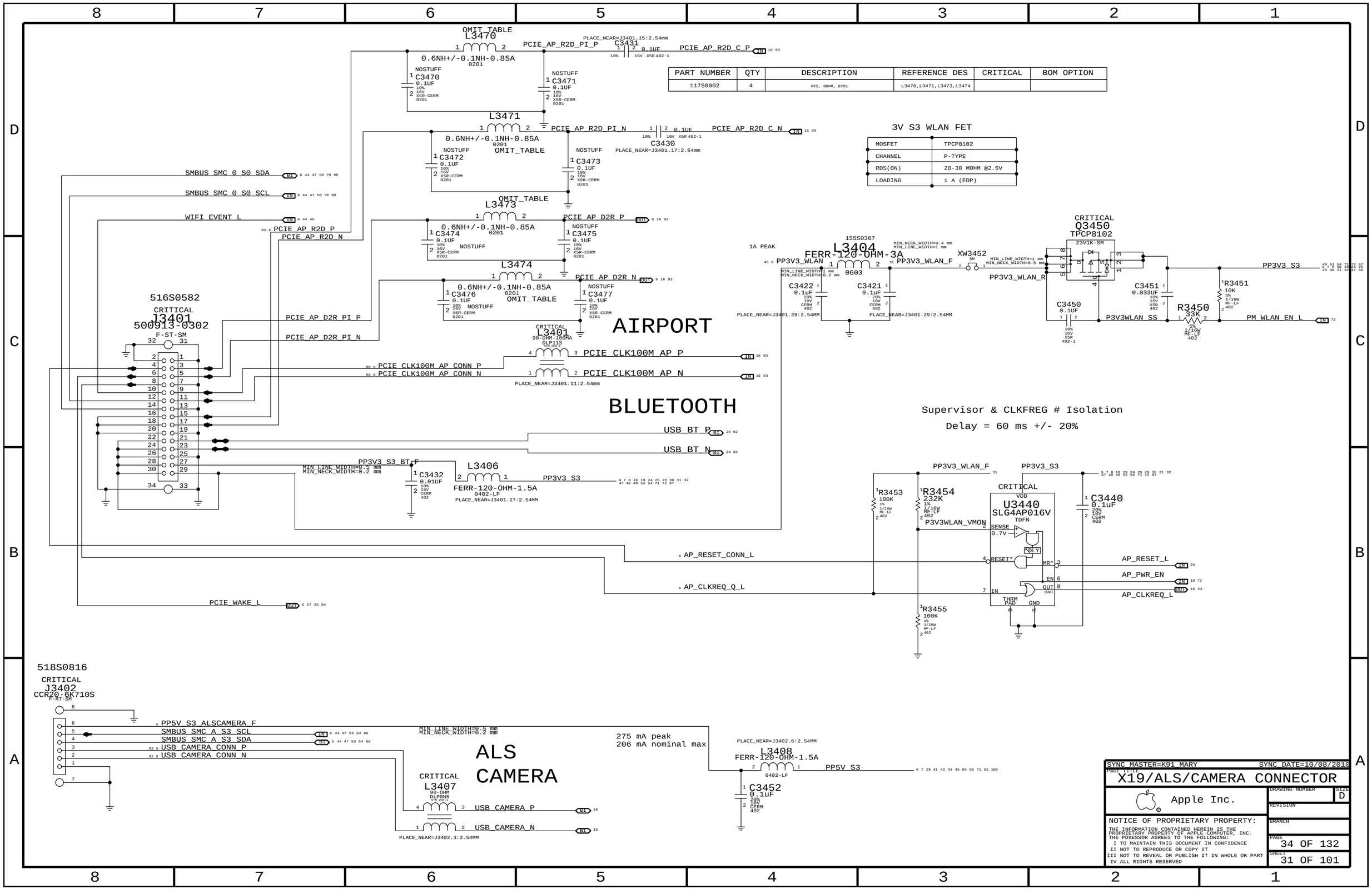
OMIT_TABLE
L3470
PCIE_AP_R2D_PI_P
PLACE_NEAR=J3401.15:2.54mm
C3431
PCIE_AP_R2D_C_P
0.6NH+/-0.1NH-0.85A
0201
NOSTUFF
C3470
0.1UF
NOSTUFF
C3471
0.1UF
L3471
PCIE_AP_R2D_PI_N
PCIE_AP_R2D_C_N
0.6NH+/-0.1NH-0.85A
C3430
C3472
0.1UF
OMIT_TABLE
NOSTUFF
C3473
0.1UF
PLACE_NEAR=J3401.17:2.54mm
SMBUS_SMC_0_S0_SDA
SMBUS_SMC_0_S0_SCL
WIFI_EVENT_L
PCIE_AP_R2D_P
PCIE_AP_R2D_N
OMIT_TABLE
L3473
PCIE_AP_D2R_P
0.6NH+/-0.1NH-0.85A
C3474
0.1UF
NOSTUFF
C3475
0.1UF
L3474
PCIE_AP_D2R_N
0.6NH+/-0.1NH-0.85A
C3476
0.1UF
OMIT_TABLE
NOSTUFF
C3477
0.1UF
516S0582
CRITICAL
J3401
500913-0302
F-ST-SM
PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N
CRITICAL
L3401
90-OHM-100MA
DLP11S
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_CONN_N
PLACE_NEAR=J3401.11:2.54mm
AIRPORT
BLUETOOTH
USB_BT_P
USB_BT_N
PP3V3_S3_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
C3432
0.01UF
L3406
FERR-120-OHM-1.5A
0402-LF
PP3V3_S3
PLACE_NEAR=J3401.27:2.54mm
AP_RESET_CONN_L
AP_CLKREQ_Q_L
PCIE_WAKE_L
PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION
117S0002 | 4 | RES, 0OHM, 0201 | L3470,L3471,L3473,L3474 | |
3V S3 WLAN FET
MOSFET | TPCP8102
CHANNEL | P-TYPE
RDS(ON) | 20-30 MOHM @2.5V
LOADING | 1 A (EDP)
1A PEAK
155S0367
L3404
FERR-120-OHM-3A
0603
PP3V3_WLAN
PP3V3_WLAN_F
XW3452
PP3V3_WLAN_R
C3422
0.1uF
C3421
0.1uF
PLACE_NEAR=J3401.29:2.54mm
CRITICAL
Q3450
TPCP8102
23V1K-SM
C3450
0.1UF
C3451
0.033UF
R3450
33K
R3451
10K
P3V3WLAN_SS
PP3V3_S3
PM_WLAN_EN_L
Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%
PP3V3_WLAN_F
PP3V3_S3
R3453
100K
R3454
232K
P3V3WLAN_VMON
CRITICAL
U3440
SLG4AP016V
TDFN
VDD
SENSE
0.7V
KDLY
RESET*
MR*
EN
OUT
IN
THRM PAD
GND
C3440
0.1uF
R3455
100K
AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L
518S0816
CRITICAL
J3402
CCR20-6K710S
F-RT-SM
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
ALS
CAMERA
CRITICAL
L3407
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
PLACE_NEAR=J3402.3:2.54mm
275 mA peak
206 mA nominal max
PLACE_NEAR=J3402.6:2.54mm
L3408
FERR-120-OHM-1.5A
0402-LF
PP5V_S3
C3452
0.1uF
SYNC_MASTER=K91_MARY
SYNC_DATE=10/08/2016
PAGE TITLE
X19/ALS/CAMERA CONNECTOR
Apple Inc.
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D
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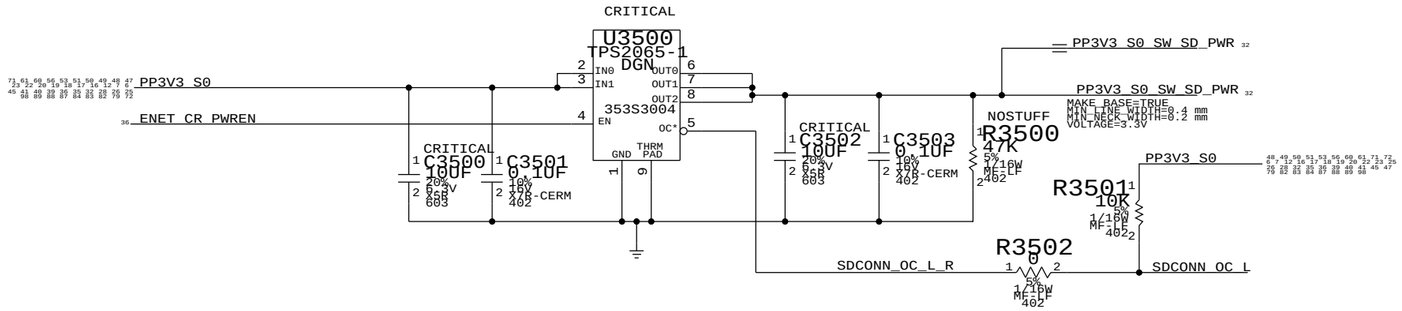
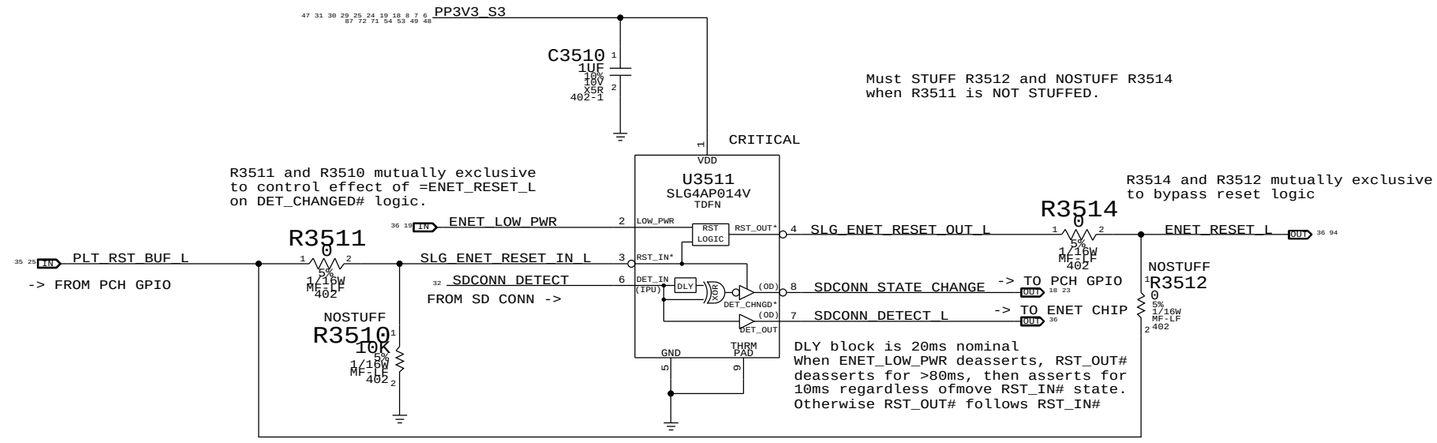
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

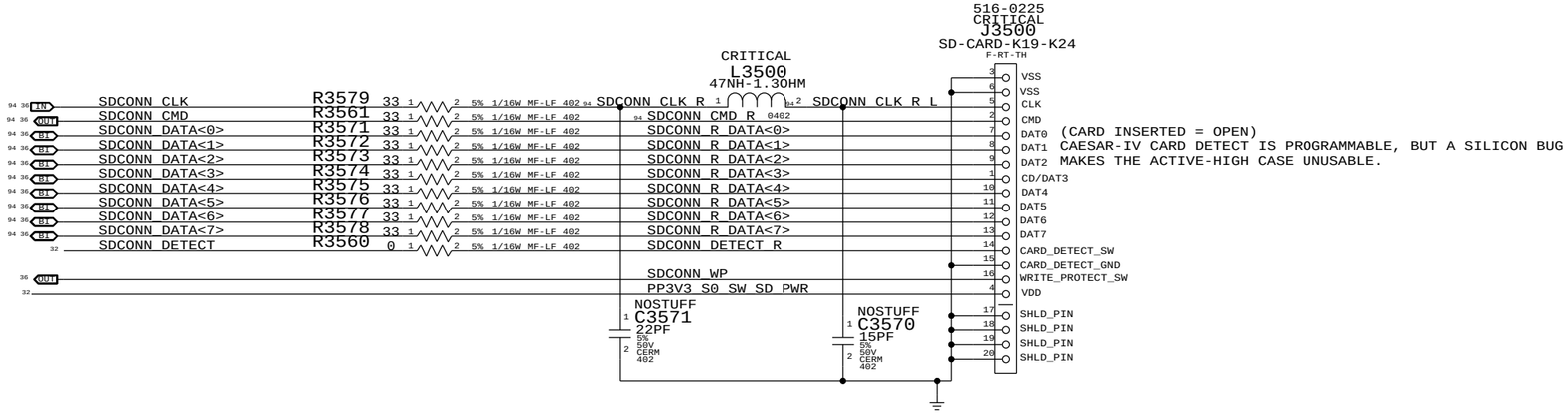
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO LATCH CIRCUIT



SD CARD CONNECTOR



SYNC MASTER=K91_ERIC SYNC DATE=10/08/2010

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

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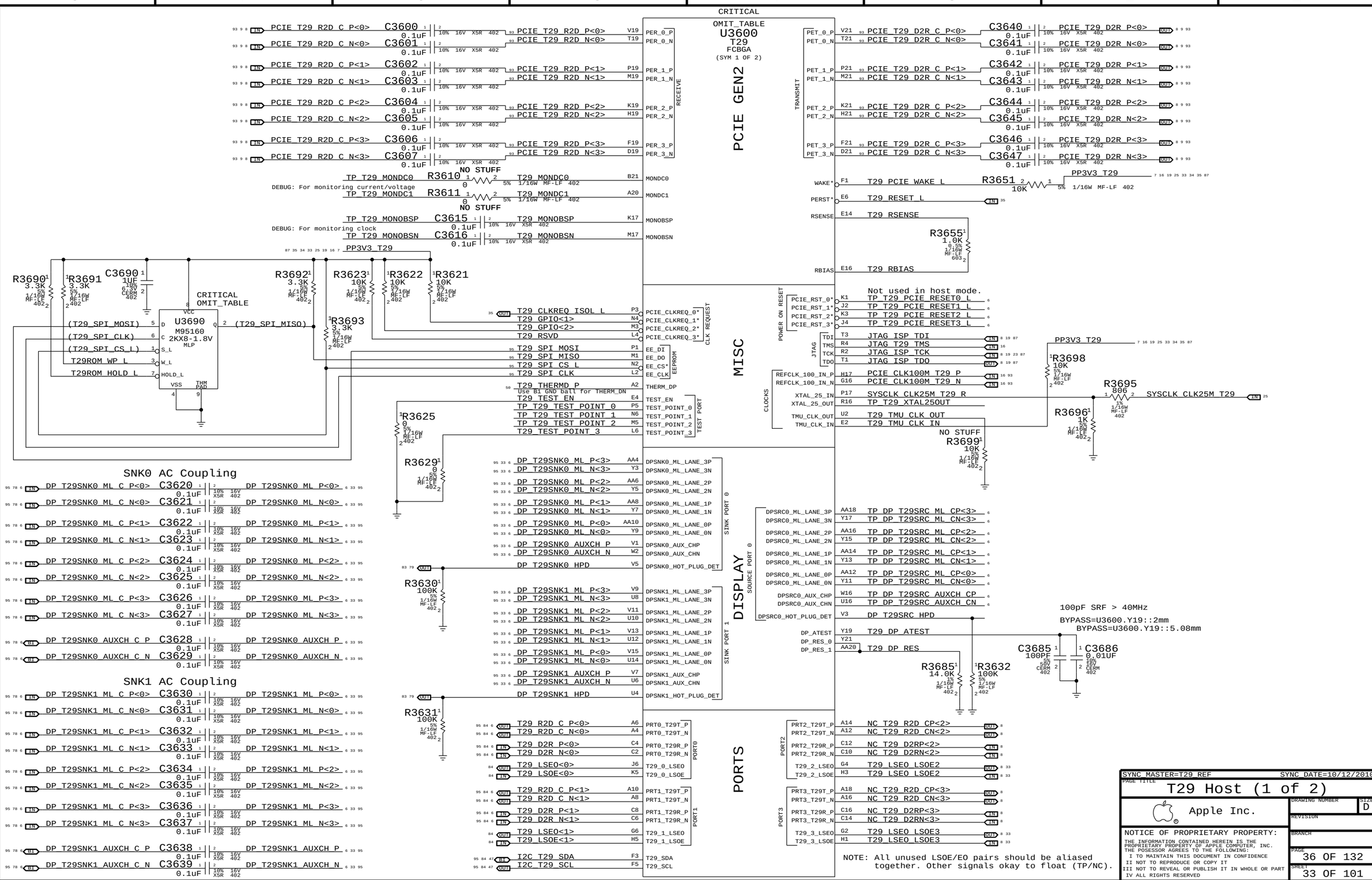
CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
PCIE T29 R2D C P<0> C3600 0.1uF PCIE T29 R2D P<0> V19 PER_0_P
PCIE T29 R2D C N<0> C3601 0.1uF PCIE T29 R2D N<0> T19 PER_0_N
PCIE T29 R2D C P<1> C3602 0.1uF PCIE T29 R2D P<1> P19 PER_1_P
PCIE T29 R2D C N<1> C3603 0.1uF PCIE T29 R2D N<1> M19 PER_1_N
PCIE T29 R2D C P<2> C3604 0.1uF PCIE T29 R2D P<2> K19 PER_2_P
PCIE T29 R2D C N<2> C3605 0.1uF PCIE T29 R2D N<2> H19 PER_2_N
PCIE T29 R2D C P<3> C3606 0.1uF PCIE T29 R2D P<3> F19 PER_3_P
PCIE T29 R2D C N<3> C3607 0.1uF PCIE T29 R2D N<3> D19 PER_3_N
PET_0_P V21 PCIE T29 D2R C P<0> C3640 0.1uF PCIE T29 D2R P<0>
PET_0_N T21 PCIE T29 D2R C N<0> C3641 0.1uF PCIE T29 D2R N<0>
PET_1_P P21 PCIE T29 D2R C P<1> C3642 0.1uF PCIE T29 D2R P<1>
PET_1_N M21 PCIE T29 D2R C N<1> C3643 0.1uF PCIE T29 D2R N<1>
PET_2_P K21 PCIE T29 D2R C P<2> C3644 0.1uF PCIE T29 D2R P<2>
PET_2_N H21 PCIE T29 D2R C N<2> C3645 0.1uF PCIE T29 D2R N<2>
PET_3_P F21 PCIE T29 D2R C P<3> C3646 0.1uF PCIE T29 D2R P<3>
PET_3_N D21 PCIE T29 D2R C N<3> C3647 0.1uF PCIE T29 D2R N<3>
NO STUFF
TP_T29_MONDC0 R3610 0 T29_MONDC0 B21 MONDC0
DEBUG: For monitoring current/voltage
TP_T29_MONDC1 R3611 0 T29_MONDC1 A20 MONDC1
NO STUFF
TP_T29_MONOBSP C3615 0.1uF T29_MONOBSP K17 MONOBSP
DEBUG: For monitoring clock
TP_T29_MONOBSN C3616 0.1uF T29_MONOBSN M17 MONOBSN
PP3V3_T29
WAKE* F1 T29_PCIE_WAKE_L R3651 10K PP3V3_T29
PERST* E6 T29_RESET_L
RSENSE E14 T29_RSENSE R3655 1.0K
RBIAS E16 T29_RBIAS
MISC
CLK REQUEST
EEPROM
TEST PORT
POWER ON RESET
JTAG
CLOCKS
Not used in host mode.
PCIE_RST_0* K1 TP_T29_PCIE_RESET0_L
PCIE_RST_1* J2 TP_T29_PCIE_RESET1_L
PCIE_RST_2* K3 TP_T29_PCIE_RESET2_L
PCIE_RST_3* J4 TP_T29_PCIE_RESET3_L
TDI T3 JTAG_ISP_TDI
TMS R4 JTAG_T29_TMS
TCK R2 JTAG_ISP_TCK
TDO T1 JTAG_ISP_TDO
REFCLK_100_IN_P H17 PCIE_CLK100M_T29_P
REFCLK_100_IN_N G16 PCIE_CLK100M_T29_N
XTAL_25_IN P17 SYSCLK_CLK25M_T29_R
XTAL_25_OUT R16 TP_T29_XTAL25OUT
TMU_CLK_OUT U2 T29_TMU_CLK_OUT
TMU_CLK_IN E2 T29_TMU_CLK_IN
PP3V3_T29
R3698 10K
R3695 806 SYSCLK_CLK25M_T29
R3696 1K
NO STUFF
R3699 10K
R3690 3.3K
R3691 3.3K
C3690 1UF
R3692 3.3K
R3693 3.3K
R3623 10K
R3622 10K
R3621 10K
CRITICAL
OMIT_TABLE
U3690
M95160
2KX8-1.8V
MLP
(T29_SPI_MOSI)
(T29_SPI_CLK)
(T29_SPI_CS_L)
T29ROM_WP_L
T29ROM_HOLD_L
(T29_SPI_MISO)
T29_CLKREQ_ISOL_L P3 PCIE_CLKREQ_0*
T29_GPIO<1> N4 PCIE_CLKREQ_1*
T29_GPIO<2> M3 PCIE_CLKREQ_2*
T29_RSVD L4 PCIE_CLKREQ_3*
T29_SPI_MOSI P1 EE_DI
T29_SPI_MISO M1 EE_DO
T29_SPI_CS_L N2 EE_CS*
T29_SPI_CLK L2 EE_CLK
T29_THERMD_P A2 THERM_DP
Use B1 GND ball for THERM_DN
T29_TEST_EN E4 TEST_EN
TP_T29_TEST_POINT_0 P5 TEST_POINT_0
TP_T29_TEST_POINT_1 N6 TEST_POINT_1
TP_T29_TEST_POINT_2 M5 TEST_POINT_2
T29_TEST_POINT_3 L6 TEST_POINT_3
R3625 0
R3629 0
DP_T29SNK0_ML_P<3> AA4 DPSNK0_ML_LANE_3P
DP_T29SNK0_ML_N<3> Y3 DPSNK0_ML_LANE_3N
DP_T29SNK0_ML_P<2> AA6 DPSNK0_ML_LANE_2P
DP_T29SNK0_ML_N<2> Y5 DPSNK0_ML_LANE_2N
DP_T29SNK0_ML_P<1> AA8 DPSNK0_ML_LANE_1P
DP_T29SNK0_ML_N<1> Y7 DPSNK0_ML_LANE_1N
DP_T29SNK0_ML_P<0> AA10 DPSNK0_ML_LANE_0P
DP_T29SNK0_ML_N<0> Y9 DPSNK0_ML_LANE_0N
DP_T29SNK0_AUXCH_P V1 DPSNK0_AUX_CHP
DP_T29SNK0_AUXCH_N W2 DPSNK0_AUX_CHN
DP_T29SNK0_HPD V5 DPSNK0_HOT_PLUG_DET
SINK PORT 0
R3630 100K
DP_T29SNK1_ML_P<3> V9 DPSNK1_ML_LANE_3P
DP_T29SNK1_ML_N<3> U8 DPSNK1_ML_LANE_3N
DP_T29SNK1_ML_P<2> V11 DPSNK1_ML_LANE_2P
DP_T29SNK1_ML_N<2> U10 DPSNK1_ML_LANE_2N
DP_T29SNK1_ML_P<1> V13 DPSNK1_ML_LANE_1P
DP_T29SNK1_ML_N<1> U12 DPSNK1_ML_LANE_1N
DP_T29SNK1_ML_P<0> V15 DPSNK1_ML_LANE_0P
DP_T29SNK1_ML_N<0> U14 DPSNK1_ML_LANE_0N
DP_T29SNK1_AUXCH_P V7 DPSNK1_AUX_CHP
DP_T29SNK1_AUXCH_N U6 DPSNK1_AUX_CHN
DP_T29SNK1_HPD U4 DPSNK1_HOT_PLUG_DET
SINK PORT 1
R3631 100K
DISPLAY
SOURCE PORT 0
DPSRC0_ML_LANE_3P AA18 TP_DP_T29SRC_ML_CP<3>
DPSRC0_ML_LANE_3N Y17 TP_DP_T29SRC_ML_CN<3>
DPSRC0_ML_LANE_2P AA16 TP_DP_T29SRC_ML_CP<2>
DPSRC0_ML_LANE_2N Y15 TP_DP_T29SRC_ML_CN<2>
DPSRC0_ML_LANE_1P AA14 TP_DP_T29SRC_ML_CP<1>
DPSRC0_ML_LANE_1N Y13 TP_DP_T29SRC_ML_CN<1>
DPSRC0_ML_LANE_0P AA12 TP_DP_T29SRC_ML_CP<0>
DPSRC0_ML_LANE_0N Y11 TP_DP_T29SRC_ML_CN<0>
DPSRC0_AUX_CHP W16 TP_DP_T29SRC_AUXCH_CP
DPSRC0_AUX_CHN U16 TP_DP_T29SRC_AUXCH_CN
DPSRC0_HOT_PLUG_DET V3 DP_T29SRC_HPD
100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm
DP_ATEST Y19 T29_DP_ATEST
DP_RES_0 Y21
DP_RES_1 AA20 T29_DP_RES
R3685 14.0K
R3632 100K
C3685 100PF
C3686 0.01UF
PORTS
PORT0
PORT1
PORT2
PORT3
T29_R2D_C_P<0> A6 PRT0_T29T_P
T29_R2D_C_N<0> A4 PRT0_T29T_N
T29_D2R_P<0> C4 PRT0_T29R_P
T29_D2R_N<0> C2 PRT0_T29R_N
T29_LSEO<0> J6 T29_0_LSEO
T29_LSOE<0> K5 T29_0_LSOE
T29_R2D_C_P<1> A10 PRT1_T29T_P
T29_R2D_C_N<1> A8 PRT1_T29T_N
T29_D2R_P<1> C8 PRT1_T29R_P
T29_D2R_N<1> C6 PRT1_T29R_N
T29_LSEO<1> G6 T29_1_LSEO
T29_LSOE<1> H5 T29_1_LSOE
I2C_T29_SDA F3 T29_SDA
I2C_T29_SCL F5 T29_SCL
NC_T29_R2D_CP<2> A14 PRT2_T29T_P
NC_T29_R2D_CN<2> A12 PRT2_T29T_N
NC_T29_D2RP<2> C12 PRT2_T29R_P
NC_T29_D2RN<2> C10 PRT2_T29R_N
T29_LSEO_LSOE2 G4 T29_2_LSEO
T29_LSEO_LSOE2 H3 T29_2_LSOE
NC_T29_R2D_CP<3> A18 PRT3_T29T_P
NC_T29_R2D_CN<3> A16 PRT3_T29T_N
NC_T29_D2RP<3> C16 PRT3_T29R_P
NC_T29_D2RN<3> C14 PRT3_T29R_N
T29_LSEO_LSOE3 G2 T29_3_LSEO
T29_LSEO_LSOE3 H1 T29_3_LSOE
NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).
SNK0 AC Coupling
DP_T29SNK0_ML_C_P<0> C3620 0.1uF DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_C_N<0> C3621 0.1uF DP_T29SNK0_ML_N<0>
DP_T29SNK0_ML_C_P<1> C3622 0.1uF DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_C_N<1> C3623 0.1uF DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_C_P<2> C3624 0.1uF DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_C_N<2> C3625 0.1uF DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_C_P<3> C3626 0.1uF DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_C_N<3> C3627 0.1uF DP_T29SNK0_ML_N<3>
DP_T29SNK0_AUXCH_C_P C3628 0.1uF DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_C_N C3629 0.1uF DP_T29SNK0_AUXCH_N
SNK1 AC Coupling
DP_T29SNK1_ML_C_P<0> C3630 0.1uF DP_T29SNK1_ML_P<0>
DP_T29SNK1_ML_C_N<0> C3631 0.1uF DP_T29SNK1_ML_N<0>
DP_T29SNK1_ML_C_P<1> C3632 0.1uF DP_T29SNK1_ML_P<1>
DP_T29SNK1_ML_C_N<1> C3633 0.1uF DP_T29SNK1_ML_N<1>
DP_T29SNK1_ML_C_P<2> C3634 0.1uF DP_T29SNK1_ML_P<2>
DP_T29SNK1_ML_C_N<2> C3635 0.1uF DP_T29SNK1_ML_N<2>
DP_T29SNK1_ML_C_P<3> C3636 0.1uF DP_T29SNK1_ML_P<3>
DP_T29SNK1_ML_C_N<3> C3637 0.1uF DP_T29SNK1_ML_N<3>
DP_T29SNK1_AUXCH_C_P C3638 0.1uF DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH_C_N C3639 0.1uF DP_T29SNK1_AUXCH_N
SYNC_MASTER=T29_REF
SYNC_DATE=10/12/2010
PAGE TITLE
T29 Host (1 of 2)
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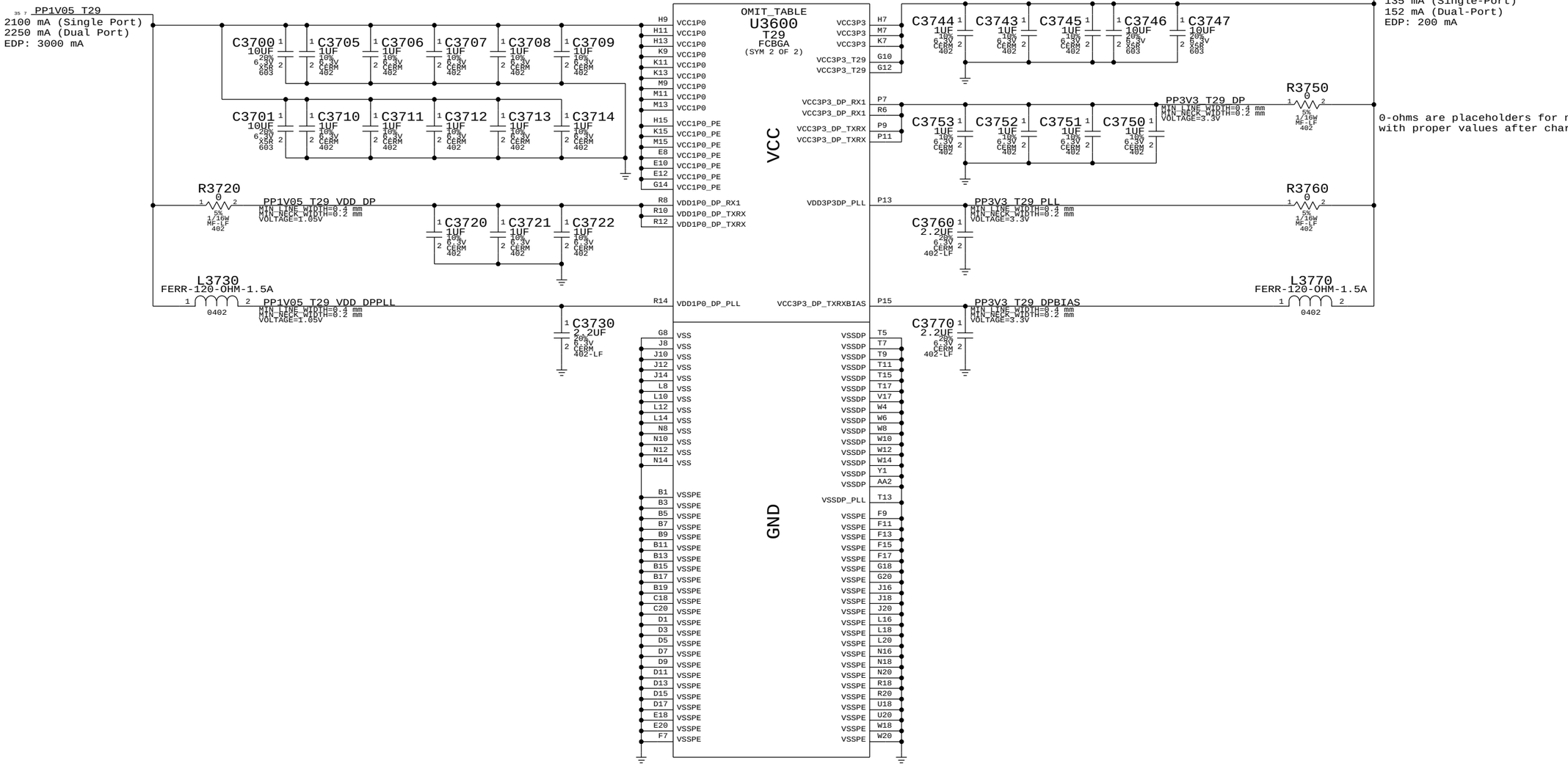

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE: T29 Host (2 of 2)

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required for 2S.

CRITICAL
T29BST:Y
Q3880
SI8409DB
86A

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

T29BST:Y R3880 470K 5% 1/16W MF-LF 402
T29BST:Y C3880 0.1UF 10% 16V X5R 402
T29BST_PWREN_DIV_L
T29BST:Y R3881 330K 5% 1/10W MF-LF 402
T29BST_PWREN_L
T29BST:Y Q3805 SSM3K15FV SOD-VESM-HF
T29_A_HV_EN

T29BST:Y C3890 10UF 10% 25V X5R 805
T29BST:Y C3891 10UF 10% 25V X5R 805
T29BST:Y R3891 200K 1% 1/10W MF-LF 402 <R1>
T29BST_EN_UVLO

CRITICAL
T29BST:Y
L3895
10UH-4A-68-MOHM
PCMB063T-100MS

T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
T29BST:Y
U3890
LT3957
QFN

VIN
SW
SNS1
SNS2
FBX
NC
INTVCC
VC
RT
SS
SYNC
SGND
GND

T29BST_SNS1
T29BST:Y R3889 0 5% 1/10W MF-LF 402
CRITICAL
T29BST:Y D3895 POWERDI-123 DFLS230L
T29BST_SNS2
XW3895 SM
PLACE_NEAR=C3895.1:2 mm
T29BST_VSNS
T29BST:Y R3895 137K 1% 1/10W MF-LF 402 <Ra>
T29BST_FBX
T29BST:Y R3896 15.8K 1% 1/10W MF-LF 402 <Rb>

T29BST:Y C3888 10PF 5% 50V CERM 402
NO STUFF
T29BST:Y C3889 100PF 5% 50V CERM 402

T29BST:Y C3892 4.7UF 10% 10V X5R 805
T29BST:Y C3887 47PF 5% 50V CERM 402
T29BST:Y R3893 10K 1% 1/10W MF-LF 402
T29BST_VC_RC
T29BST:Y C3893 3300PF 10% 50V X7R-CERM 0402
T29BST:Y R3894 41.2K 1% 1/10W MF-LF 402
T29BST:Y R3892 73.2K 1% 1/10W MF-LF 402 <R2>
T29BST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

GND_T29BST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

T29BST:Y C3895 4.7UF 10% 10V X7R-CERM 1206
T29BST:Y C3896 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3897 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3898 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3899 0.001UF 10% 50V X7R 402

PP15V_T29
Vout = 15V
Max Current = 0.8A
Freq = 300KHz

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

Supervisor & CLKREQ# Isolation

PP3V3_S0
C3800 0.1UF 10% 16V X5R 402

CRITICAL
U3800
SLG4AP016V
TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
GND
THRM PAD

PP3V3_T29
T29BST:Y R3807 100K 5% 1/10W MF-LF 402
PP1V05_T29

Platform (PCIe) Reset
PLT_RST_BUF_L
R3803 10K 5% 1/10W MF-LF 402
Open-Drain GPIO
T29_SW_RESET_L
T29_RESET_L
DLY = 60 ms +/- 20%
T29_CLKREQ_L
Pull-up provided by SB page.
T29_CLKREQ_ISOL_L
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE

T29BST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
T29BST:Y R3888 330K 5% 1/10W MF-LF 402
T29BST_SHDN_DIV
T29BST:Y R3887 330K 5% 1/10W MF-LF 402
T29BST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

3.3V T29 Switch

PP3V3_S0
U3810
TPS22924
CSP
A2 B2 C2 A1 B1 C1
VIN VOUT ON GND
CRITICAL
C3810 1UF 10% 6.3V CERM 402
PP3V3_T29
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

PP1V05_S0
U3815
TPS22924
CSP
CRITICAL
C3815 1UF 10% 6.3V CERM 402
PP1V05_T29
Max Current = 3.4A (85C)

U3816
TPS22924
CSP
CRITICAL
T29_PWR_EN
Pull-up provided by SB page.
U3816.A2: PLACE_NEAR=U3815.B2:3 mm

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2016

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T29 Power Support

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG

CRITICAL L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH — C3900 0.1UF
CRITICAL L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH — C3905 0.1UF
CRITICAL L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH — R3910 4.7K, C3910 0.1UF, C3911 0.1UF

R3940 4.7K, R3941 4.7K, C3915 4.7UF, C3916 0.1UF

ENET_SR_LX
PP1V2_ENET
Internal 1.2V Switching Regulator pins.

PP1V2_ENET
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL — C3921 0.1UF, C3920 4.7UF
CRITICAL L3925 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL — C3926 0.1UF, C3925 4.7UF
CRITICAL L3930 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL — C3931 0.1UF, C3930 4.7UF
C3936 0.1UF, CRITICAL C3935 10UF

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3_S0
R3942 1K Current Limiting Resistor
C3950 0.1uF, C3951 0.1uF, C3955 0.1uF, C3956 0.1uF, R3943 0

OMIT
U3900
BCM57765B0
QFN-8X8

PCIE_ENET_D2R_N	PCIE_TXD_N	ENET_MDI_P<0>	TRD0_P
PCIE_ENET_D2R_P	PCIE_TXD_P	ENET_MDI_N<0>	TRD0_N
PCIE_ENET_R2D_P	PCIE_RXD_P	ENET_MDI_P<1>	TRD1_P
PCIE_ENET_R2D_N	PCIE_RXD_N	ENET_MDI_N<1>	TRD1_N
PCIE_CLK100M_ENET_P	PCIE_REFCLK_P	ENET_MDI_P<2>	TRD2_P
PCIE_CLK100M_ENET_N	PCIE_REFCLK_N	ENET_MDI_N<2>	TRD2_N
ENET_RESET_L	PERST* (IPD)	ENET_MDI_P<3>	TRD3_P
ENET_CLKREQ_L	CLKREQ* (OD)	ENET_MDI_N<3>	TRD3_N
ENET_WAKE_R_L	WAKE* (OD)		
ENET_LOW_PWR	LOW_PWR (IPD)		
BCM57765_SMB_CLK	SMB_CLK		
BCM57765_SMB_DATA	SMD_DATA (IPD)		
BCM57765_SCLK	SCLK		
BCM57765_MISO	SI/LINKLED*		
BCM57765_MOSI	SO		
BCM57765_CS_L	CS*		
TP_BCM57765_SPD100LED_L	SPD100LED*/SERIAL_DO (OD)		
TP_BCM57765_TRAFFICLED_L	TRAFFICLED*/SERIAL_DI (OD)		
SYSCLK_CLK25M_ENET	XTALI		
NC	XTALO		
BCM57765_RDAC	RDAC		
	THRM_PAD		

GPIO_0	NC	
GPIO_1/CR_BUS_PWR		ENET_MEDIA_SENSE
RE*/GPIO_2		SDCONN_DETECT_L
(IPU) DETECT/WE*		SDCONN_CMD
(IPU) CR_CMD/CLE		SDCONN_CLK
CR_CLK/RY_BY*		SDCONN_DATA<0>
CR_DATA0		SDCONN_DATA<1>
CR_DATA1		SDCONN_DATA<2>
CR_DATA2		SDCONN_DATA<3>
CR_DATA3		SDCONN_DATA<4>
CR_DATA4		SDCONN_DATA<5>
CR_DATA5		SDCONN_DATA<6>
CR_DATA6		SDCONN_DATA<7>
CR_DATA7		
CE*/MS_INS*	TP_CE_L_MS_INS_L	
CR_LED/ALE	ENET_CR_PWREN	
CR_WP*/XD_WP*		SDCONN_WP
XD_DETECT	BDM57765_SR_DISABLE	

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

PP3V3R1V8_ENET_LR_OUT_REG
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C3970 4.7UF, C3971 0.1UF, C3972 0.1UF

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3980 1K

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

PP3V3_ENET
C3990 0.1UF
U3990 AT45DB011D SOIC-8S1 OMIT
BCM57765_SCLK, BCM57765_CS_L, BCM57765_MOSI, BCM57765_MISO
NOSTUFF R3990 4.7K, R3997 4.7K

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K91_ERIC SYNC_DATE=10/11/2010
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ETHERNET PHY (CAESAR IV)
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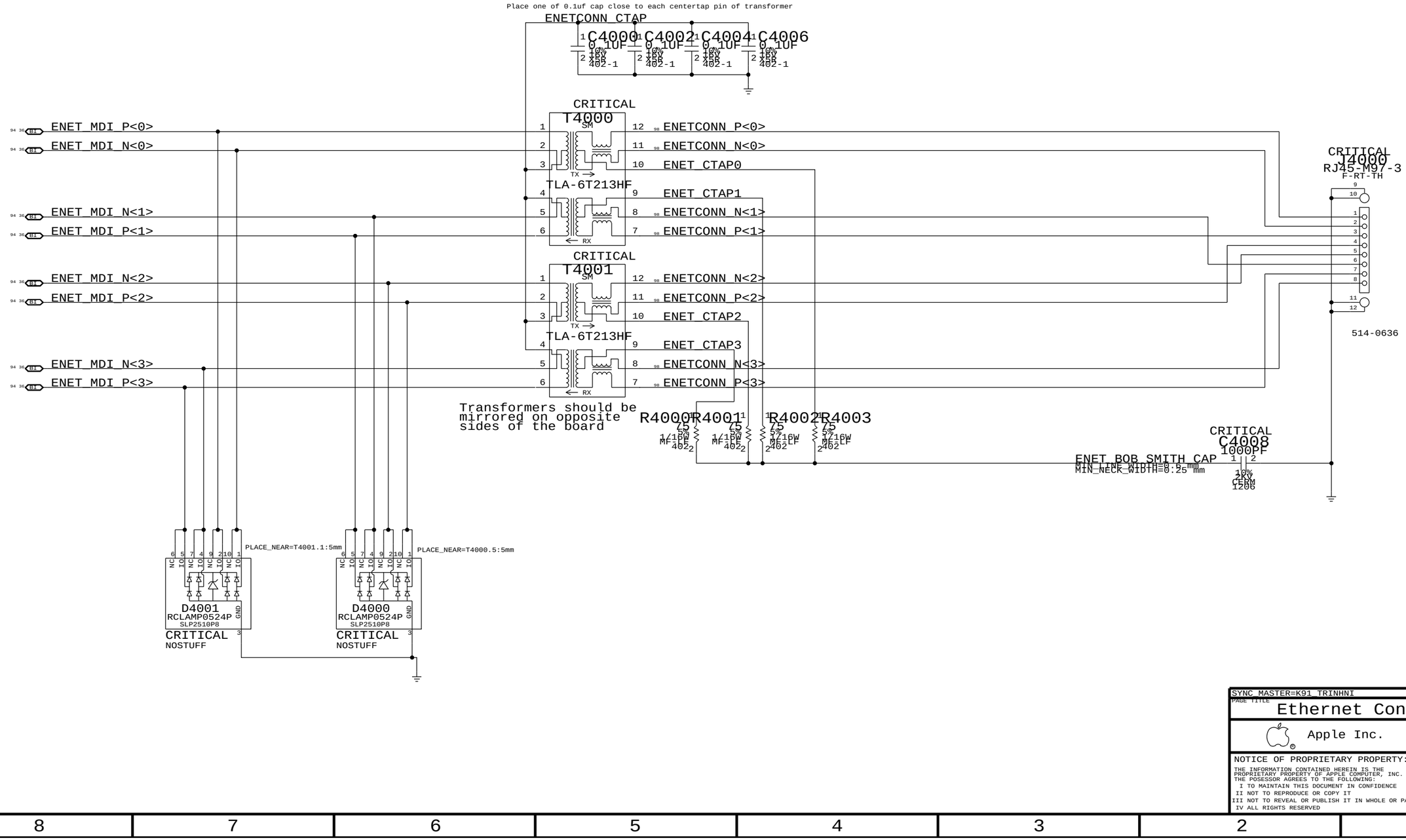
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_TRINHNI SYNC_DATE=05/26/2010

PAGE TITLE
Ethernet Connector

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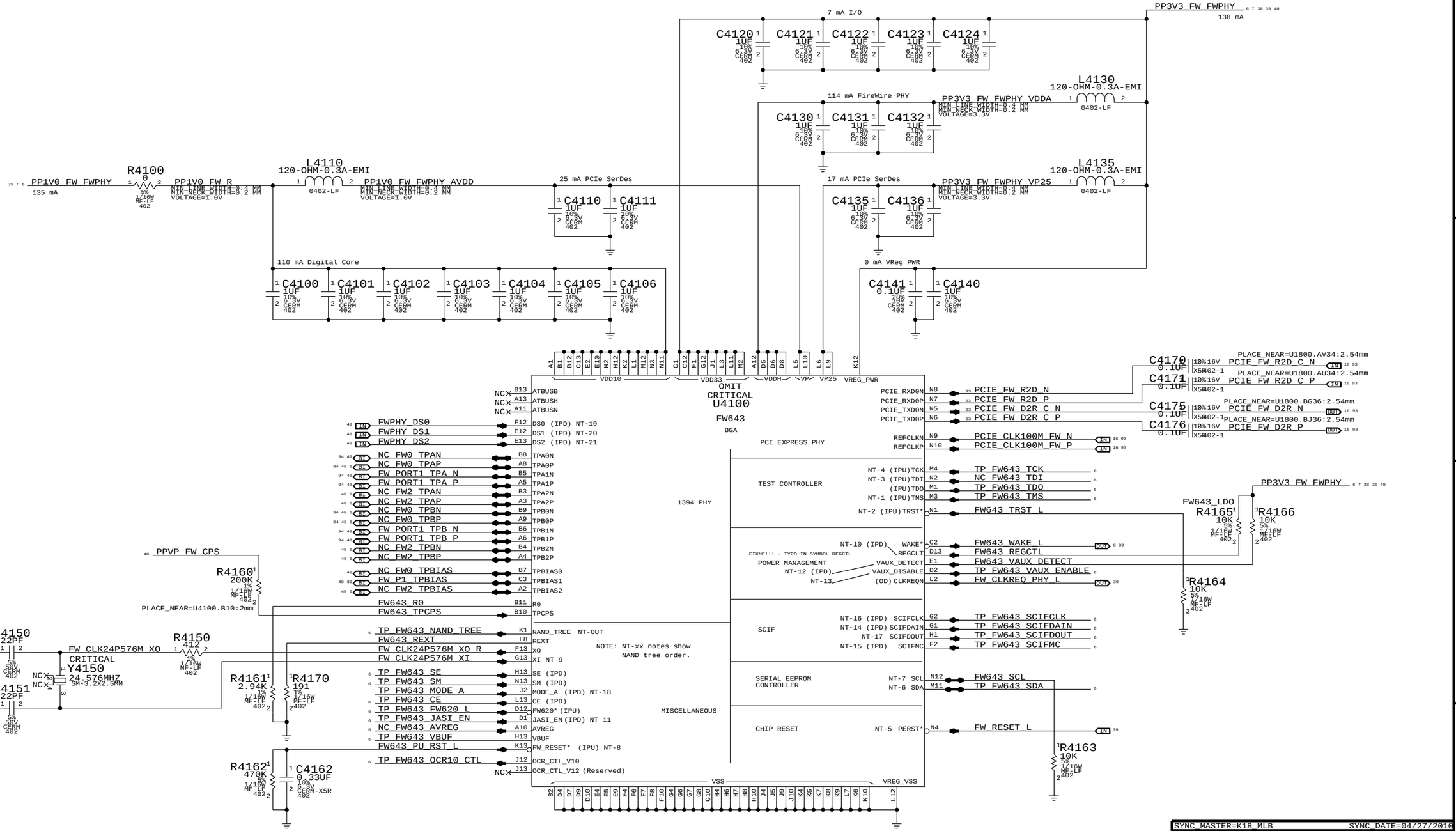
PP1V0_FW_FWPHY
135 mA
R4100
0
1/10W
MF-LF
402
PP1V0_FW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
L4110
120-OHM-0.3A-EMI
0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402
110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402
7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY
138 mA
L4130
120-OHM-0.3A-EMI
114 mA FireWire PHY
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
0402-LF
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402
L4135
120-OHM-0.3A-EMI
17 mA PCIe SerDes
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
0402-LF
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402
0 mA VReg PWR
C4141 0.1UF 20% 16V CERM 402
C4140 1UF 10% 6.3V CERM 402
VDD10
VDD33
VDDH
VP
VP25
VREG_PWR
OMIT
CRITICAL
U4100
FW643
BGA
NC ATBUSB
NC ATBUSH
NC ATBUSN
FWPHY_DS0 DS0 (IPD) NT-19
FWPHY_DS1 DS1 (IPD) NT-20
FWPHY_DS2 DS2 (IPD) NT-21
NC_FW0_TPAN TPA0N
NC_FW0_TPAP TPA0P
FW_PORT1_TPA_N TPA1N
FW_PORT1_TPA_P TPA1P
NC_FW2_TPAN TPA2N
NC_FW2_TPAP TPA2P
NC_FW0_TPBN TPB0N
NC_FW0_TPBP TPB0P
FW_PORT1_TPB_N TPB1N
FW_PORT1_TPB_P TPB1P
NC_FW2_TPBN TPB2N
NC_FW2_TPBP TPB2P
NC_FW0_TPBIAS TPBIAS0
FW_P1_TPBIAS TPBIAS1
NC_FW2_TPBIAS TPBIAS2
PCI EXPRESS PHY
PCIE_RXD0N PCIE_FW_R2D_N
PCIE_RXD0P PCIE_FW_R2D_P
PCIE_TXD0N PCIE_FW_D2R_C_N
PCIE_TXD0P PCIE_FW_D2R_C_P
C4170 0.1UF 10% 16V X5R 402-1 PCIE_FW_R2D_C_N
C4171 0.1UF 10% 16V X5R 402-1 PCIE_FW_R2D_C_P
C4175 0.1UF 10% 16V X5R 402-1 PCIE_FW_D2R_N
C4176 0.1UF 10% 16V X5R 402-1 PCIE_FW_D2R_P
PLACE_NEAR=U1800.AV34:2.54mm
PLACE_NEAR=U1800.AU34:2.54mm
PLACE_NEAR=U1800.BG36:2.54mm
PLACE_NEAR=U1800.BJ36:2.54mm
REFCLKN PCIE_CLK100M_FW_N
REFCLKP PCIE_CLK100M_FW_P
1394 PHY
TEST CONTROLLER
NT-4 (IPU) TCK TP_FW643_TCK
NT-3 (IPU) TDI NC_FW643_TDI
(IPU) TDO TP_FW643_TDO
NT-1 (IPU) TMS TP_FW643_TMS
NT-2 (IPU) TRST* FW643_TRST_L
PP3V3_FW_FWPHY
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
R4163 10K 5% 1/16W MF-LF 402
POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
NT-10 (IPD) WAKE* FW643_WAKE_L
REGCLT FW643_REGCTL
NT-12 (IPD) VAUX_DETECT FW643_VAUX_DETECT
NT-13 VAUX_DISABLE TP_FW643_VAUX_ENABLE
(OD) CLKREQN FW_CLKREQ_PHY_L
SCIF
NT-16 (IPD) SCIFCLK TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN TP_FW643_SCIFDAIN
NT-17 SCIFDOUT TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC TP_FW643_SCIFMC
SERIAL EEPROM CONTROLLER
NT-7 SCL FW643_SCL
NT-6 SDA TP_FW643_SDA
CHIP RESET
NT-5 PERST* FW_RESET_L
MISCELLANEOUS
PPVP_FW_CPS
R4160 200K 1% 1/16W MF-LF 402
PLACE_NEAR=U4100.B10:2mm
FW643_R0
FW643_TPCPS
C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
CRITICAL
Y4150 24.576MHZ SM-3.2X2.5MMZ
R4150 412 1% 1/16W MF-LF 402
R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402
TP_FW643_NAND_TREE NAND_TREE NT-OUT
FW643_REXT REXT
FW_CLK24P576M_XO_R XO
FW_CLK24P576M_XI XI NT-9
TP_FW643_SE SE (IPD)
TP_FW643_SM SM (IPD)
TP_FW643_MODE_A MODE_A (IPD) NT-18
TP_FW643_CE CE (IPD)
TP_FW643_FW620_L FW620* (IPU)
TP_FW643_JASI_EN JASI_EN (IPD) NT-11
NC_FW643_AVREG AVREG
TP_FW643_VBUF VBUF
FW643_PU_RST_L FW_RESET* (IPU) NT-8
TP_FW643_OCR10_CTL OCR_CTL_V10
OCR_CTL_V12 (Reserved)
NOTE: NT-xx notes show NAND tree order.
VSS
VREG_VSS
SYNC_MASTER=K18_MLB
SYNC_DATE=04/27/2010
PAGE TITLE
FireWire LLC/PHY (FW643)
Apple Inc.
DRAWING NUMBER
SIZE D
REVISION
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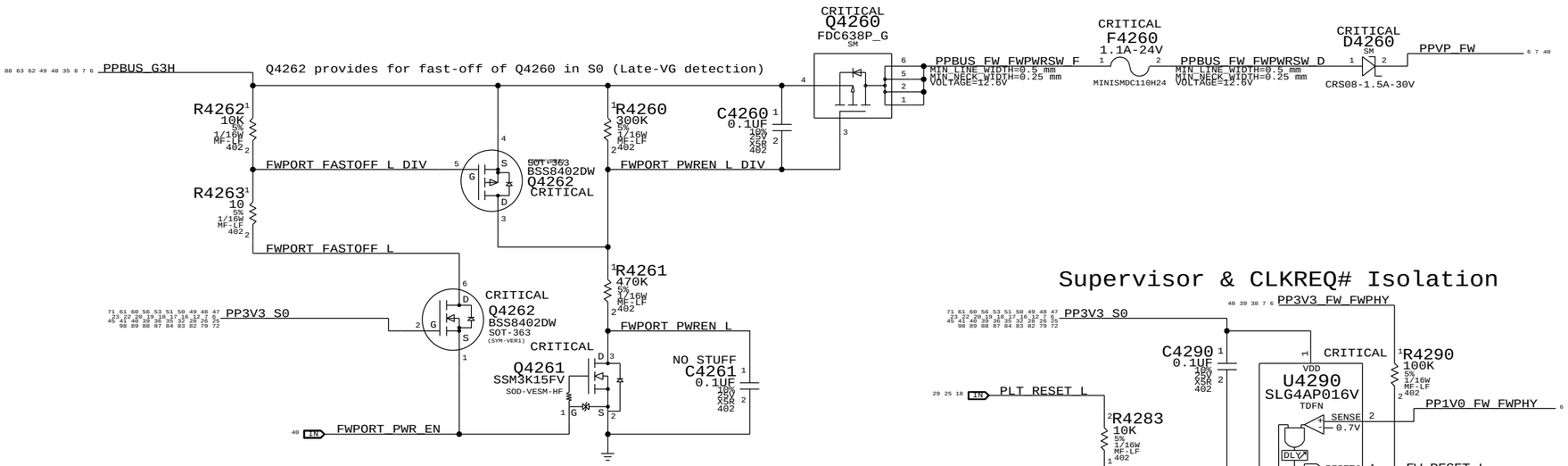
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

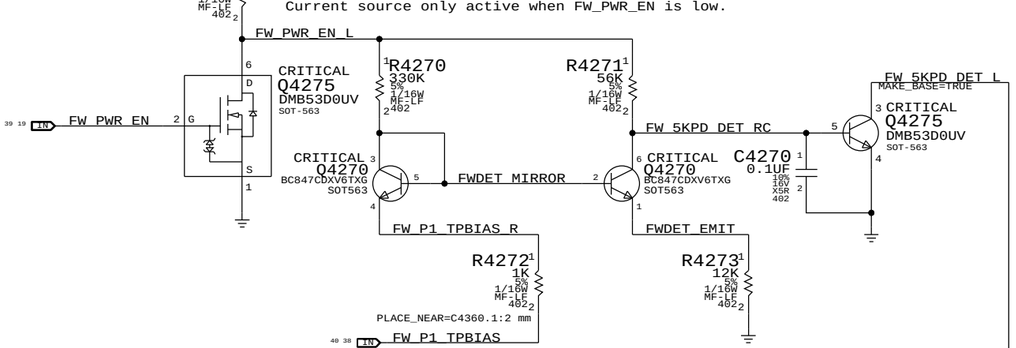
FireWire Port Power Switch



Supervisor & CLKREQ# Isolation

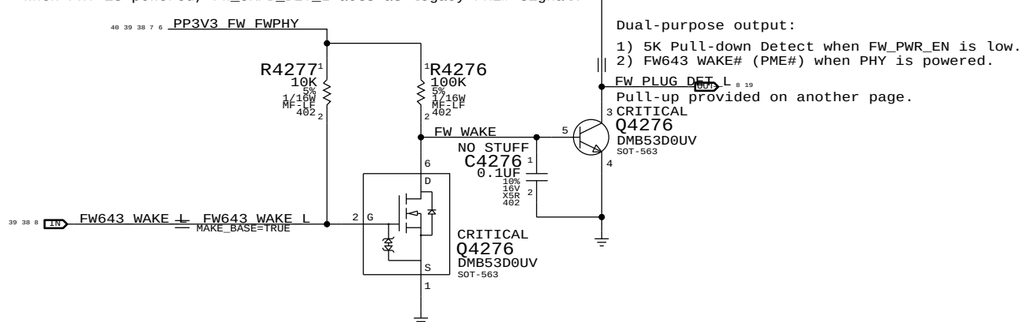
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

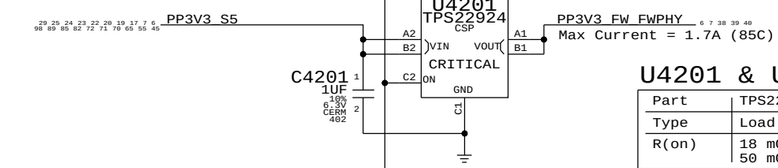


FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



3.3V FW Switch

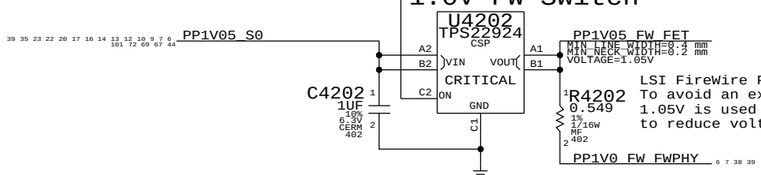


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

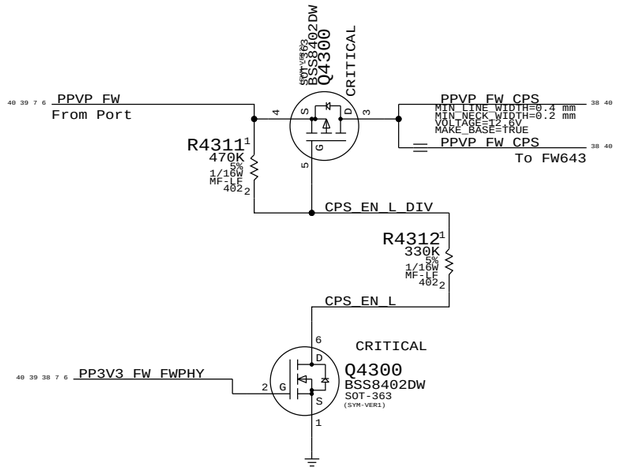
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

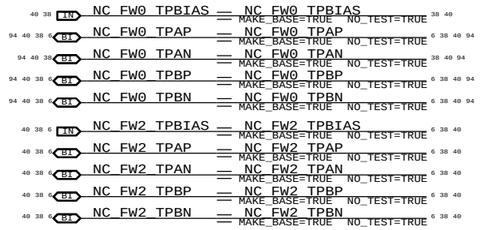
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



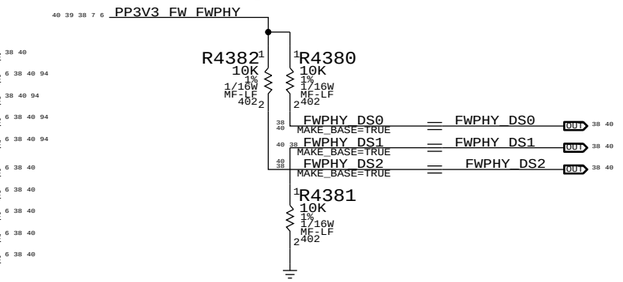
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



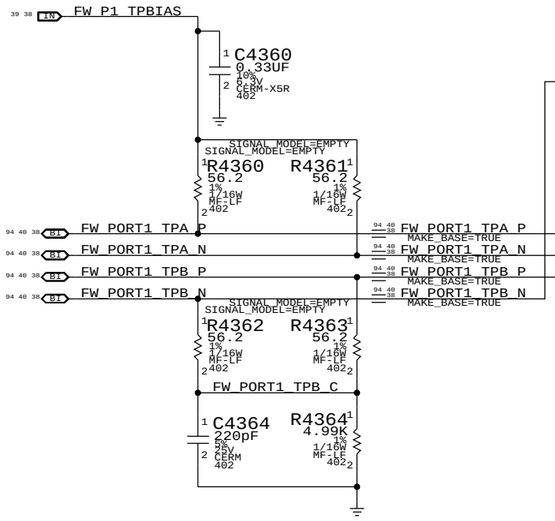
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

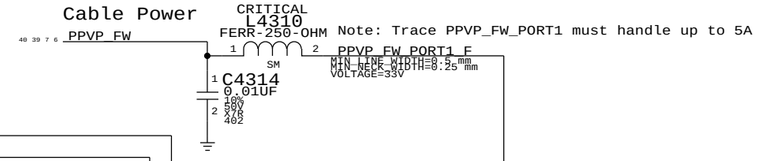


Termination

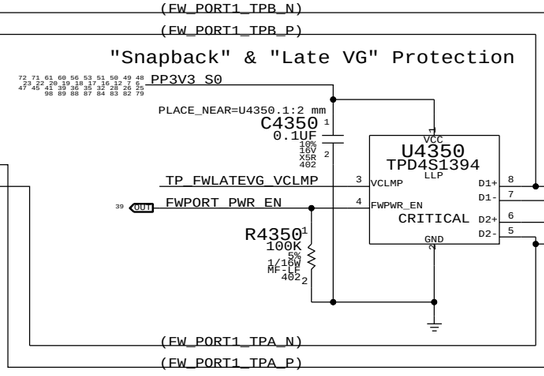
Place close to FireWire PHY



Cable Power

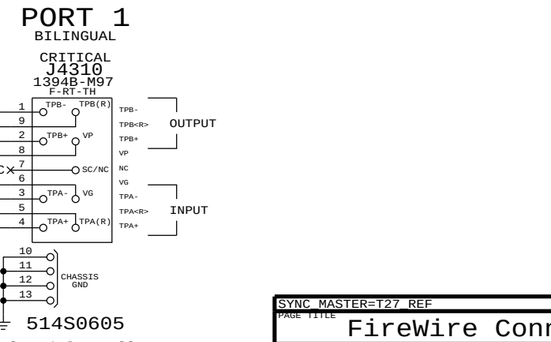


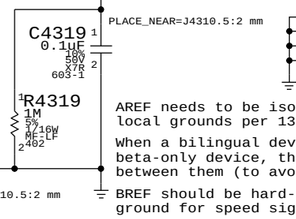
"Snapback" & "Late VG" Protection



PORT 1

BILINGUAL





AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE: FireWire Connector

Apple Inc.

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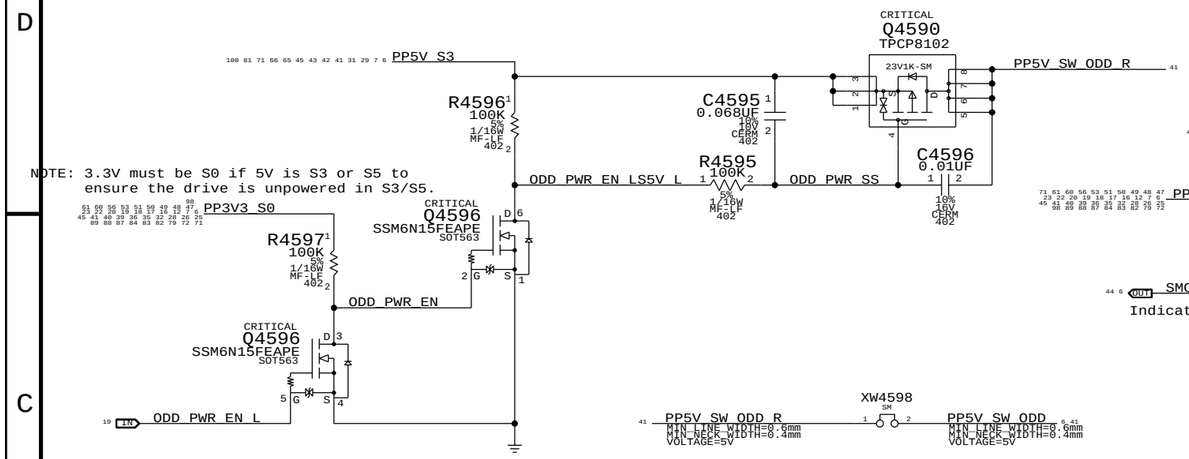
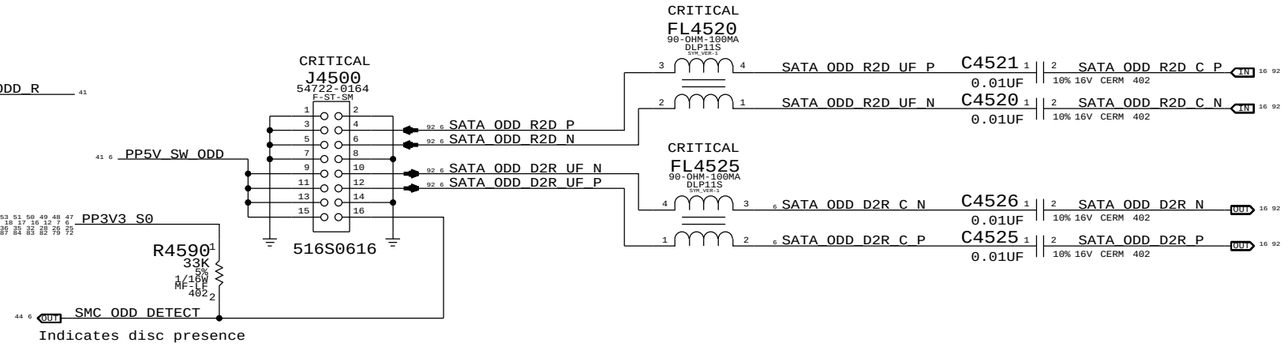
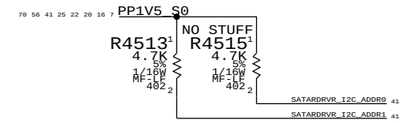
ODD Power Control



SATA ODD Connector

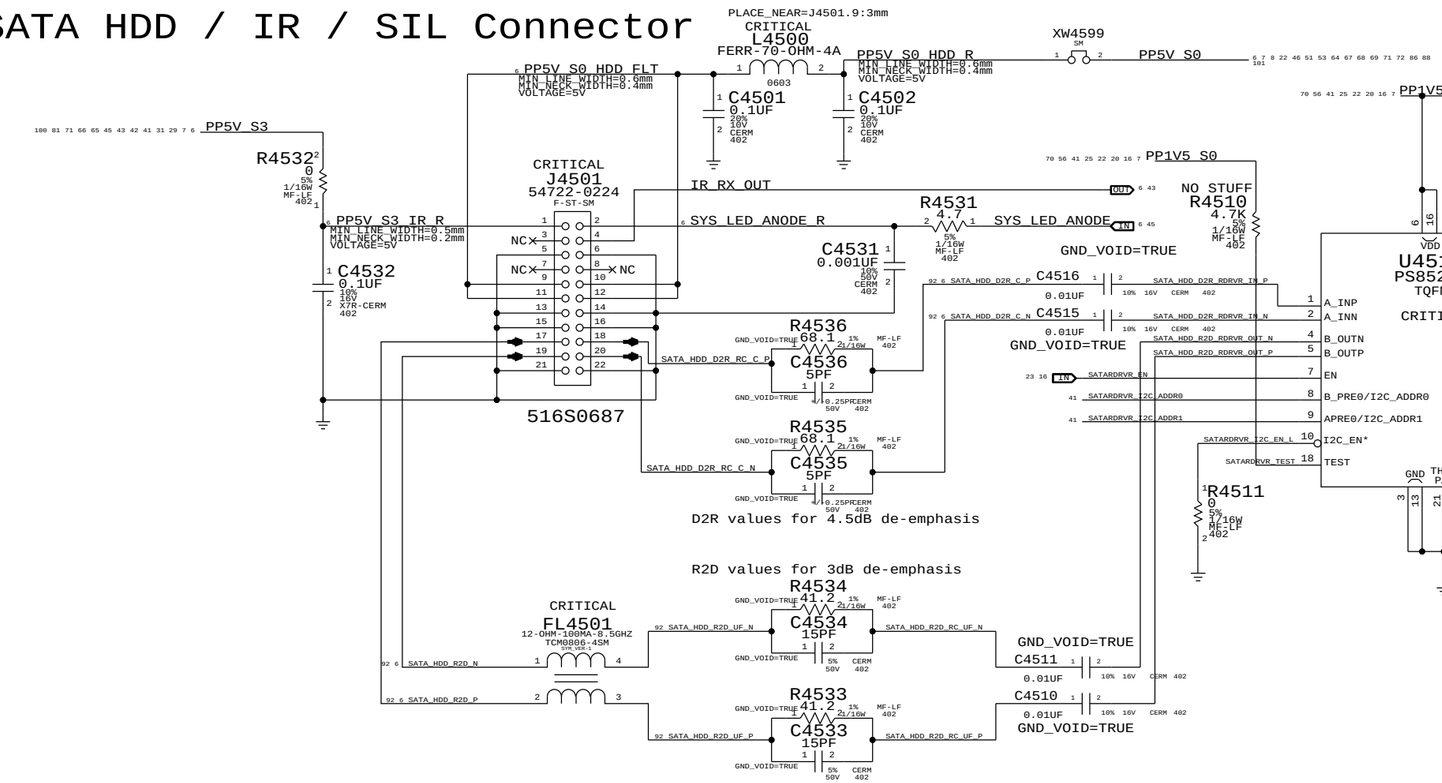




Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATA HDD / IR / SIL Connector



SYNC_MASTER=K91_ERIC	SYNC_DATE=11/08/2010
PAGE TITLE	SATA/IR/SIL Connectors
Apple Inc.	DRAWING NUMBER / SIZE D
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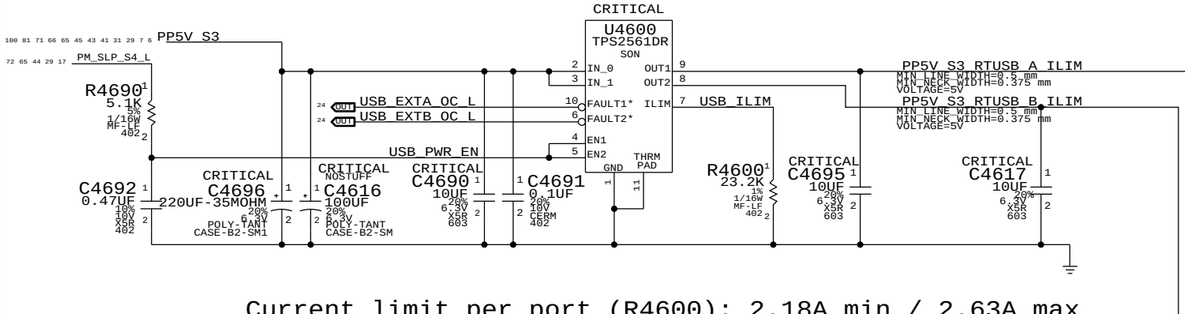
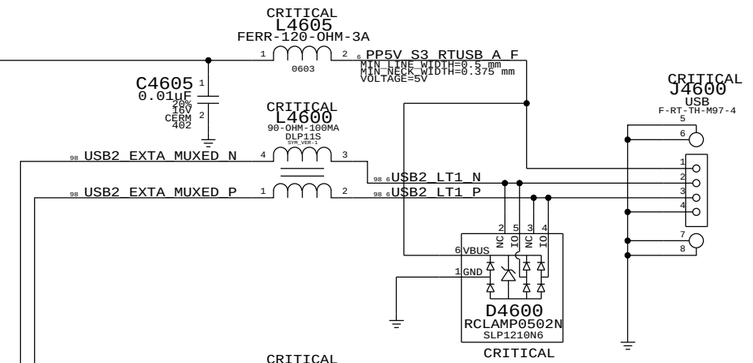
USB Port Power Switch



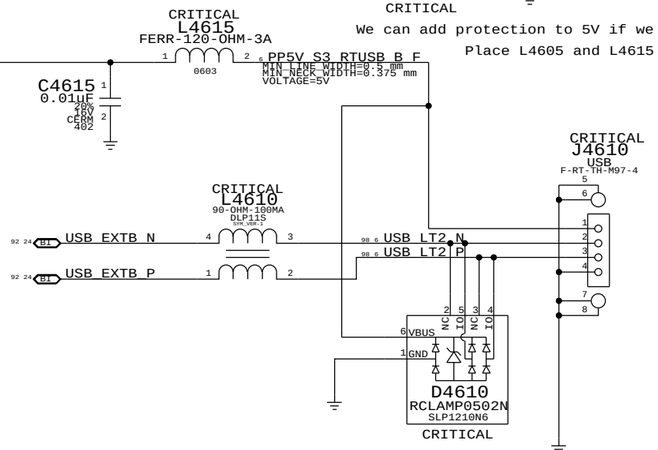
Current limit per port (R4600): 2.18A min / 2.63A max

Left USB Port A

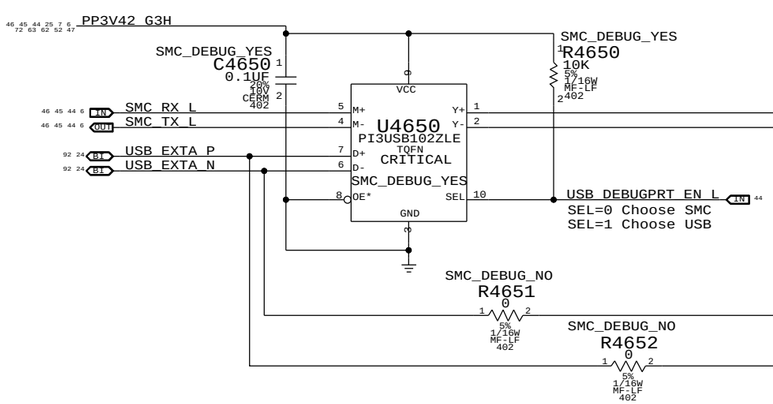


We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin



USB/SMC Debug Mux



Left USB Port B

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: External USB Connectors

Apple Inc.

DRAWING NUMBER:

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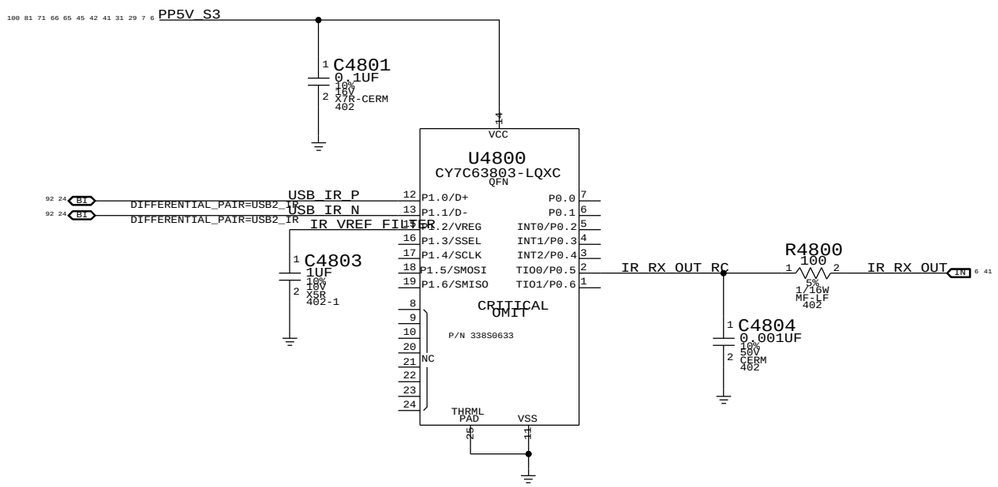
IR SUPPORT



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

Front Flex Support

Apple Inc.

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SIZE D

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BRANCH

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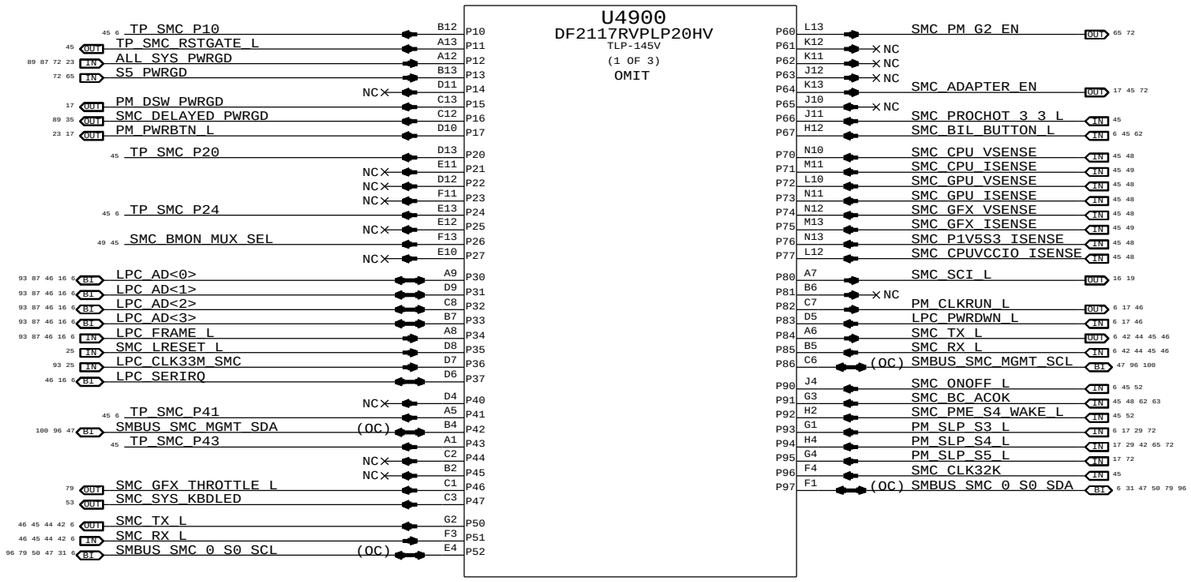
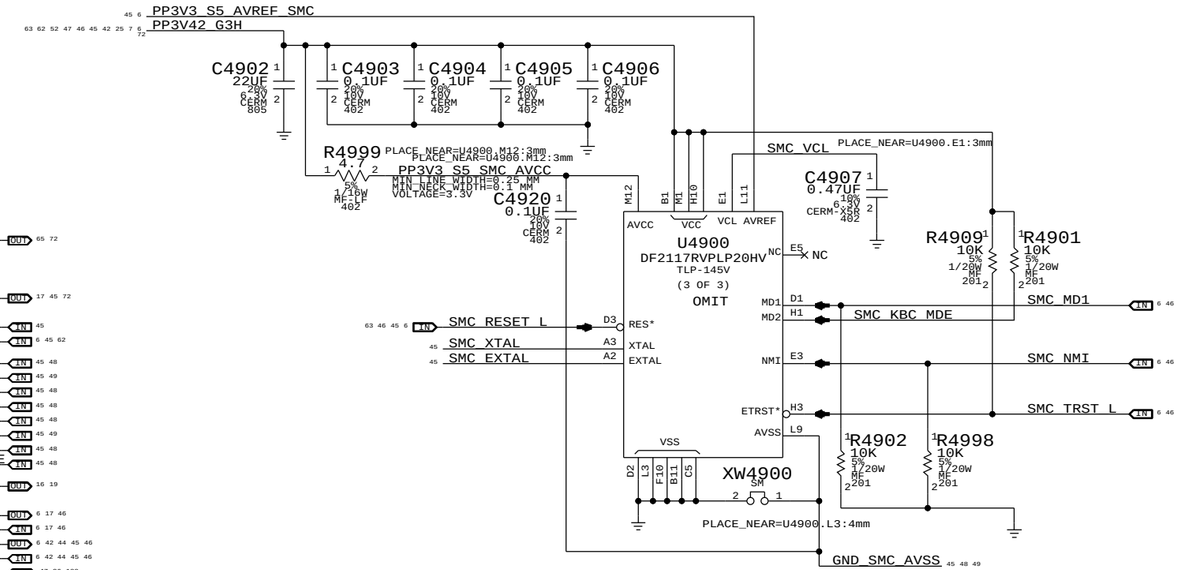
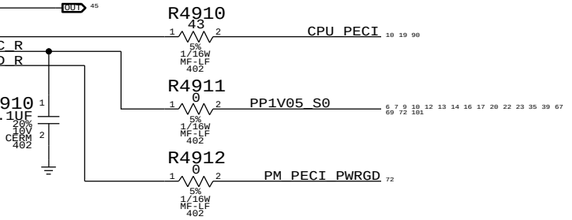
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.





SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: D

SIZE: D

REVISION:

BRANCH:

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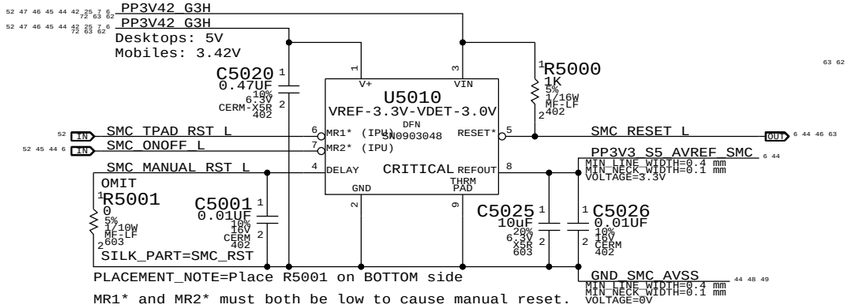
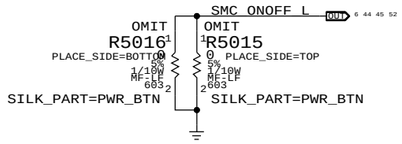
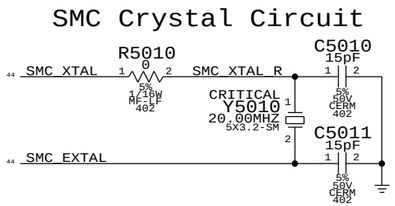
SMC Reset "Button", Supervisor & AVREF Supply



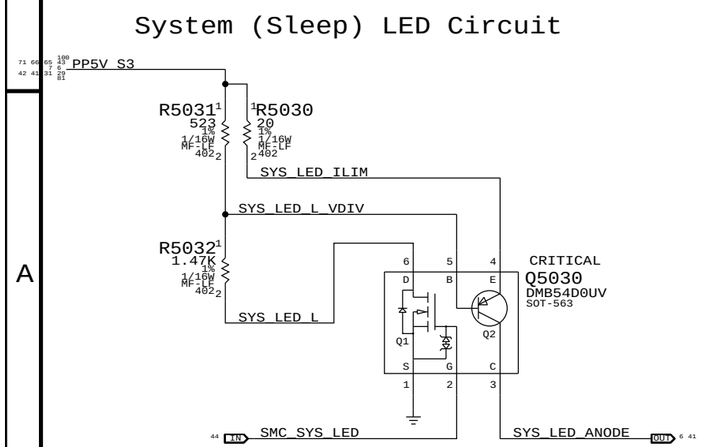
Debug Power "Buttons"



SMC Crystal Circuit

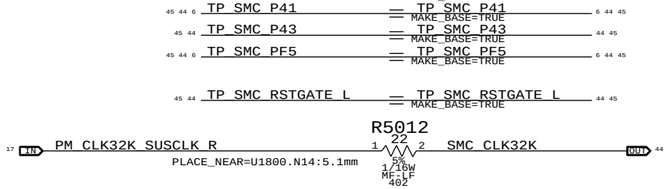


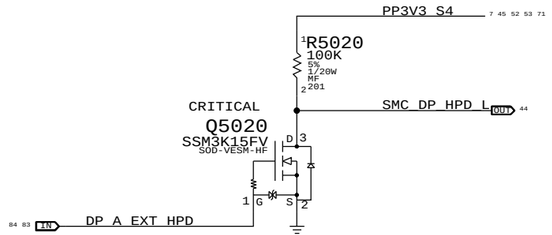
System (Sleep) LED Circuit

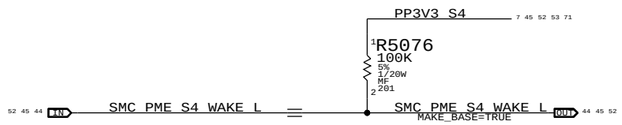


SMC_xxx_ACOK Signals

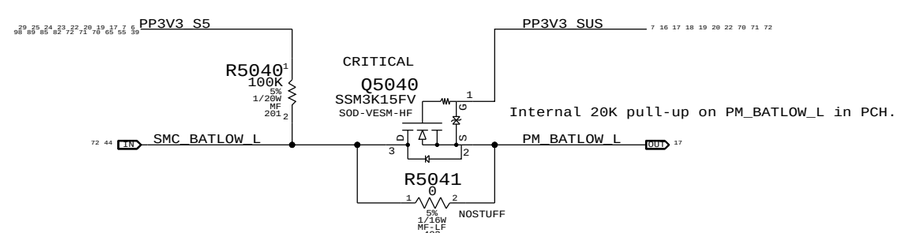
NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE
SMC_BC_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
SMS_INT_L	SMS_INT_L	MAKE_BASE=TRUE
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_GPU_VSENSE	SMC_GPU_VSENSE	MAKE_BASE=TRUE
SMC_GPU_ISENSE	SMC_GPU_ISENSE	MAKE_BASE=TRUE
SMC_GFX_VSENSE	SMC_GFX_VSENSE	MAKE_BASE=TRUE
SMC_GFX_ISENSE	SMC_GFX_ISENSE	MAKE_BASE=TRUE
SMC_P1V5S3_ISENSE	SMC_P1V5S3_ISENSE	MAKE_BASE=TRUE
SMC_CPUVCCIO_ISENSE	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_SA_ISENSE	SMC_SA_ISENSE	MAKE_BASE=TRUE
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_GPU_HI_ISENSE	SMC_GPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_OTHER_HI_ISENSE	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
TP_SMC_P10	TP_SMC_P10	MAKE_BASE=TRUE
TP_SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE
TP_SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE
SMC_BMON_MUX_SEL	SMC_BMON_MUX_SEL	MAKE_BASE=TRUE
TP_SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE
TP_SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE
TP_SMC_PF5	TP_SMC_PF5	MAKE_BASE=TRUE
TP_SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE



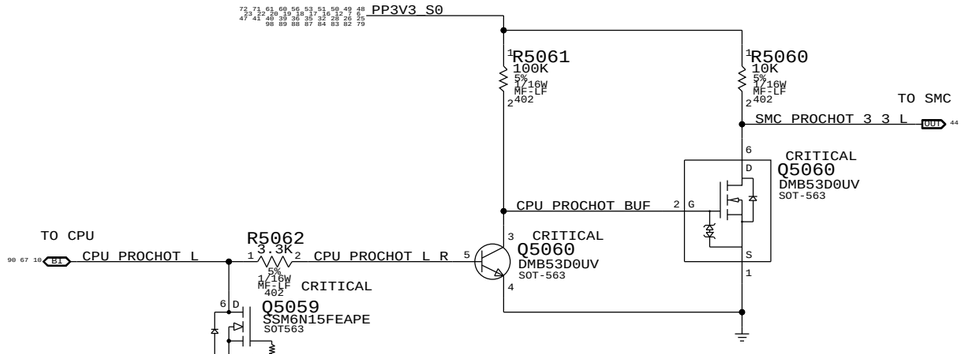




BATLOW# Isolation



SMC FSB to 3.3V Level Shifting



PP3V42_G3H Pull-ups

SMC_ONOFF_L	R5070	10K	5%	1/20W	MF	201	
G3_POWERON_L	R5072	10K	5%	1/20W	MF	201	
SMC_LID	R5071	100K	5%	1/20W	MF	201	
SMC_TX_L	R5073	10K	5%	1/20W	MF	201	
SMC_RX_L	R5074	100K	5%	1/20W	MF	201	
SMC_TMS	R5077	10K	5%	1/20W	MF	201	
SMC_TDO	R5078	10K	5%	1/20W	MF	201	
SMC_TDI	R5079	10K	5%	1/20W	MF	201	
SMC_TCK	R5080	10K	5%	1/20W	MF	201	
SMC_BIL_BUTTON_L	R5081	10K	5%	1/20W	MF	201	
SMC_BC_ACOK	R5087	470K	5%	1/20W	MF	201	
SMS_INT_L	R5093	10K	5%	1/20W	MF	201	
				NOSTUFF			
SMC_PA0_PU	R5091	100K	5%	1/20W	MF	201	
SMC_ADAPTER_EN	R5085	10K	5%	1/20W	MF	201	
SMC_CASE_OPEN	R5086	10K	5%	1/20W	MF	201	
SMC_PB4	R5088	10K	5%	1/20W	MF	201	
SMC_S4_WAKESRC_EN	R5090	100K	5%	1/20W	MF	201	
WIFI_EVENT_L	R5089	10K	5%	1/20W	MF	201	

PP3V3_WLAN

SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

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Apple Inc.

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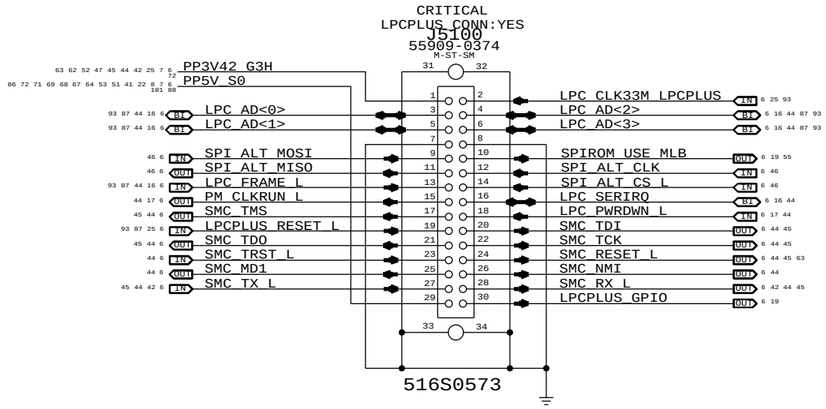
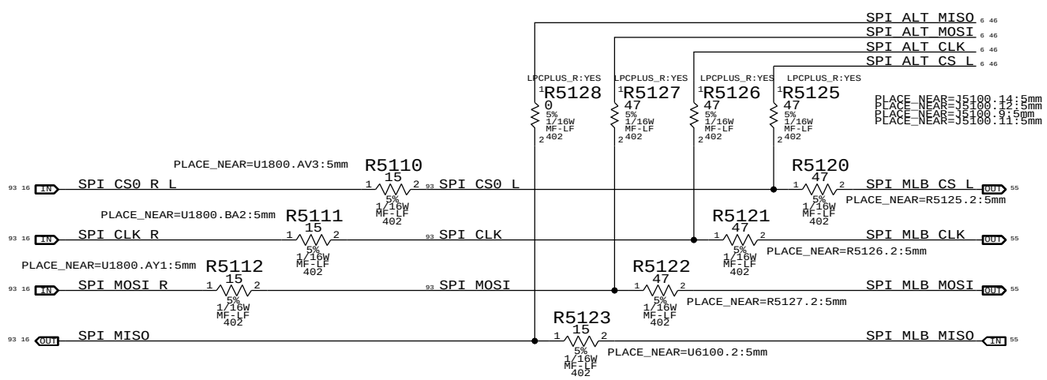
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K18_MLB	SYNC_DATE=04/27/2010
PAGE TITLE	LPC+SPI Debug Connector
Apple Inc.	DRAWING NUMBER / SIZE D
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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 5% 1/16W MF-LF 402 — R5201 1K 5% 1/16W MF-LF 402

Cougar Point
U1800
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
MAKE_BASE=TRUE

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U3301
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SATA Redriver
U4510
(Write: 0xB6 Read: 0xB7)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U9701
(WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2500 & J2550
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6880
(Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SDRVI2C:SB
R5237 0 5% 1/16W MF-LF 402

SDRVI2C:SB
R5236 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA
MAKE_BASE=TRUE

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402 — R5211 8.2K 5% 1/16W MF-LF 402

Cougar Point
U1800
(MASTER)
- SML_PCH_0_CLK
- SML_PCH_0_DATA
MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF R5220 8.2K 5% 1/16W MF-LF 402 — NO STUFF R5221 8.2K 5% 1/16W MF-LF 402

R5223 0 5% 1/16W MF-LF 402

R5222 0 5% 1/16W MF-LF 402

Cougar Point
U1800
(Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK
- SML_PCH_1_DATA
MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 5% 1/16W MF-LF 402 — R5251 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int)
Whistler: U8000
(Write: 0x82 Read: 0x83)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

X19
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5270 1K 5% 1/16W MF-LF 402 — R5271 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

Trackpad
J5800
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

J3401
ALS
(Write: 0x72 Read: 0x73)
Lid Angle Detect
(Write: 0x32 Read: 0x33)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

Digital SMS
LIS331DLH: U5920
(Write: 0x30 Read: 0x31)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 5% 1/16W MF-LF 402 — R5261 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

CPU Temp
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

T29 Temp
EMC1412-A: U5520
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

R5280 2.0K 5% 1/16W MF-LF 402 — R5281 2.0K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x92 Read: 0x93)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

R5290 4.7K 5% 1/16W MF-LF 402 — R5291 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

T29 SMBus Connections

PP3V3_S0

R5230 4.7K 5% 1/16W MF-LF 402 — R5231 4.7K 5% 1/16W MF-LF 402

T29 IC
U3600
(MASTER)
- I2C_T29_SCL
- I2C_T29_SDA
MAKE_BASE=TRUE

T29 Port A MCU
J9330
(Write: 0x26 Read: 0x27)
- I2C_T29_SCL
- I2C_T29_SDA

SDRVI2C:MCU
R5234 0 5% 1/16W MF-LF 402

SDRVI2C:MCU
R5235 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA
MAKE_BASE=TRUE

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: SMBus Connections

Apple Inc.

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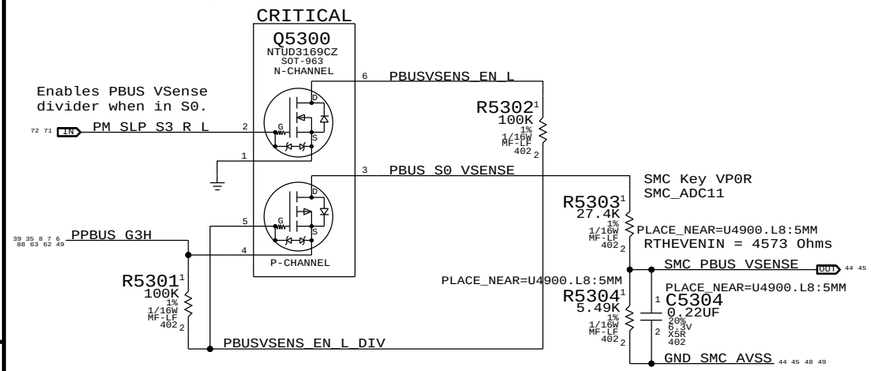
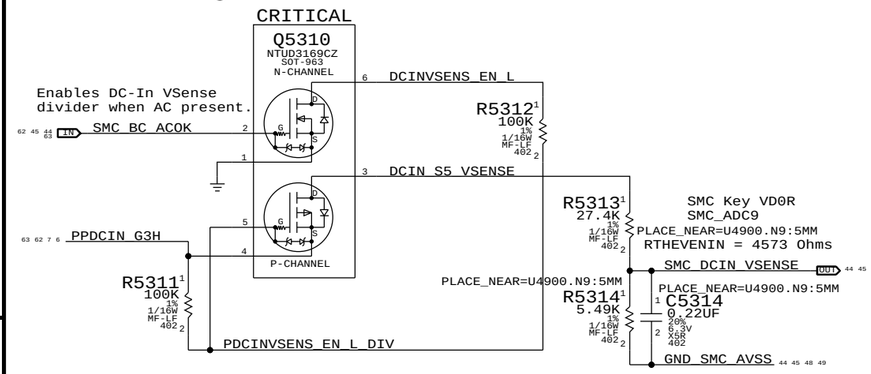
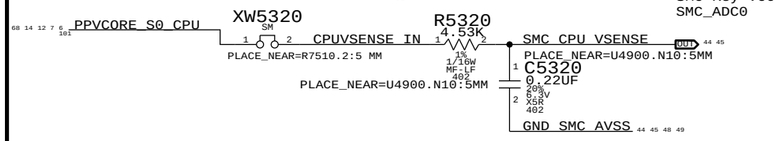
PBUS Voltage Sense Enable & Filter



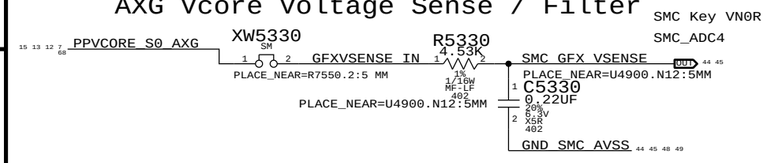
DC-In Voltage Sense Enable & Filter



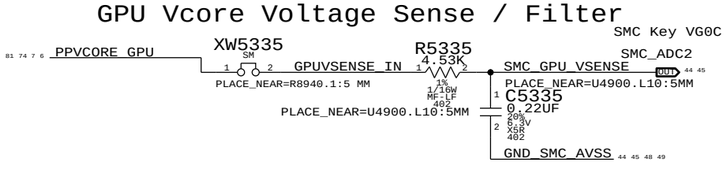
CPU Vcore Voltage Sense / Filter



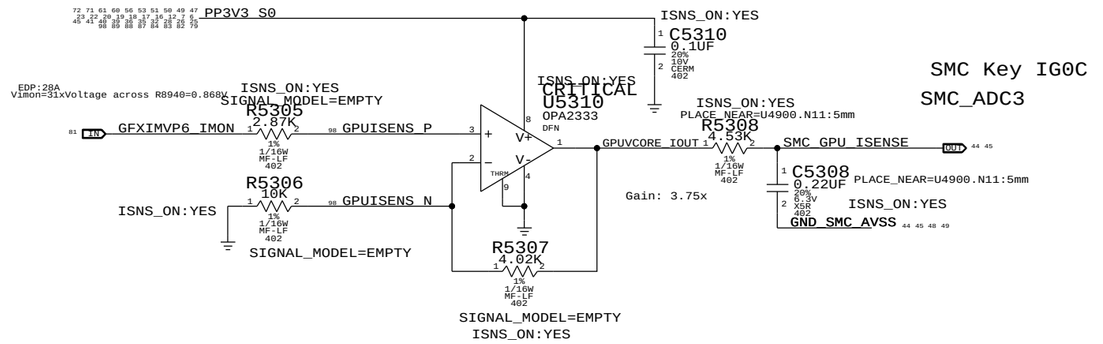
AXG Vcore Voltage Sense / Filter



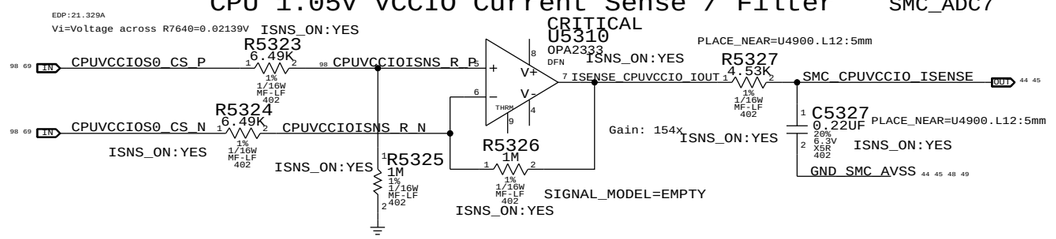
GPU Vcore Voltage Sense / Filter



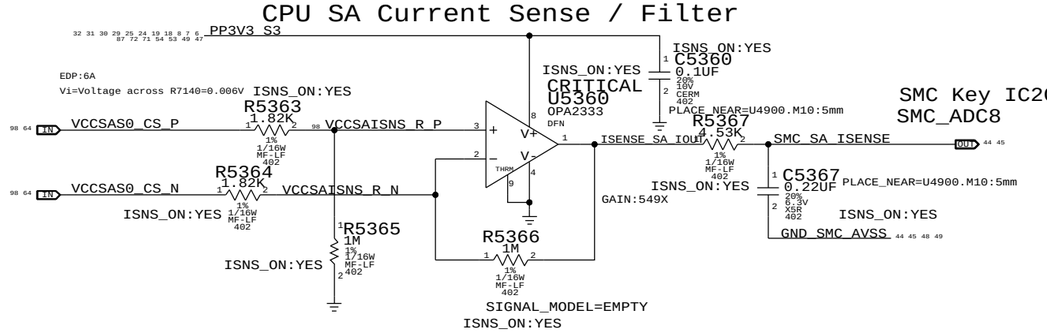
GPU VCore Load Side Current Sense / Filter



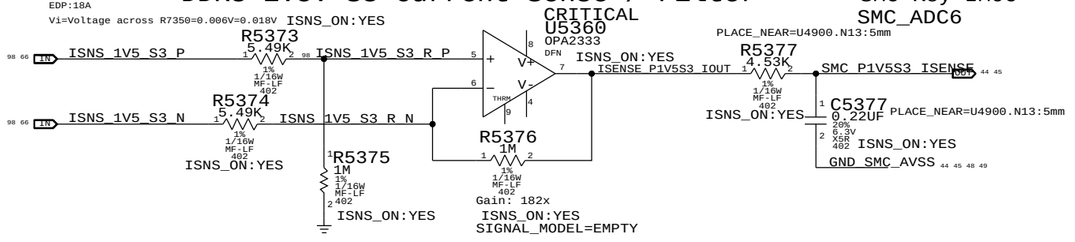
CPU 1.05V VCCIO Current Sense / Filter



CPU SA Current Sense / Filter



DDR3 1.5V S3 Current Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	4	RES, 00HM, 0402	C5308,C5327,C5367,C5377		ISNS_ON:NO

SYNC_MASTER=K91_DINESH SYNC_DATE=08/16/2010

PAGE TITLE: Voltage & Load Side Current Sensing

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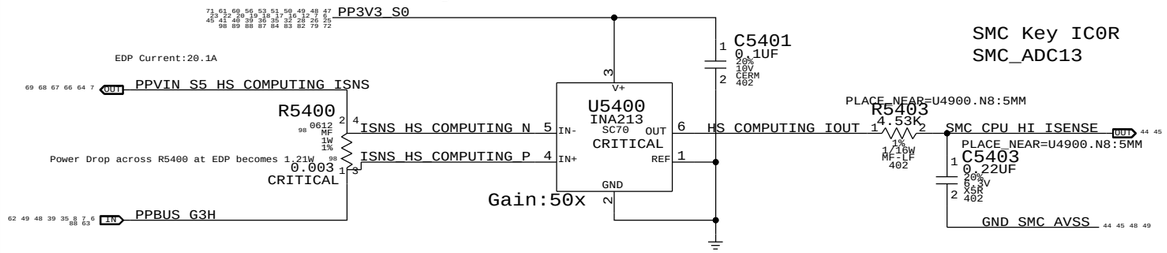
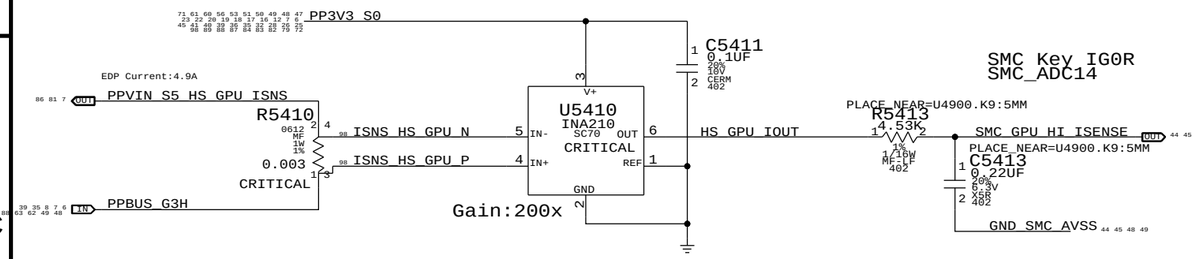
COMPUTING High Side Current Sense / Filter



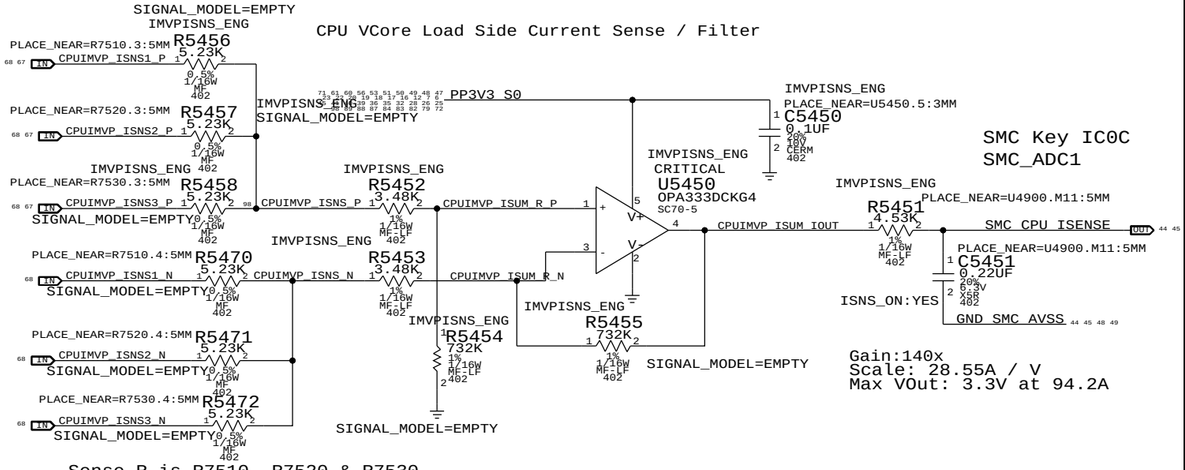
SMC Key IC0R
SMC_ADC13

GRAPHICS High Side Current Sense / Filter



SMC Key IG0R
SMC_ADC14

CPU VCore Load Side Current Sense / Filter

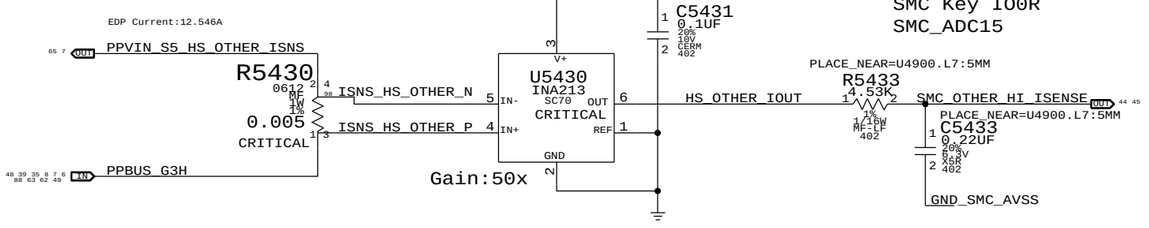


SMC Key IC0C
SMC_ADC1

Gain:140x
Scale: 28.55A / V
Max VOut: 3.3V at 94.2A

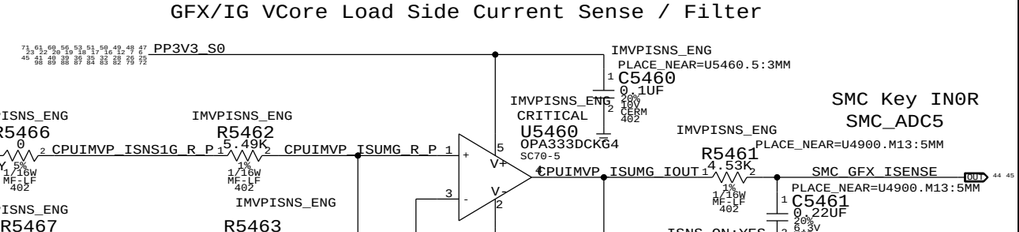
Sense R is R7510, R7520 & R7530
Individual Sense R is 0.75mOhm
EDP: 94A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

OTHER High Side Current Sense / Filter



SMC Key IO0R
SMC_ADC15

GFX/IG VCore Load Side Current Sense / Filter

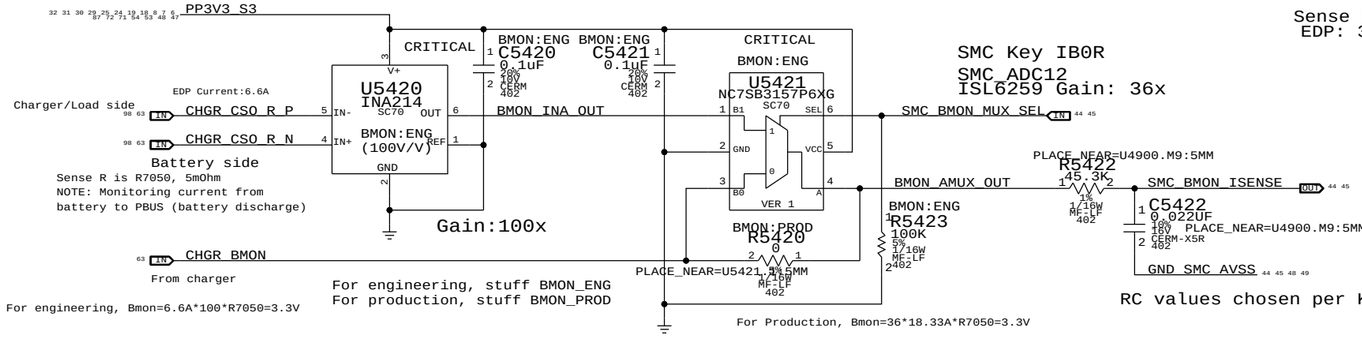


SMC Key IN0R
SMC_ADC5

Gain:133.33x
Scale: 10A / V
Max VOut: 3.3V at 33A

Sense R is R7550, 0.75mOhm
EDP: 33A TDP: 21.5A

CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter

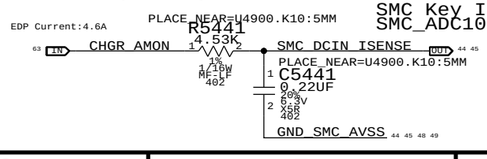


SMC Key IB0R
SMC_ADC12
ISL6259 Gain: 36x

RC values chosen per K17 Radar 7337775

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	2	RES, 0OHM, 0402	C5451,C5461		ISNS_ON:NO

DC-IN (AMON) Current Sense Filter



SMC Key ID0R
SMC_ADC10

SYNC_MASTER=K91_DINESH	SYNC_DATE=10/29/2016
PAGE TITLE: High Side and CPU/AXG Current Sensing	
Apple Inc.	DRAWING NUMBER: D; SIZE: D
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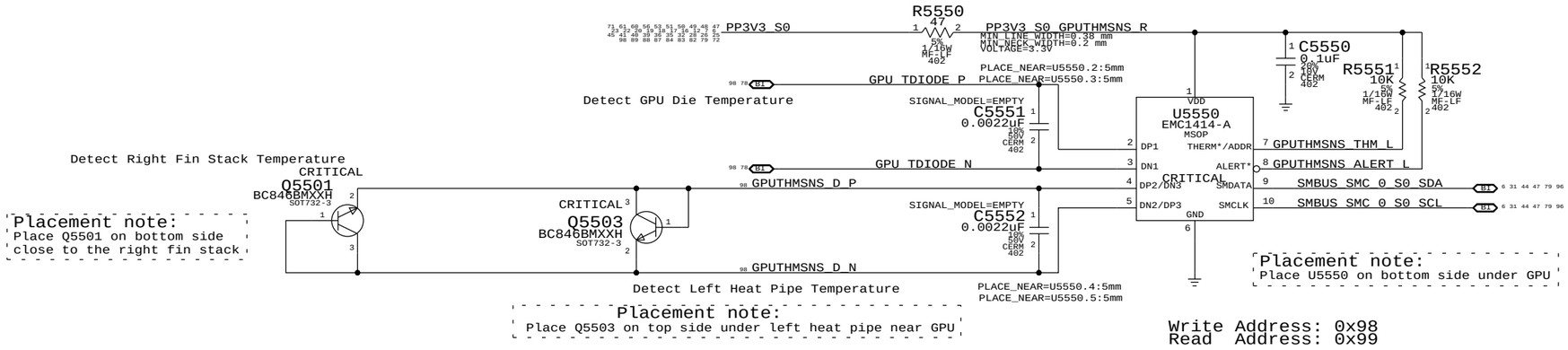
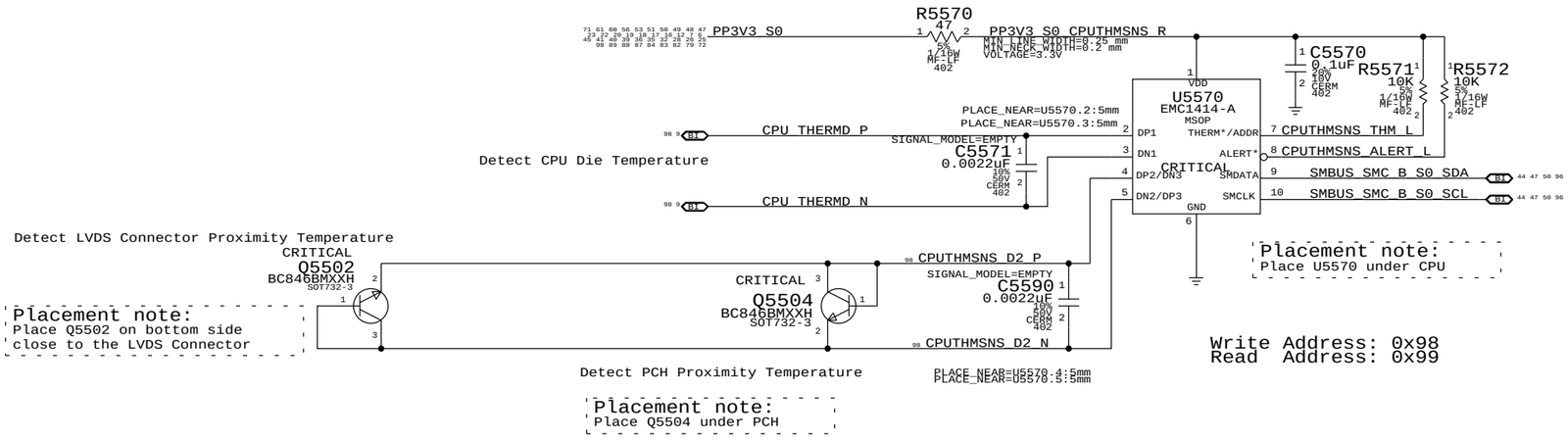
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack

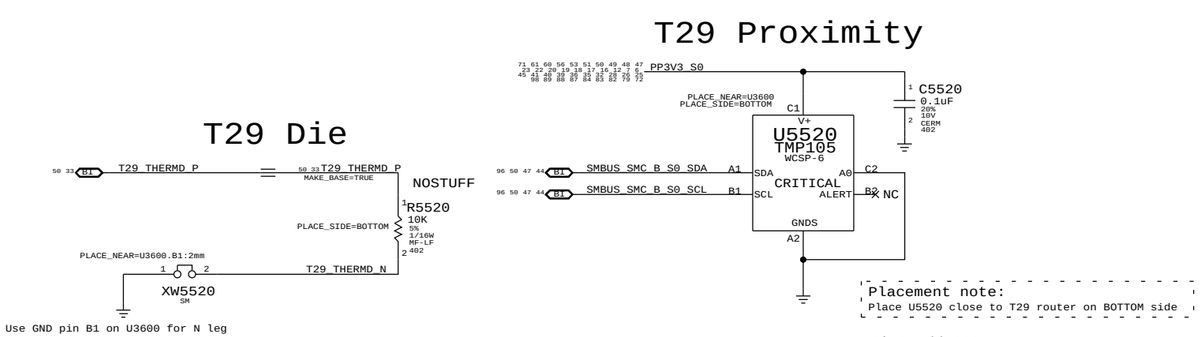


CPU Proximity/CPU Die/PCH Proximity/LVDS Connector Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

T29 Proximity



SYNC_MASTER=K91_DINESH	SYNC_DATE=09/22/2010
PAGE TITLE	Thermal Sensors
Apple Inc.	DRAWING NUMBER / SIZE: D
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	BRANCH
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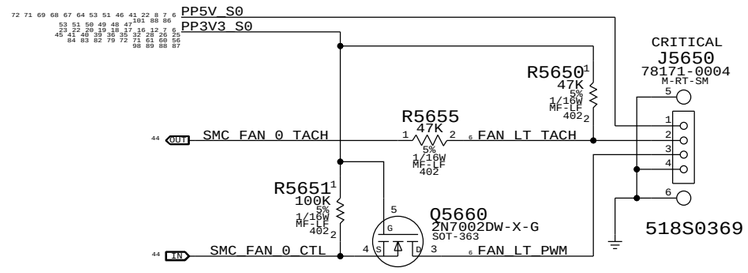
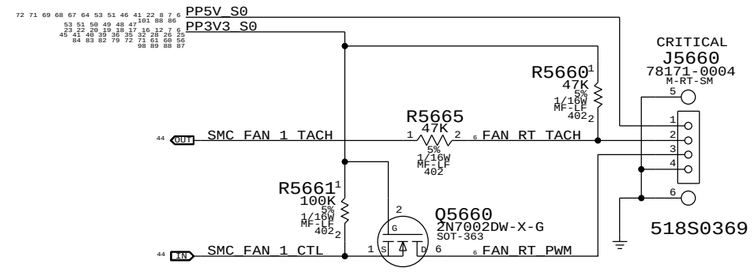
Left Fan



Right Fan



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: Fan Connectors

Apple Inc.

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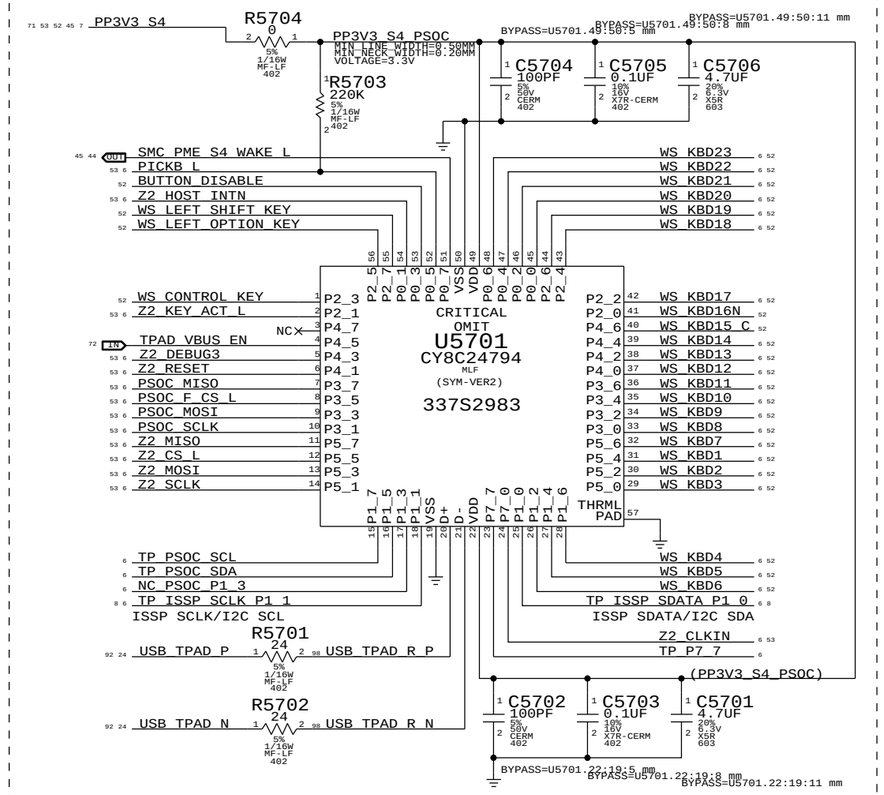
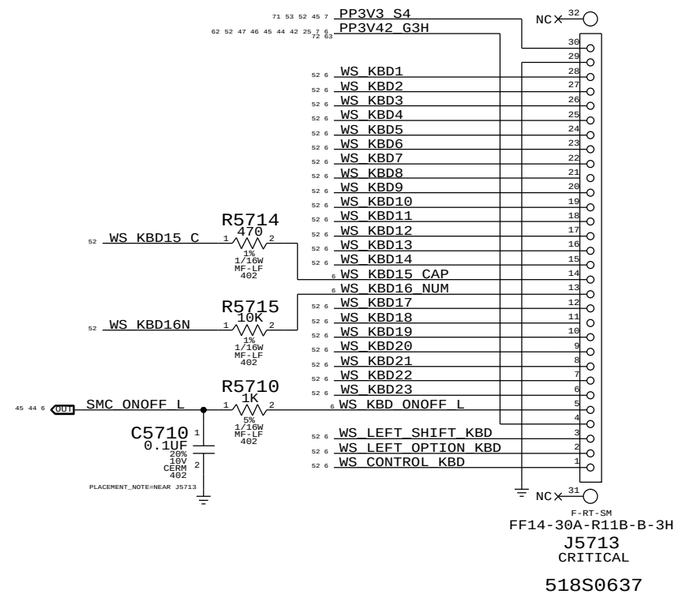
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



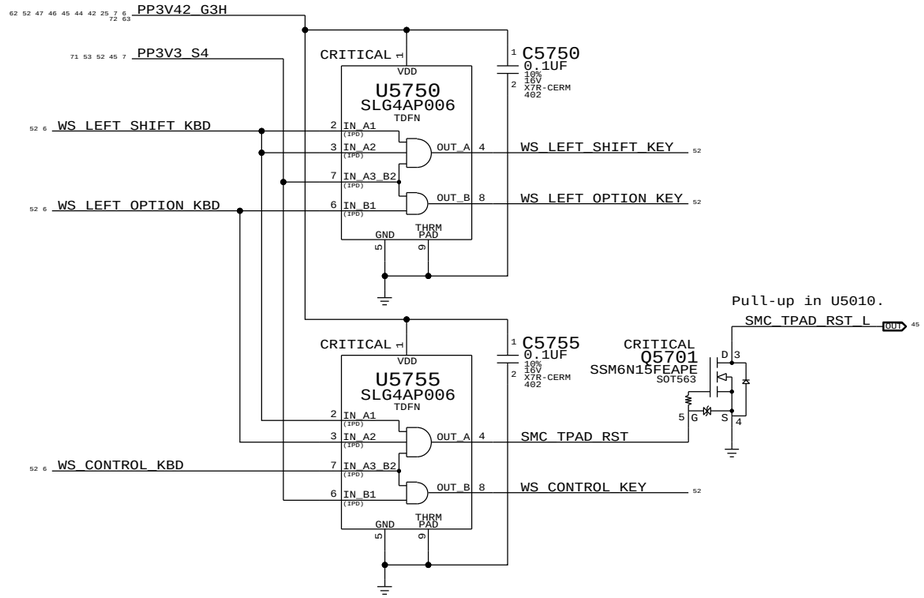
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

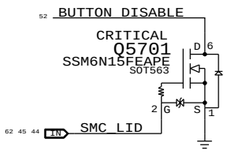


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

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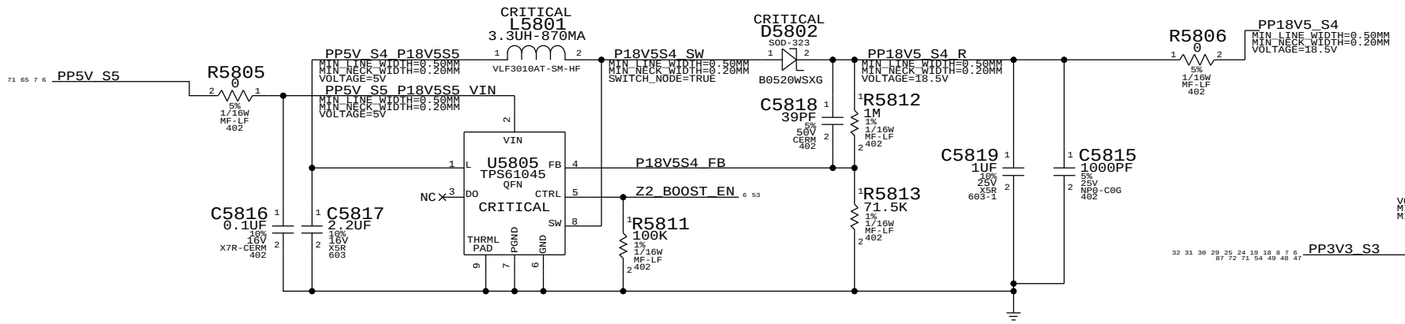
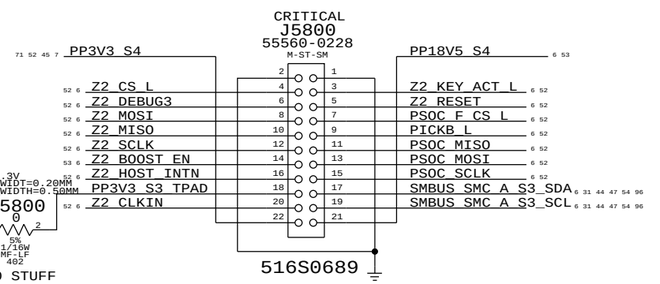
BOOSTER +18.5VDC FOR SENSORS

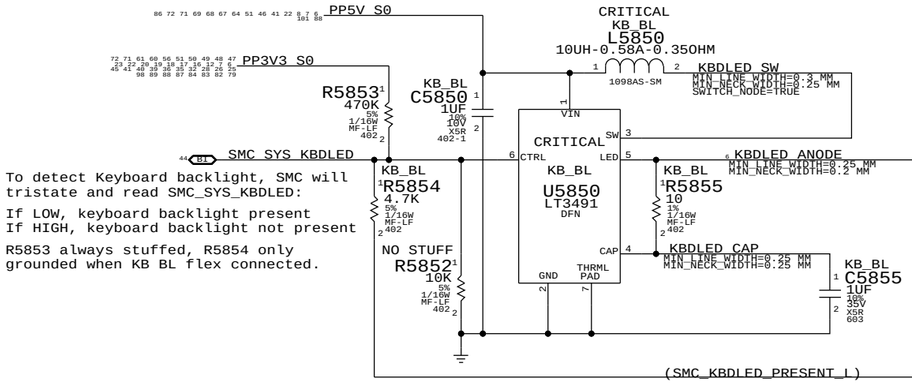
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

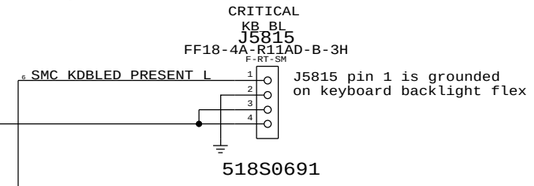


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



SYNC_MASTER=K91_ERIC SYNC_DATE=07/14/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER | SIZE: D

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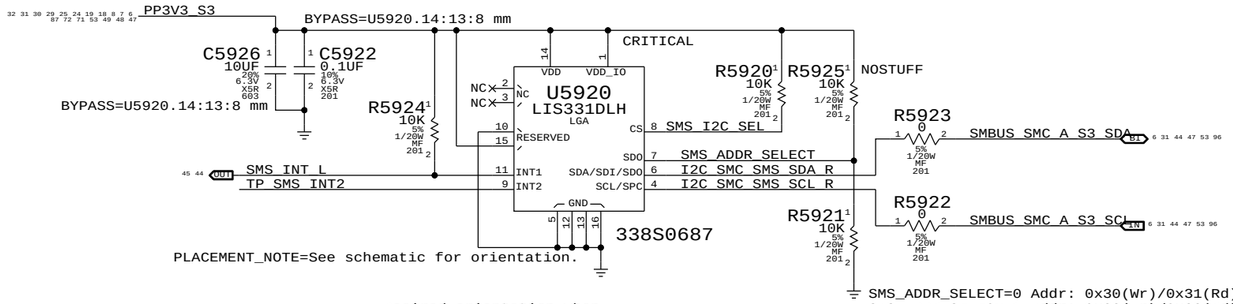

SYNC_MASTER=K91_DINESH SYNC_DATE=08/06/2010

PAGE TITLE
Digital Accelerometer

Apple Inc.

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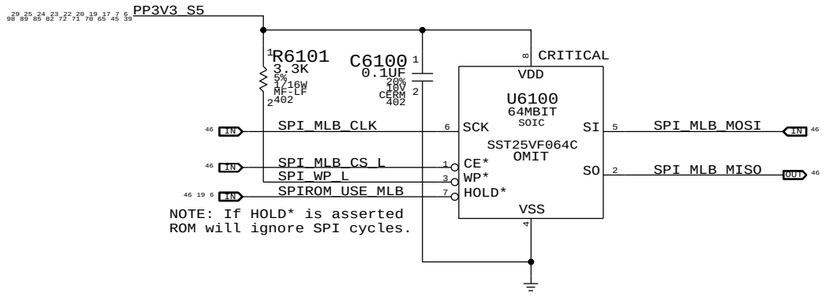

SYNC_MASTER=K91_BEN SYNC_DATE=06/08/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER

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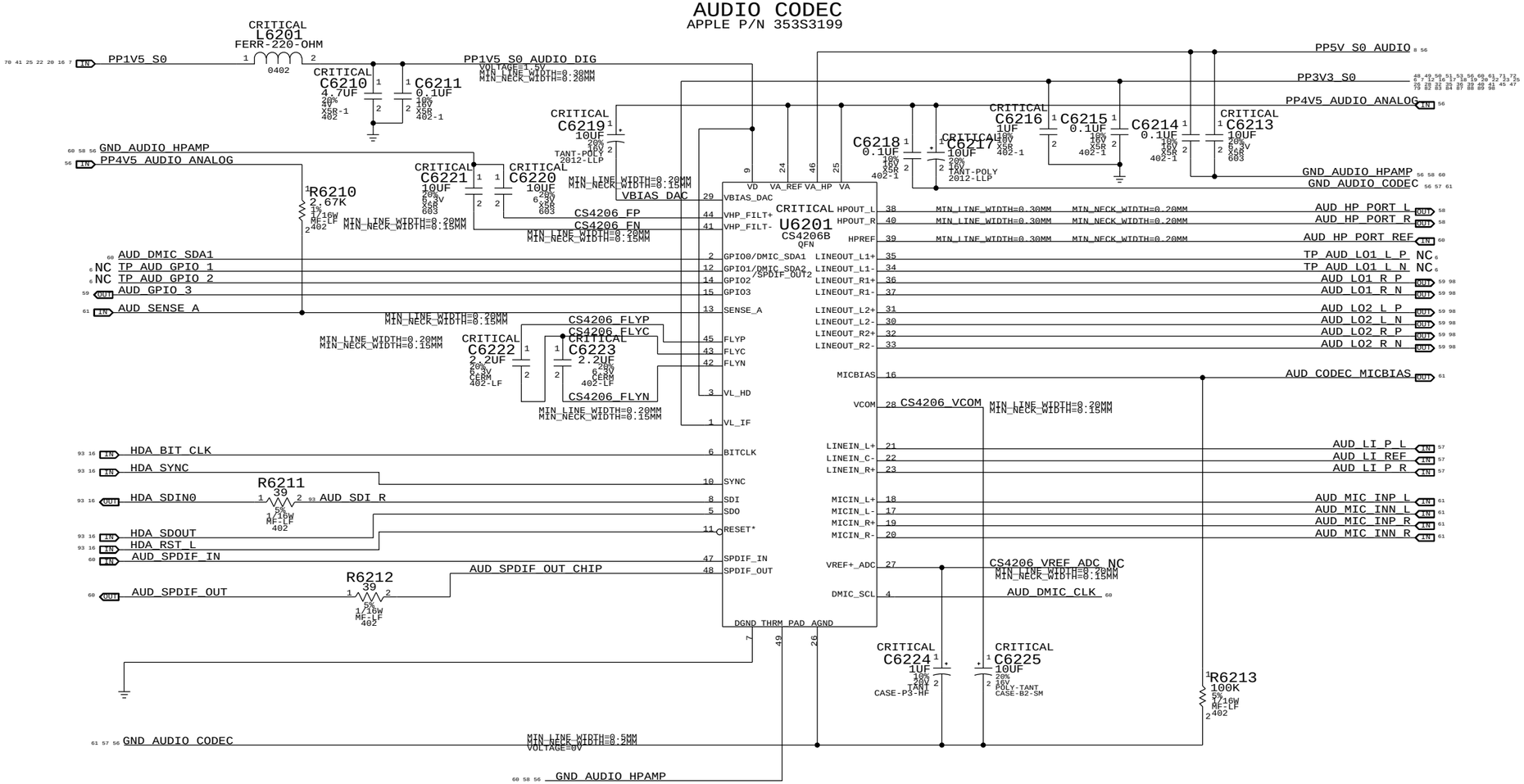
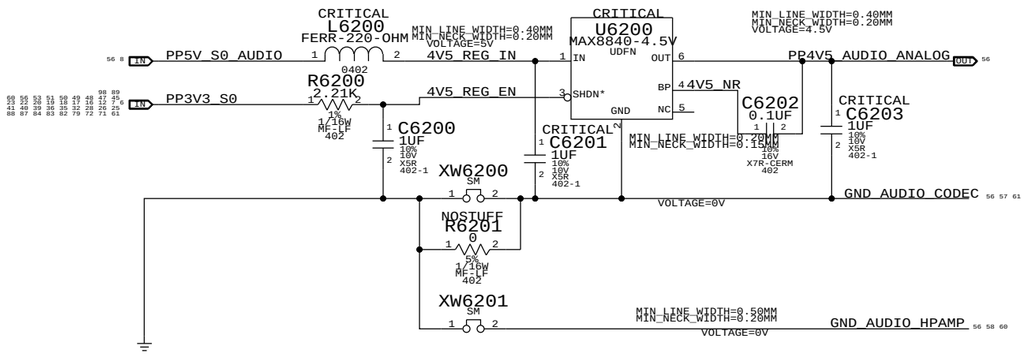
AUDIO CODEC
APPLE P/N 353S3199



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K91_AUDIO SYNC_DATE=09/30/2010

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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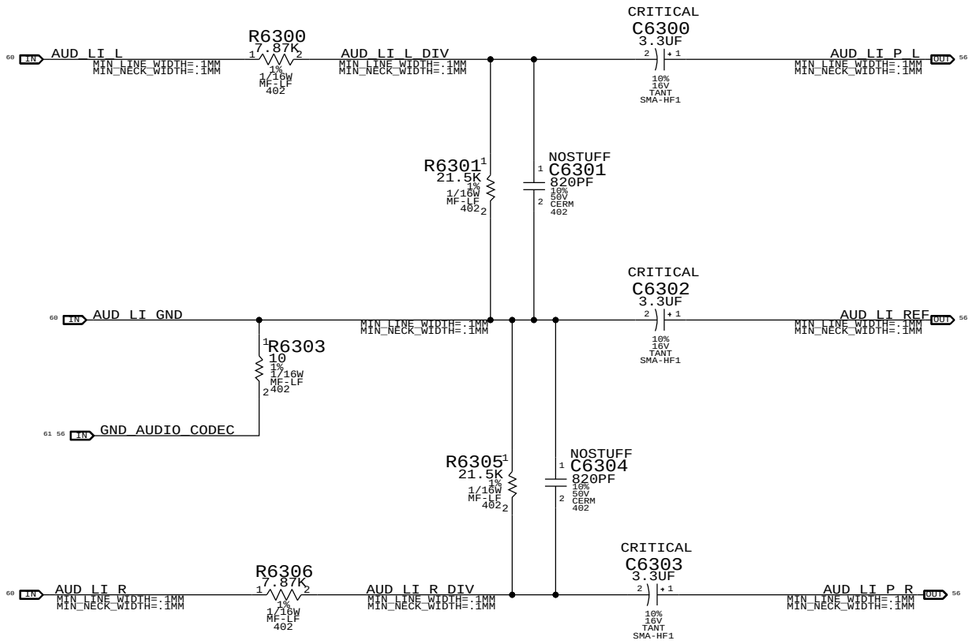
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

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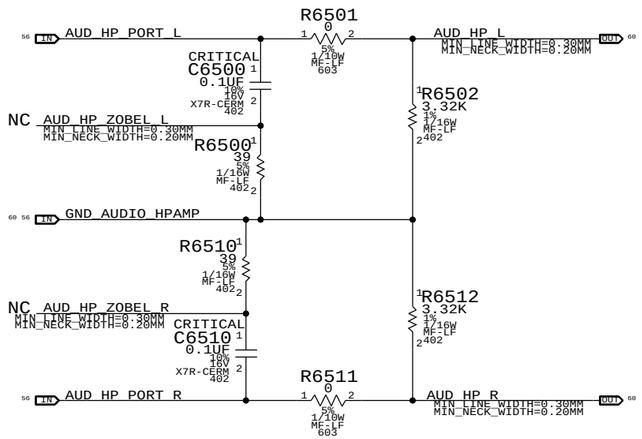
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

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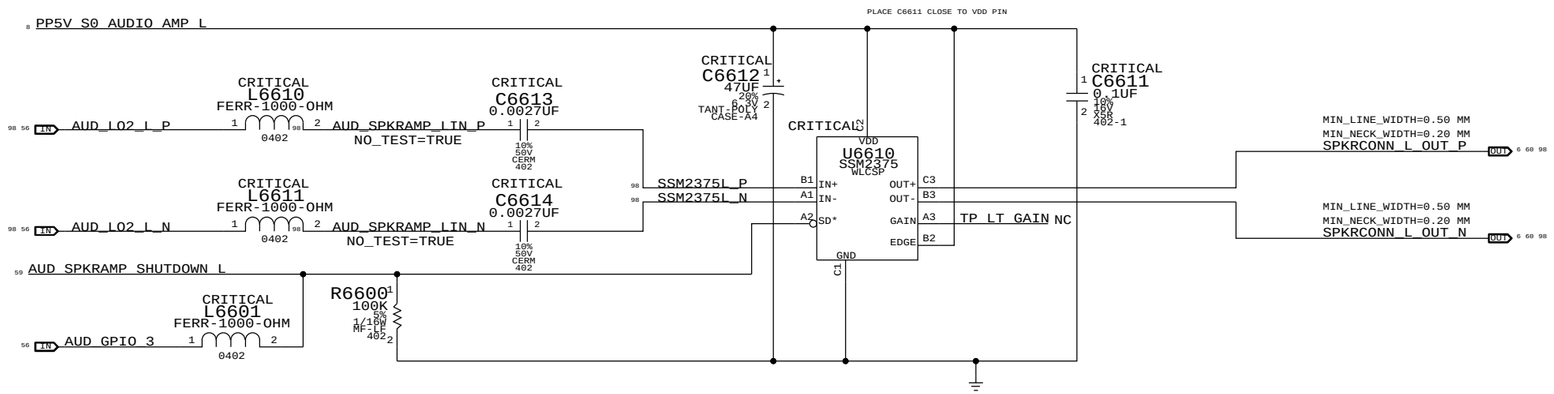
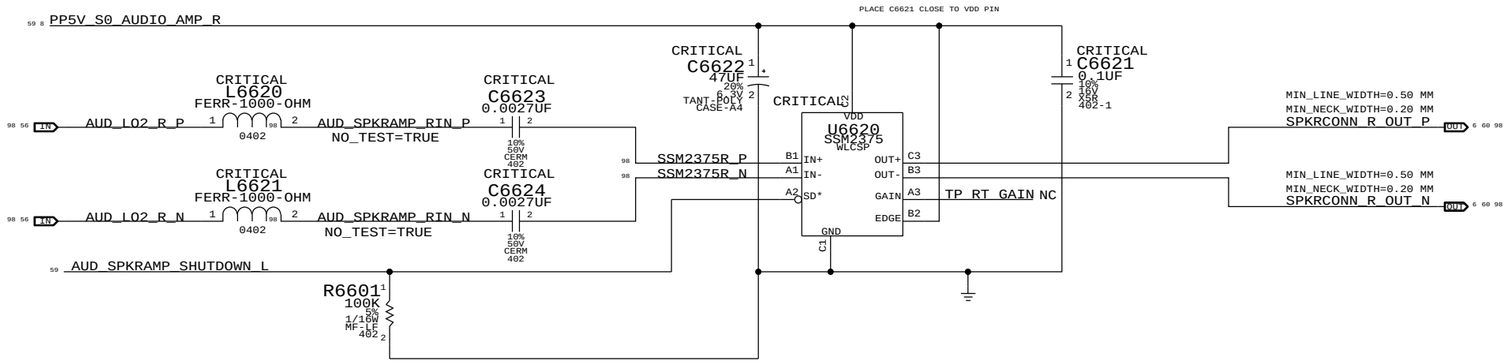
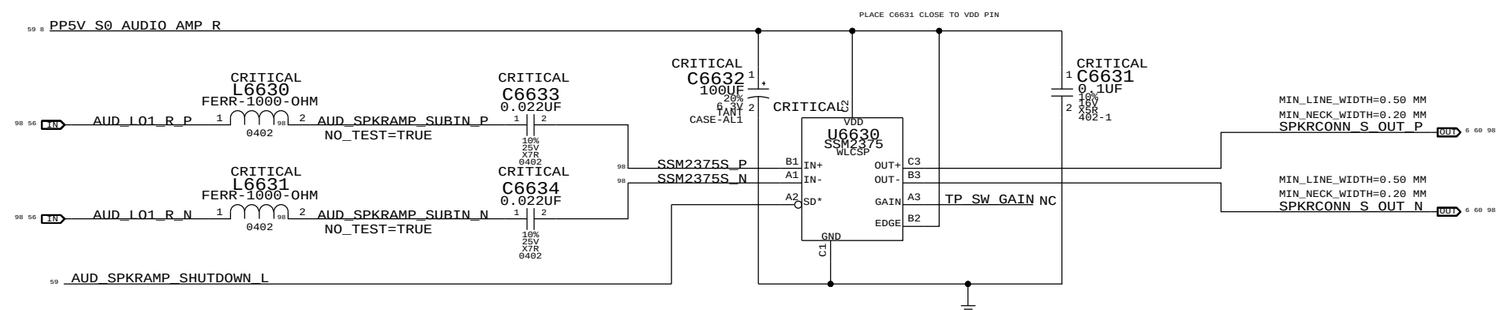
3X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958

GAIN = +3 DB
1ST ORDER FC (L&R) = ~737 HZ
1ST ORDER FC (SUB) = ~90 HZ







SYNC_MASTER=K91_AUDIO	SYNC_DATE=07/12/2010
PAGE TITLE	AUDIO: SPEAKER AMP
Apple Inc.	DRAWING NUMBER: D
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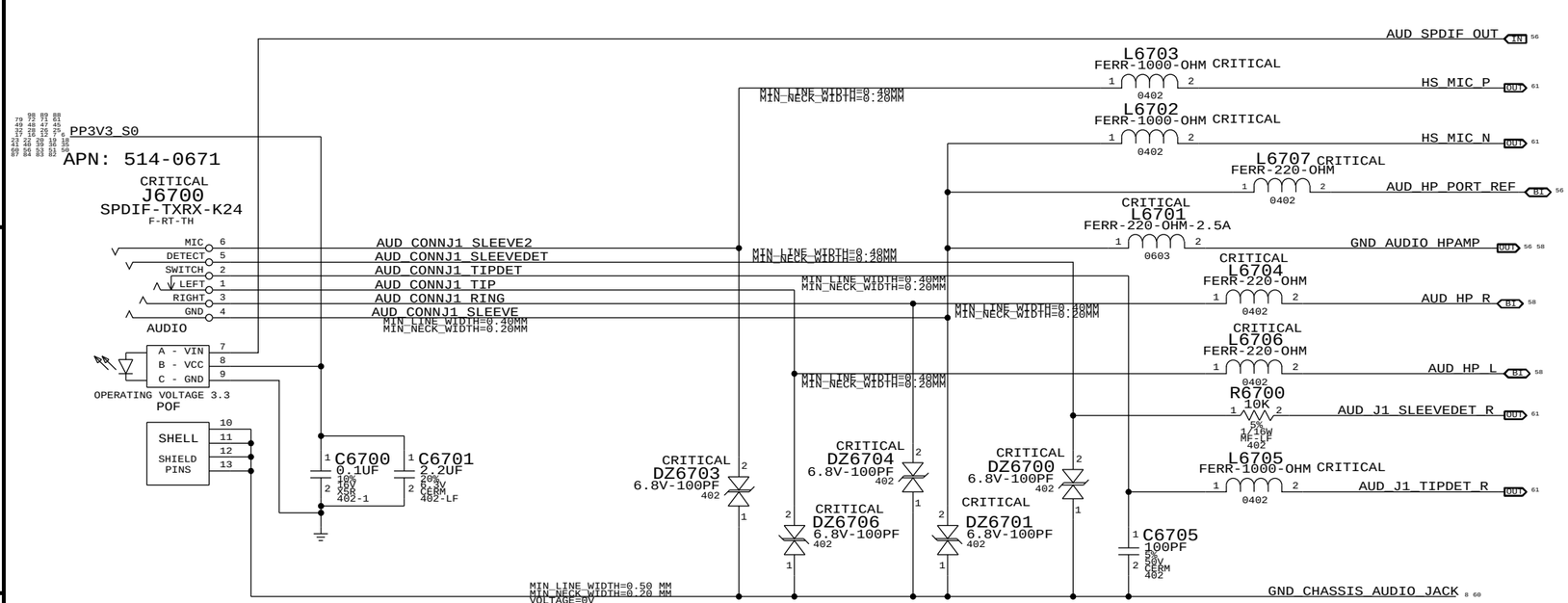
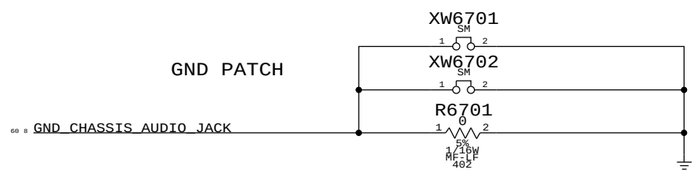
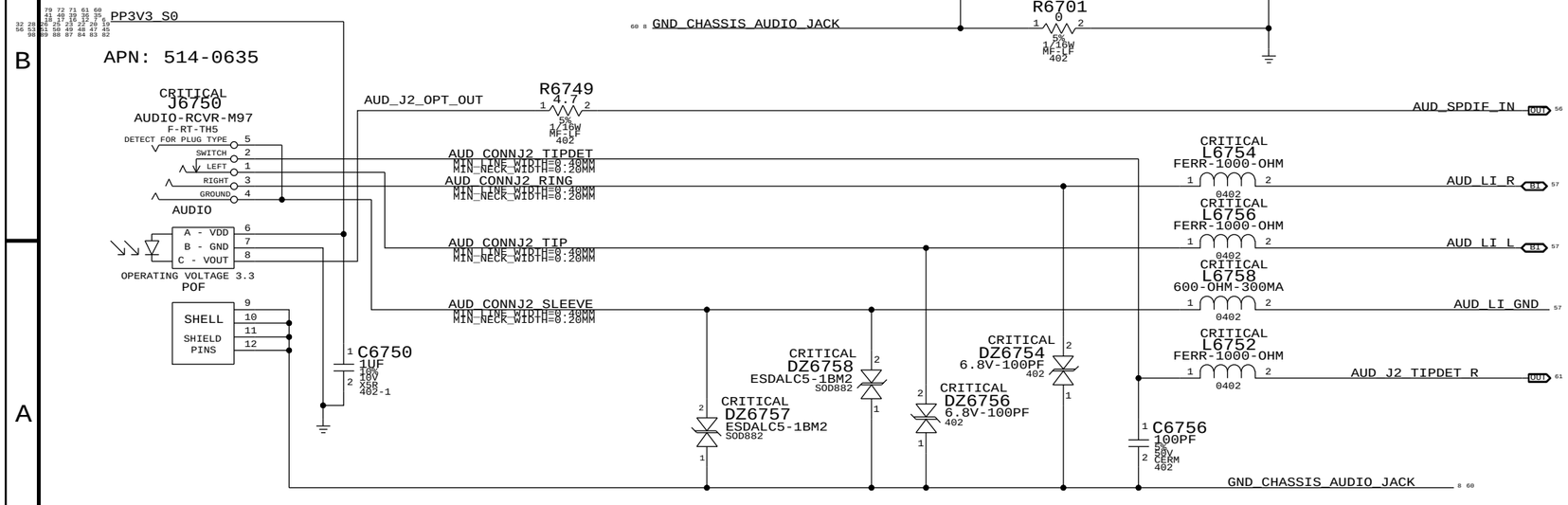
AUDIO JACK 1 LO/HP JACK, SPDIF TX



GND PATCH

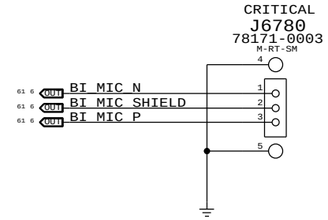


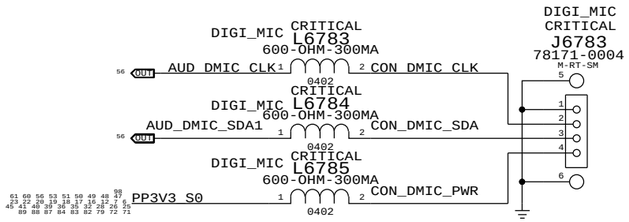
AUDIO JACK 2 LINE IN JACK, SPDIF RX



MIC CONNECTOR
Dual DMIC removed.Added single analog mic like K18.
Sept 21st 2010

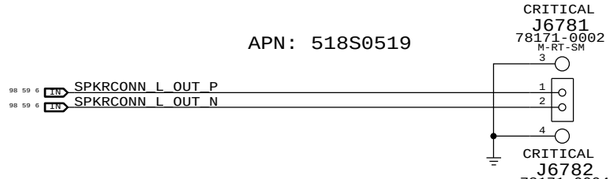
Place this in place of DMIC connector J6780



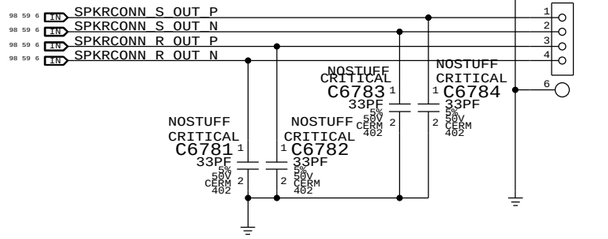


SPEAKER CONNECTOR

APN: 518S0519



APN: 518S0521



SYNC_MASTER=K91_AUDIO SYNC_DATE=09/30/2010

PAGE TITLE: AUDIO: JACKS

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ

PP3V3_S0 — CRITICAL L6880 FERR-1000-OHM 0402 — PP3V3_S0_HS_RX
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM VOLTAGE=3.3V
CSP MIKEY APN:353S2640
R6886 10K 5% 1/16W MF-LF 402
CRITICAL C6880 10UF 20% 6.3V X5R 603
CRITICAL C6887 0.1UF 10% 25V X5R 402
CRITICAL U6880 CD3282A1 WCSP
PULLUPS ON MCP PAGE
R6882 0 5% 1/16W MF-LF 402 — SMBUS_PCH_CLK
R6883 0 5% 1/16W MF-LF 402 — SMBUS_PCH_DATA
R6884 0 5% 1/16W MF-LF 402 — AUD_I2C_INT_L
R6885 0 5% 1/16W MF-LF 402 — AUD_IPHS_SWITCH_EN
HS_SCL HS_SDA HS_INT_L HS_ENABLE TIPDET_UNFILT
SCL SDA INT* ENABLE HDET CS MICBIAS DETECT BYPASS DGND AGND
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM
HS_MIC_BIAS HS_SW_DET HS_RX_BP
CRITICAL C6882 2.2UF 20% 6.3V X5R 402 — GND_AUDIO_CODEC
C6881 0.01UF 10% 16V CERM 402
R6887 100K 5% 1/16W MF-LF 402 — GND_AUDIO_CODEC
R6880 1K 1% 1/16W MF-LF 402
R6881 2.2K 5% 1/16W MF-LF 402

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)

AUD_SENSE_A
PP3V3_S0_AUDIO_F
R6801 220K 5% 1/16W MF-LF 402
APN:376S0613
AUD_OUTJACK_INSERT_L
R6806 39.2K 1% 1/16W MF-LF 402 — AUD_PORTA_DET_L NC
R6805 20.0K 1% 1/16W MF-LF 402 — AUD_PORTB_DET_L NC
Q6800 SSM6N15FEAPE SOT563
Q6801 SSM6N15FEAPE SOT563
Q6801 SSM6N15FEAPE SOT563
R6802 47K 5% 1/16W MF-LF 402 — AUD_J1_TIPDET_R — AUD_J1_DET_RC
C6801 0.1UF 20% 10V CERM 402
GND_AUDIO_CODEC
R6803 220K 5% 1/16W MF-LF 402 — PP3V3_S0_AUDIO_F — AUD_J1_SLEEVEDET_INV
R6804 220K 5% 1/16W MF-LF 402
Q6800 SSM6N15FEAPE SOT563
AUD_J1_SLEEVEDET_R
C6802 0.01UF 10% 16V CERM 402
GND_AUDIO_CODEC
AUD_J1_SLEEVEDET_R

PORT B RIGHT(BUILT-IN MIC)

AUD_CODEC_MICBIAS — R6850 100 1% 1/16W MF-LF 402 — MIC_BIAS_FILT — R6851 2.4K 1% 1/16W MF 402-1
CRITICAL C6852 2.2UF 20% 6.3V TANT 402
GND_AUDIO_CODEC
CRITICAL C6850 0.1UF 10% 25V X5R 402 — AUD_MIC_INP_R — BI_MIC_HI_F — L6850 FERR-1000-OHM 0402 — BI_MIC_P
R6852 100K 5% 1/16W MF-LF 402
CRITICAL C6853 0.001UF 10% 50V X5R 402 CERM
CRITICAL C6851 0.1UF 10% 25V X5R 402 — AUD_MIC_INN_R — BI_MIC_LO_F — L6851 FERR-1000-OHM 0402 — BI_MIC_N
GND_AUDIO_CODEC
R6853 2.4K 1% 1/16W MF 402-1
XW6851 SM BI_MIC_SHIELD
HP=80HZ
Place this next to the connector

EXTRACTION NOTIFICATION

PP3V3_S0 — CRITICAL L6862 FERR-1000-OHM 0402 — PP3V3_S0_AUDIO_F
MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM VOLTAGE=3.3V
C6861 0.1UF 10% 25V X5R 402 CERM
GND_AUDIO_CODEC
R6865 100K 5% 1/16W MF-LF 402 — AUD_PERPH_DET_R
R6867 0 5% 1/16W MF-LF 402 — AUD_IP_PERIPHERAL_DET
R6864 220K 5% 1/16W MF-LF 402 — AUD_J1_TIPDET_INV
R6866 0 5% 1/16W MF-LF 402 — TIPDET_UNFILT
Q6803 SSM6N15FEAPE SOT563
Q6803 SSM6N15FEAPE SOT563
R6860 15K 5% 1/16W MF-LF 402 — AUD_J1_TIPDET_R — TIPDET_FILT
C6860 0.1UF 20% 10V CERM 402
GND_AUDIO_CODEC

PORT C DETECT (LINE-IN)

AUD_SENSE_A
PP3V3_S0_AUDIO_F
R6813 10K 1% 1/16W MF-LF 402
R6811 270K 5% 1/16W MF-LF 402
AUD_INJACK_INSERT_L NC
Q6802 SSM3K15FV SOD-VESM-HF
APN:376S0612
R6812 47K 5% 1/16W MF-LF 402 — AUD_J2_TIPDET_R — AUD_J2_DET_RC
C6811 0.1UF 20% 10V CERM 402
GND_AUDIO_CODEC

AUD_MIC_INP_L — CRITICAL C6883 0.1UF 10% 25V X5R 402 — HS_MIC_HI_RC — R6890 2.2K 5% 1/16W MF-LF 402 — HS_MIC_P
CRITICAL C6886 0.1UF 10% 25V X5R 402 — AUD_MIC_INN_L
R6888 100K 5% 1/16W MF-LF 402
C6884 0.0082UF 10% 25V X7R 402 CRITICAL
XW6880 SM
C6885 27PF 5% 50V C0G 402 CERM CRITICAL
GND_AUDIO_CODEC — HS_MIC_N

SYNC_MASTER=K91_AUDIO	SYNC_DATE=09/21/2010
PAGE TITLE	AUDIO: JACK TRANSLATORS
Apple Inc.	DRAWING NUMBER: — SIZE: D
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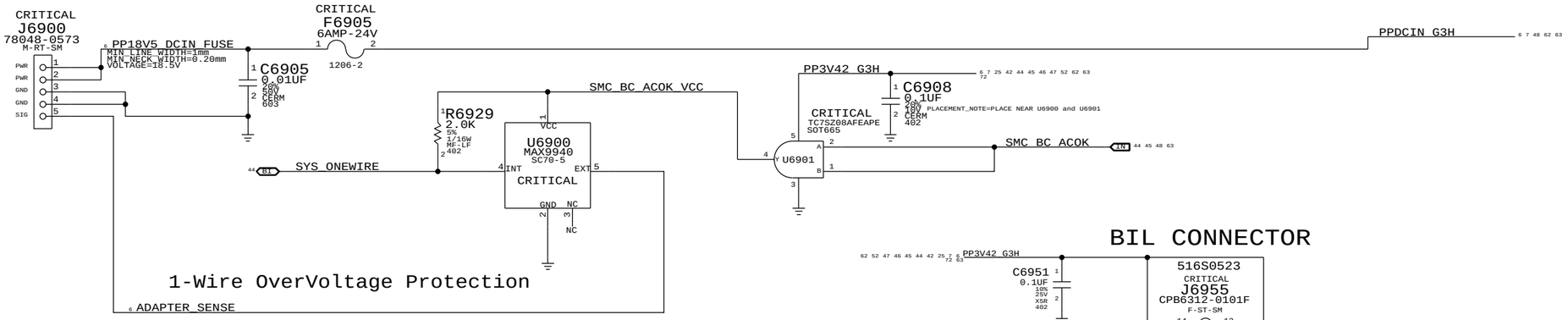
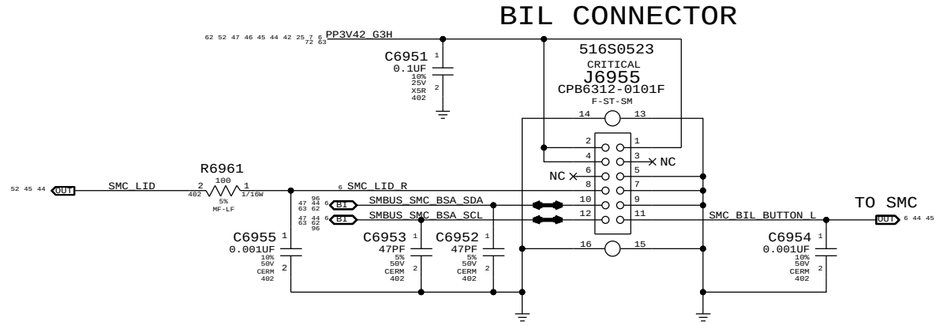
MagSafe DC Power Jack



1-Wire OverVoltage Protection

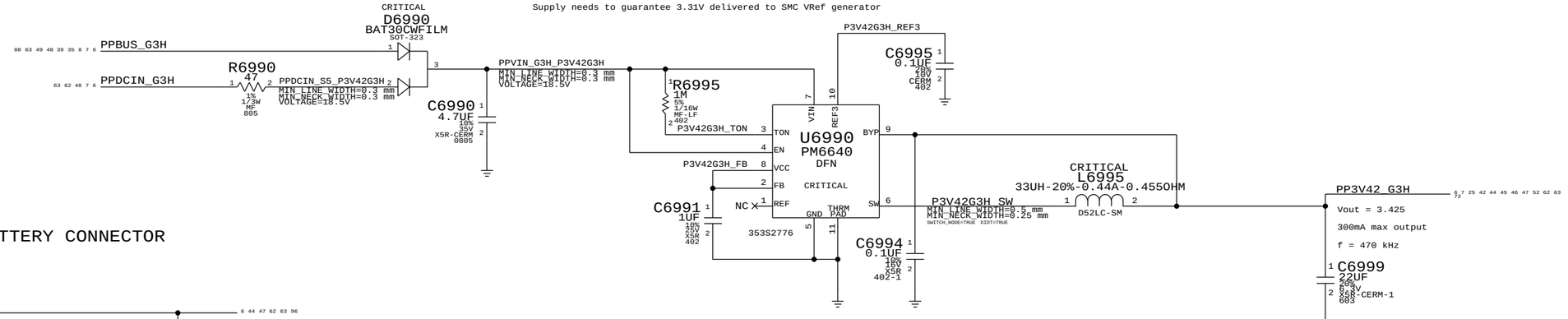
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

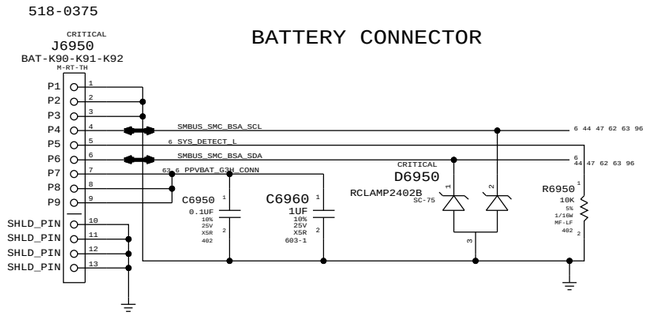


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: SIZE D
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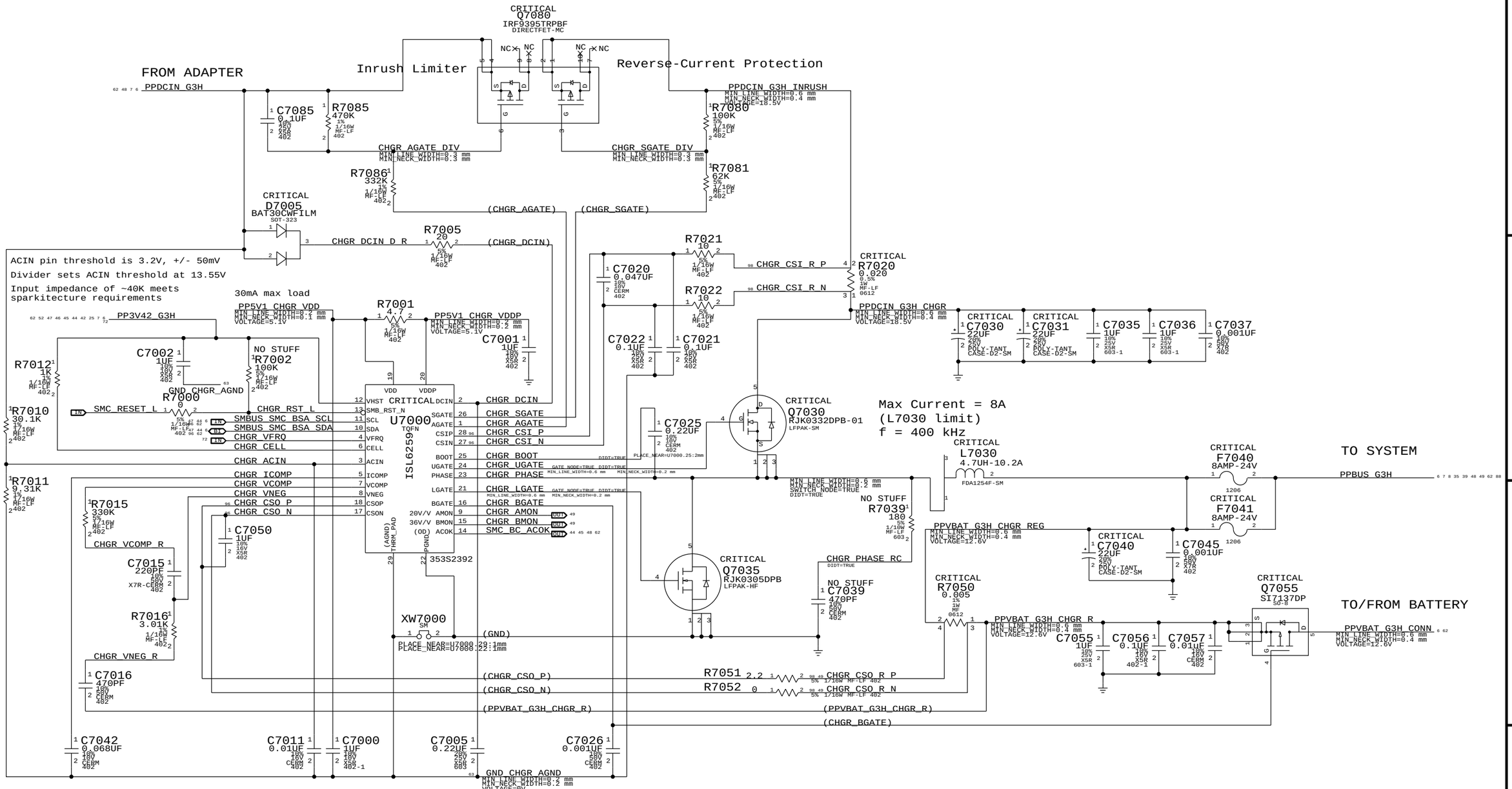

SYNC_MASTER=K91_CHANG SYNC_DATE=07/20/2016

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

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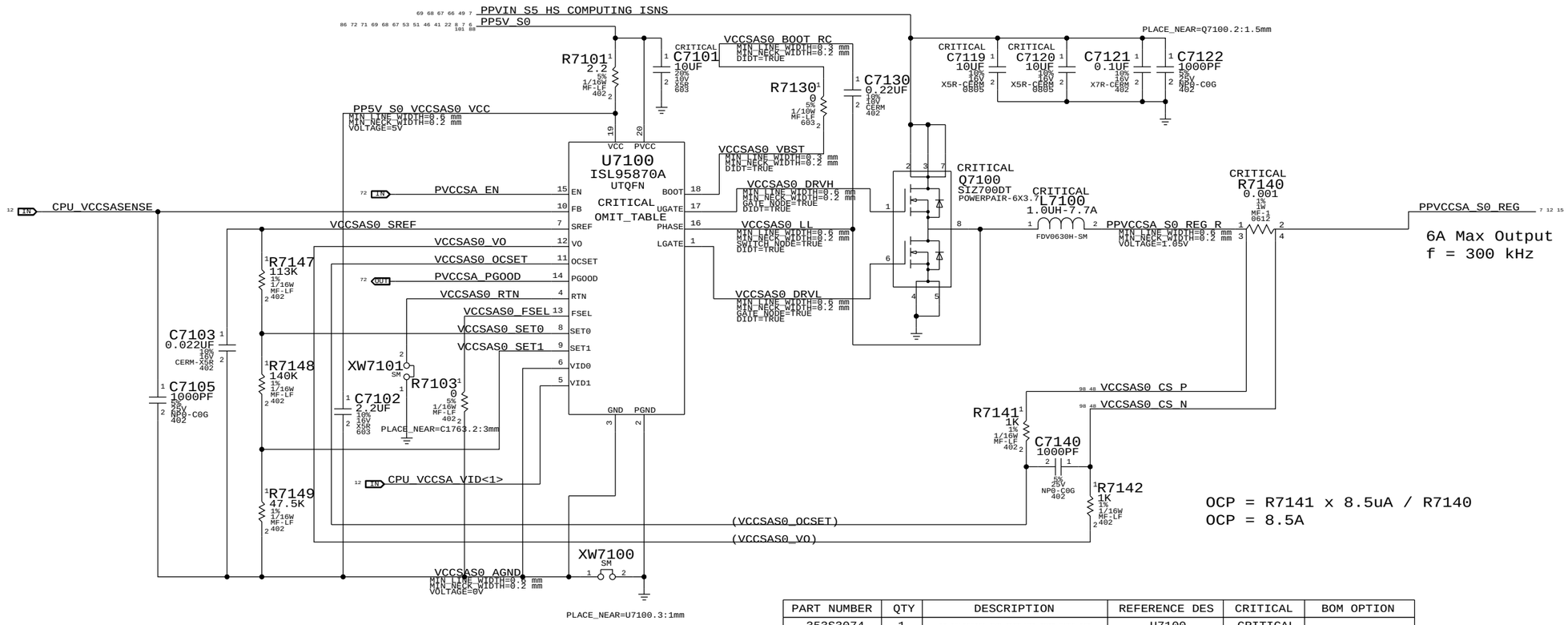

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: System Agent Supply

Apple Inc.

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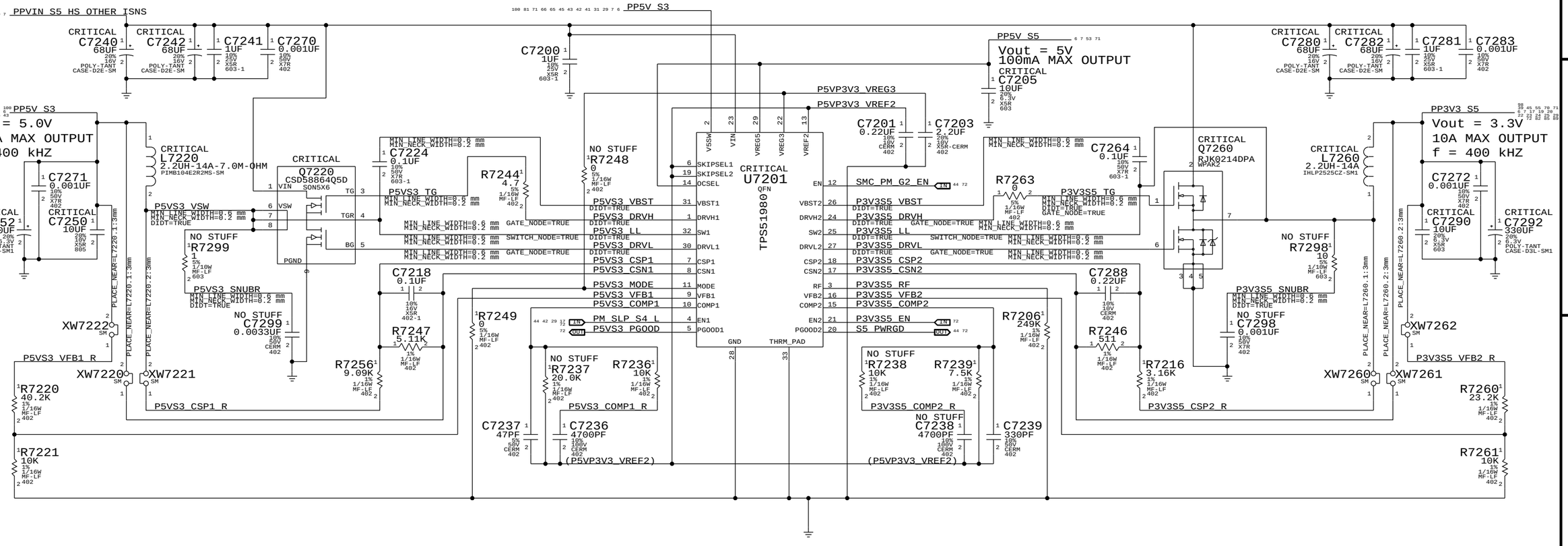
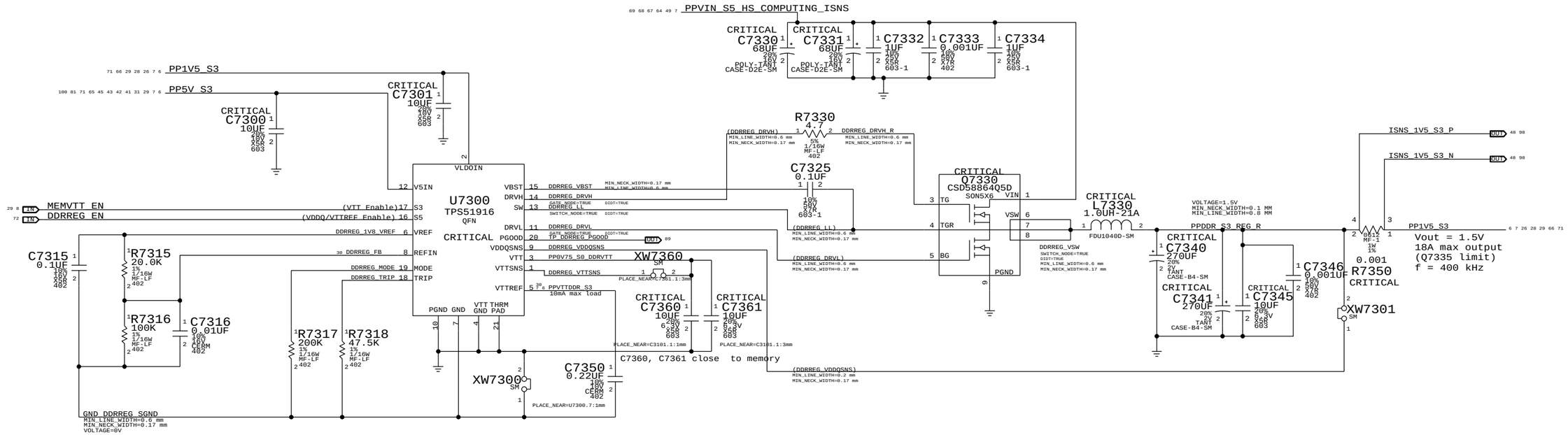


SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER · SIZE D
	REVISION
	BRANCH
	PAGE 72 OF 132
	SHEET 65 OF 101



SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER · SIZE D
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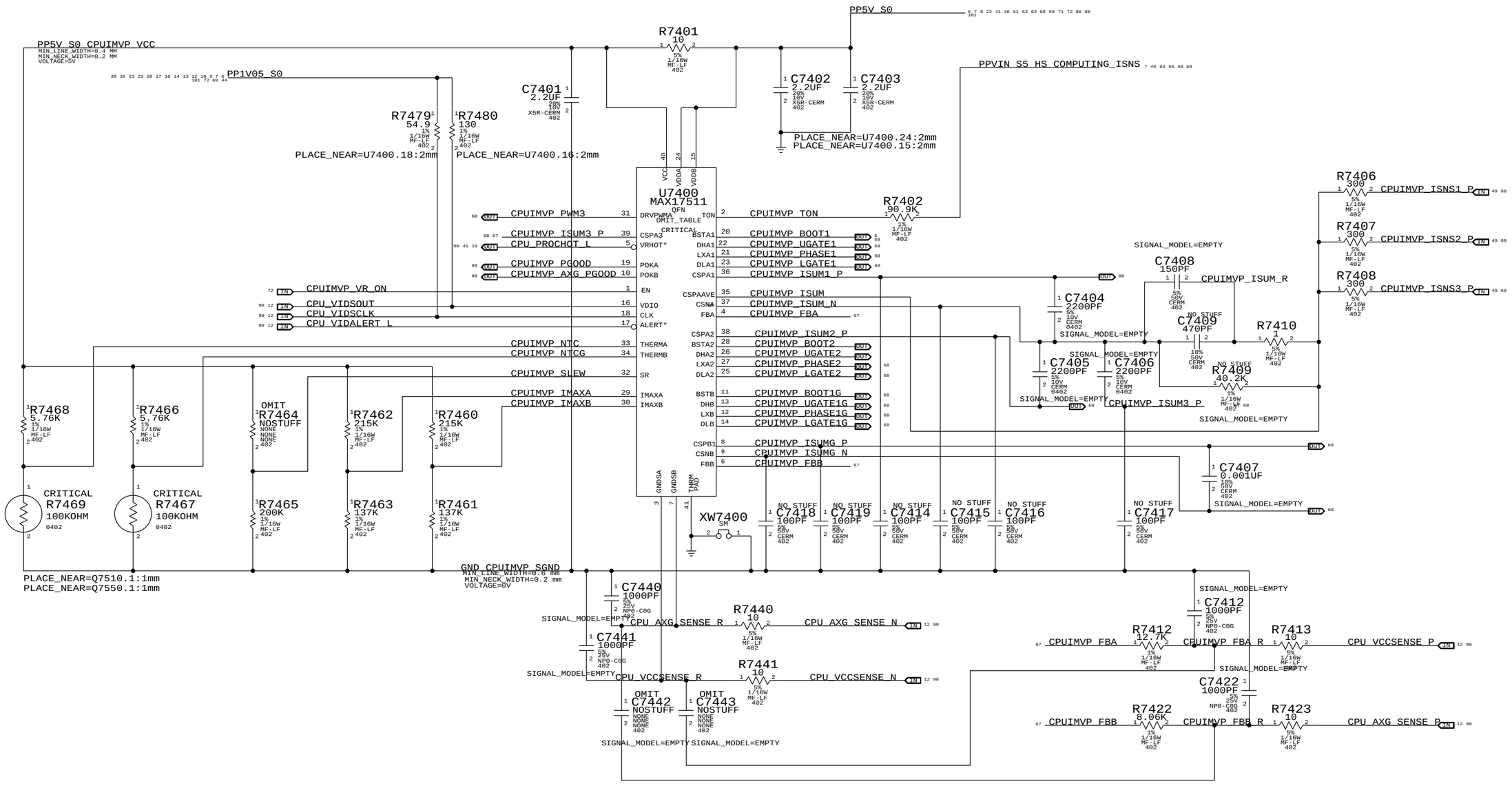
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC,MAX15092,3+1PH CPU REG,IMVP7,5X5QFN40	U7400	CRITICAL	



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER

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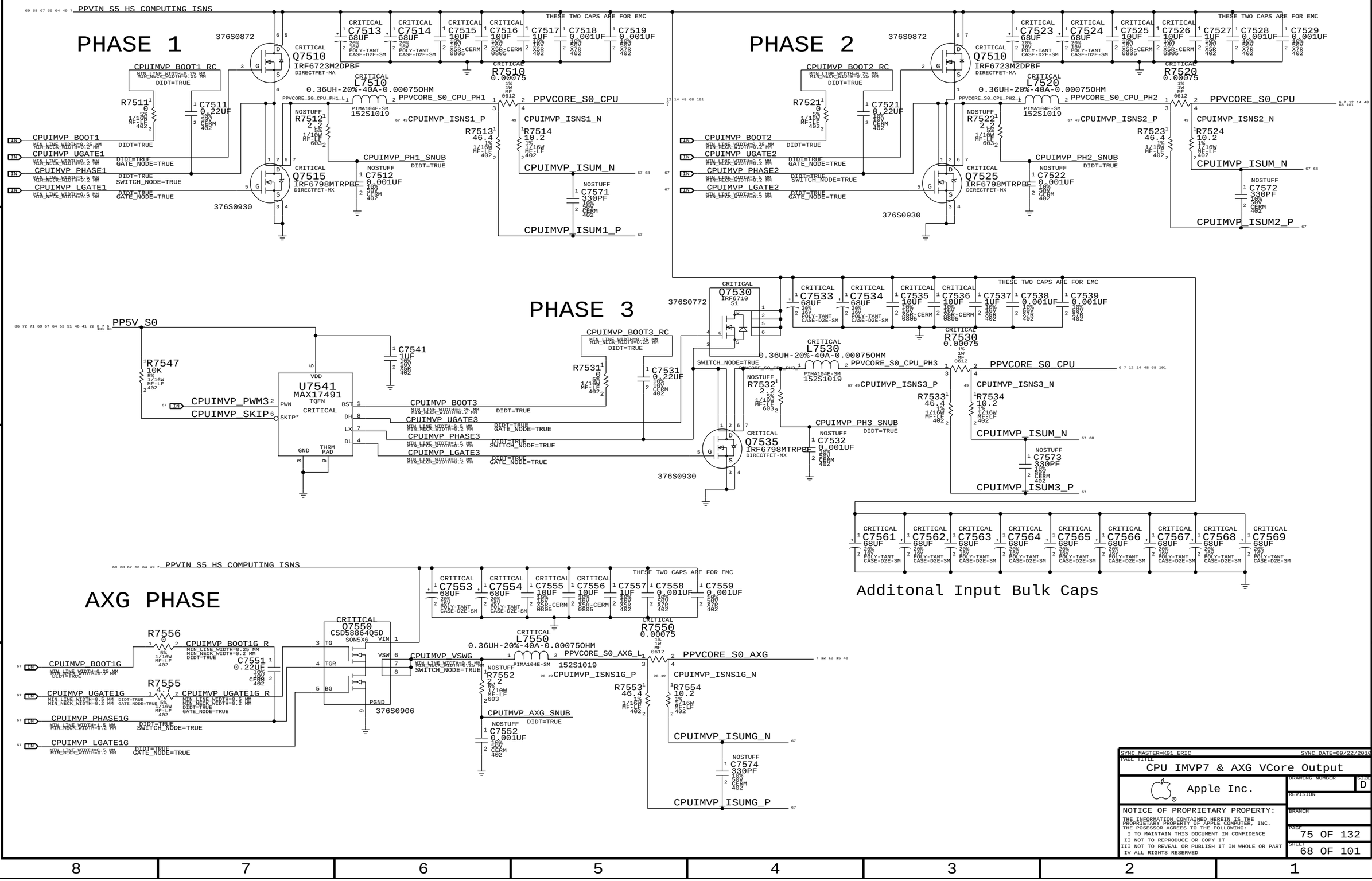
PHASE 1
PPVIN_S5_HS_COMPUTING_ISNS
376S0872
CRITICAL
Q7510
IRF6723M2DPBF
DIRECTFET-MA
CPUIMVP_BOOT1_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
DIDT=TRUE
R7511 0 5% 1/16W MF-LF 402
C7511 0.22UF 10% 10V CERM 402
CRITICAL
L7510
0.36UH-20%-40A-0.000750HM
PPVCORE_S0_CPU_PH1_L
PIMA104E-SM
152S1019
PPVCORE_S0_CPU_PH1
PPVCORE_S0_CPU
NOSTUFF
R7512 2.2 5% 1/10W MF-LF 603
CPUIMVP_ISNS1_P
CPUIMVP_ISNS1_N
R7513 46.4 1% 1/16W MF-LF 402
R7514 10.2 1% 1/16W MF-LF 402
CPUIMVP_PH1_SNUB
DIDT=TRUE
NOSTUFF
C7512 0.001UF 10% 50V X7R 402
CPUIMVP_ISUM_N
NOSTUFF
C7571 330PF 10% 50V CERM 402
CPUIMVP_ISUM1_P
THESE TWO CAPS ARE FOR EMC
CRITICAL
C7513 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7514 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL
C7515 10UF 10% 16V X5R-CERM 0805
C7516 10UF 10% 16V X5R-CERM 0805
C7517 1UF 10% 16V X5R 402
C7518 0.001UF 10% 50V X7R 402
C7519 0.001UF 10% 50V X7R 402
CRITICAL
R7510 0.00075 1% 1W MF 0612
CRITICAL
Q7515
IRF6798MTRPBF
DIRECTFET-MX
376S0930
CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
SWITCH_NODE=TRUE
GATE_NODE=TRUE
PHASE 2
376S0872
CRITICAL
Q7510
IRF6723M2DPBF
DIRECTFET-MA
CPUIMVP_BOOT2_RC
R7521 0 5% 1/16W MF-LF 402
C7521 0.22UF 10% 10V CERM 402
CRITICAL
L7520
0.36UH-20%-40A-0.000750HM
PPVCORE_S0_CPU_PH2_L
PIMA104E-SM
152S1019
PPVCORE_S0_CPU_PH2
PPVCORE_S0_CPU
NOSTUFF
R7522 2.2 5% 1/10W MF-LF 603
CPUIMVP_ISNS2_P
CPUIMVP_ISNS2_N
R7523 46.4 1% 1/16W MF-LF 402
R7524 10.2 1% 1/16W MF-LF 402
CPUIMVP_PH2_SNUB
DIDT=TRUE
NOSTUFF
C7522 0.001UF 10% 50V X7R 402
CPUIMVP_ISUM_N
NOSTUFF
C7572 330PF 10% 50V CERM 402
CPUIMVP_ISUM2_P
THESE TWO CAPS ARE FOR EMC
CRITICAL
C7523 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7524 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL
C7525 10UF 10% 16V X5R-CERM 0805
C7526 10UF 10% 16V X5R-CERM 0805
C7527 1UF 10% 16V X5R 402
C7528 0.001UF 10% 50V X7R 402
C7529 0.001UF 10% 50V X7R 402
CRITICAL
R7520 0.00075 1% 1W MF 0612
CRITICAL
Q7525
IRF6798MTRPBF
DIRECTFET-MX
376S0930
CPUIMVP_BOOT2
CPUIMVP_UGATE2
CPUIMVP_PHASE2
CPUIMVP_LGATE2
SWITCH_NODE=TRUE
GATE_NODE=TRUE
PHASE 3
376S0772
CRITICAL
Q7530
IRF6710
S1
CPUIMVP_BOOT3_RC
R7531 0 5% 1/16W MF-LF 402
C7531 0.22UF 10% 10V CERM 402
CRITICAL
L7530
0.36UH-20%-40A-0.000750HM
PPVCORE_S0_CPU_PH3_L
PIMA104E-SM
152S1019
PPVCORE_S0_CPU_PH3
PPVCORE_S0_CPU
NOSTUFF
R7532 2.2 5% 1/10W MF-LF 603
CPUIMVP_ISNS3_P
CPUIMVP_ISNS3_N
R7533 46.4 1% 1/16W MF-LF 402
R7534 10.2 1% 1/16W MF-LF 402
CPUIMVP_PH3_SNUB
DIDT=TRUE
NOSTUFF
C7532 0.001UF 10% 50V X7R 402
CPUIMVP_ISUM_N
NOSTUFF
C7573 330PF 10% 50V CERM 402
CPUIMVP_ISUM3_P
THESE TWO CAPS ARE FOR EMC
CRITICAL
C7533 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7534 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL
C7535 10UF 10% 16V X5R-CERM 0805
C7536 10UF 10% 16V X5R-CERM 0805
C7537 1UF 10% 16V X5R 402
C7538 0.001UF 10% 50V X7R 402
C7539 0.001UF 10% 50V X7R 402
CRITICAL
R7530 0.00075 1% 1W MF 0612
CRITICAL
Q7535
IRF6798MTRPBF
DIRECTFET-MX
376S0930
PP5V_S0
R7547 10K 5% 1/16W MF-LF 402
C7541 1UF 10% 16V X5R 402
U7541
MAX17491
TQFN
CRITICAL
VDD
PWN
SKIP*
BST
DH
LX
DL
GND
THRM PAD
CPUIMVP_PWM3
CPUIMVP_SKIP
CPUIMVP_BOOT3
CPUIMVP_UGATE3
CPUIMVP_PHASE3
CPUIMVP_LGATE3
Additonal Input Bulk Caps
CRITICAL
C7561 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7562 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7563 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7564 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7565 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7566 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7567 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7568 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7569 68UF 20% 16V POLY-TANT CASE-D2E-SM
PPVIN_S5_HS_COMPUTING_ISNS
AXG PHASE
THESE TWO CAPS ARE FOR EMC
CRITICAL
C7553 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7554 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL
C7555 10UF 10% 16V X5R-CERM 0805
C7556 10UF 10% 16V X5R-CERM 0805
C7557 1UF 10% 16V X5R 402
C7558 0.001UF 10% 50V X7R 402
C7559 0.001UF 10% 50V X7R 402
CRITICAL
Q7550
CSD58864Q5D
SON5X6
CRITICAL
L7550
0.36UH-20%-40A-0.000750HM
PPVCORE_S0_AXG_L
PIMA104E-SM
152S1019
PPVCORE_S0_AXG
CRITICAL
R7550 0.00075 1% 1W MF 0612
CPUIMVP_BOOT1G_R
R7556 0 5% 1/16W MF-LF 402
C7551 0.22UF 10% 10V CERM 402
R7555 4.7 5% 1/10W MF-LF 402
CPUIMVP_UGATE1G_R
CPUIMVP_VSWG
NOSTUFF
R7552 2.2 5% 1/10W MF-LF 603
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N
R7553 46.4 1% 1/16W MF-LF 402
R7554 10.2 1% 1/16W MF-LF 402
CPUIMVP_AXG_SNUB
DIDT=TRUE
NOSTUFF
C7552 0.001UF 10% 50V X7R 402
CPUIMVP_ISUMG_N
NOSTUFF
C7574 330PF 10% 50V CERM 402
CPUIMVP_ISUMG_P
376S0906
CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
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SYNC_MASTER=K91_ERIC
SYNC_DATE=09/22/2010
PAGE TITLE
CPU IMVP7 & AXG VCore Output
Apple Inc.
DRAWING NUMBER
SIZE
D
REVISION
BRANCH
PAGE
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SHEET
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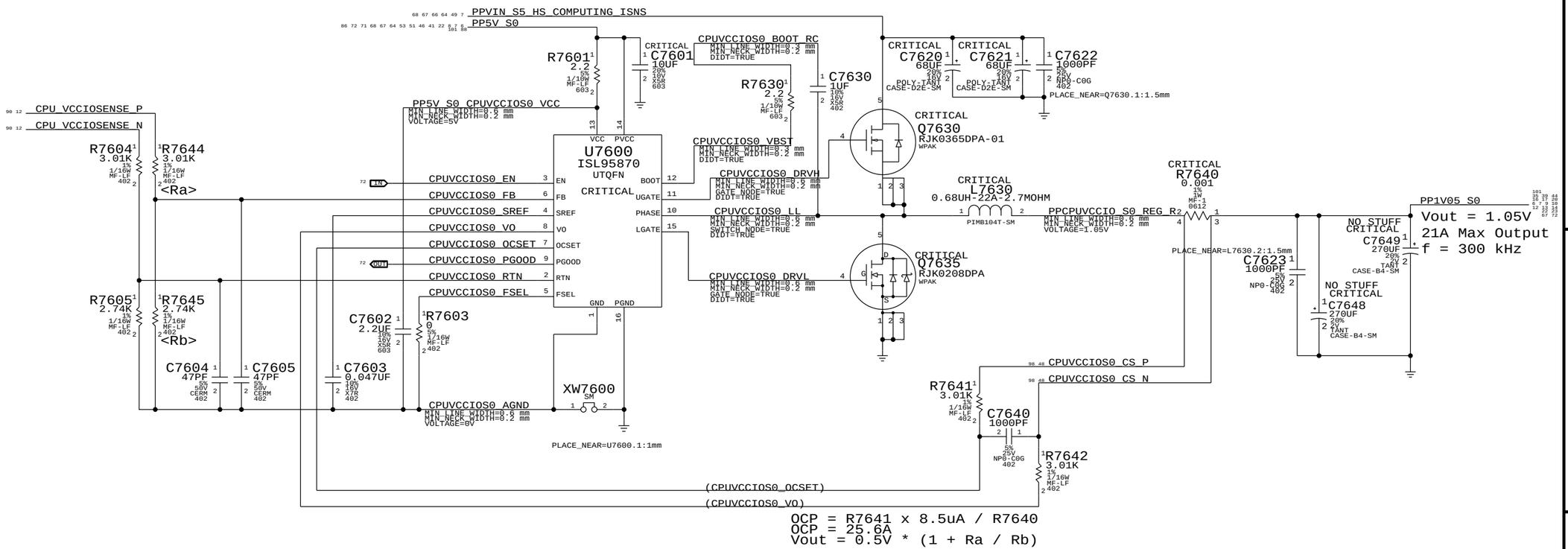
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

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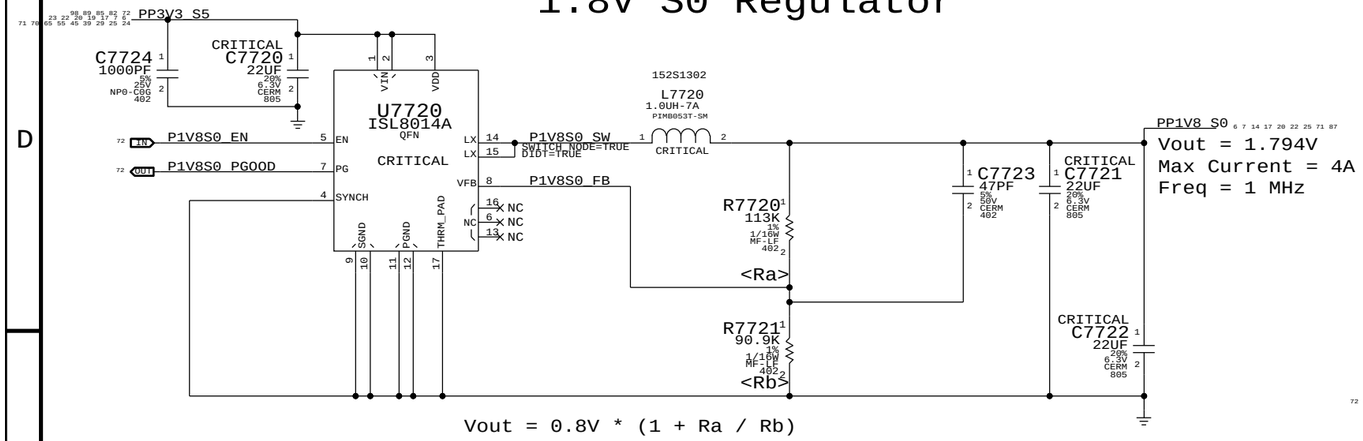
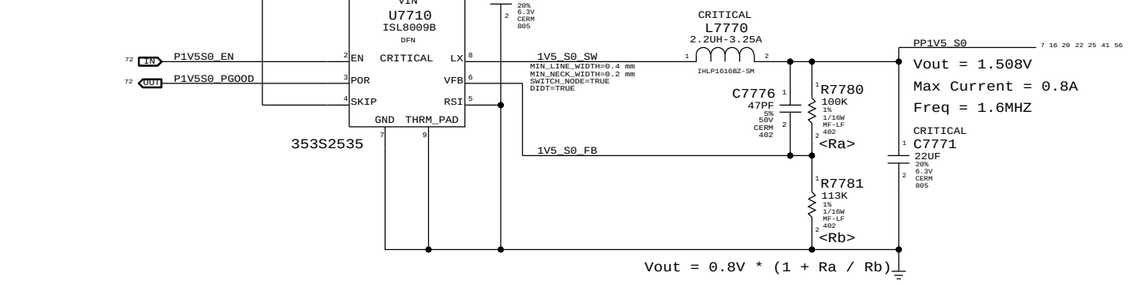
1.8V S0 Regulator



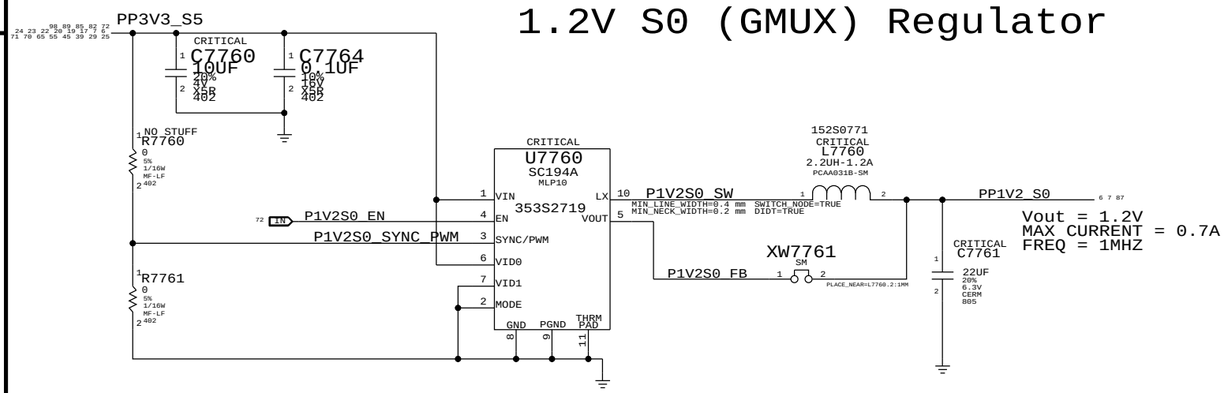
Vout = 0.8V * (1 + Ra / Rb)

1.5V S0 Regulator



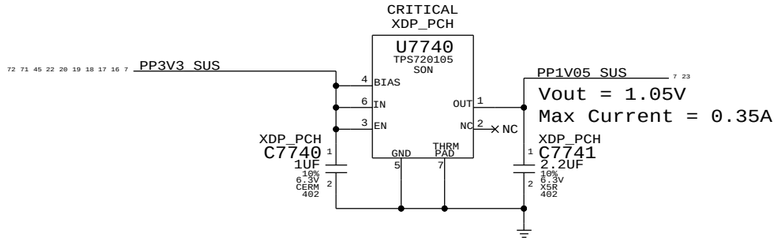
Vout = 0.8V * (1 + Ra / Rb)

1.2V S0 (GMUX) Regulator

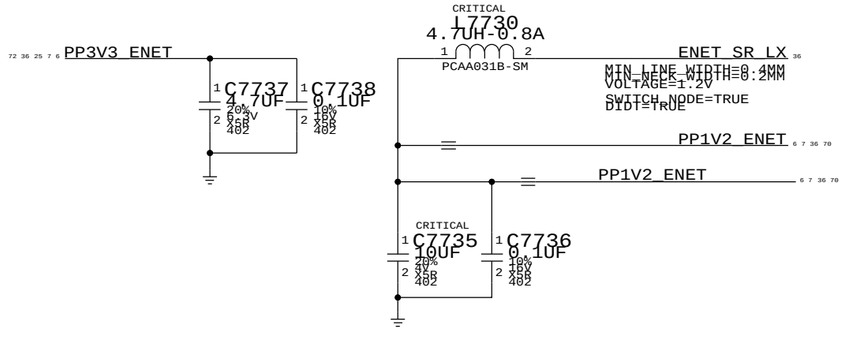


1.05V SUS LDO

Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



CAESAR IV 1.2V INT.VR CMPTS



SYNC_MASTER=K91_ERIC SYNC_DATE=11/01/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER | SIZE: D

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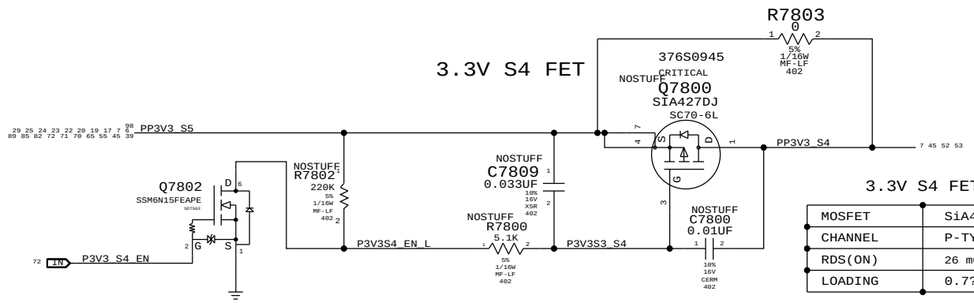
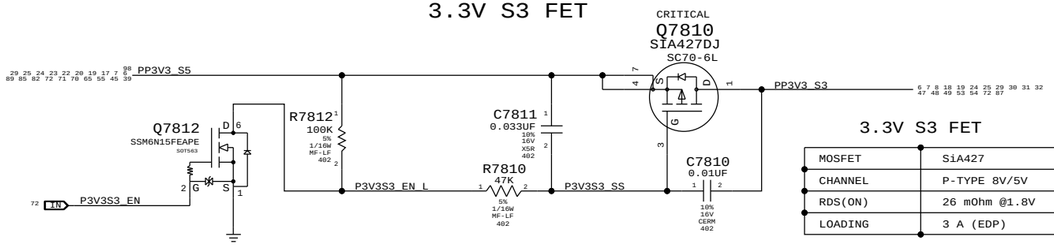
3.3V S4 FET



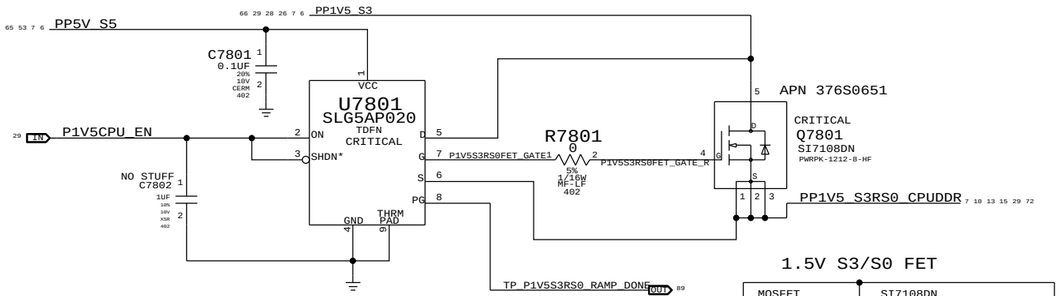
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



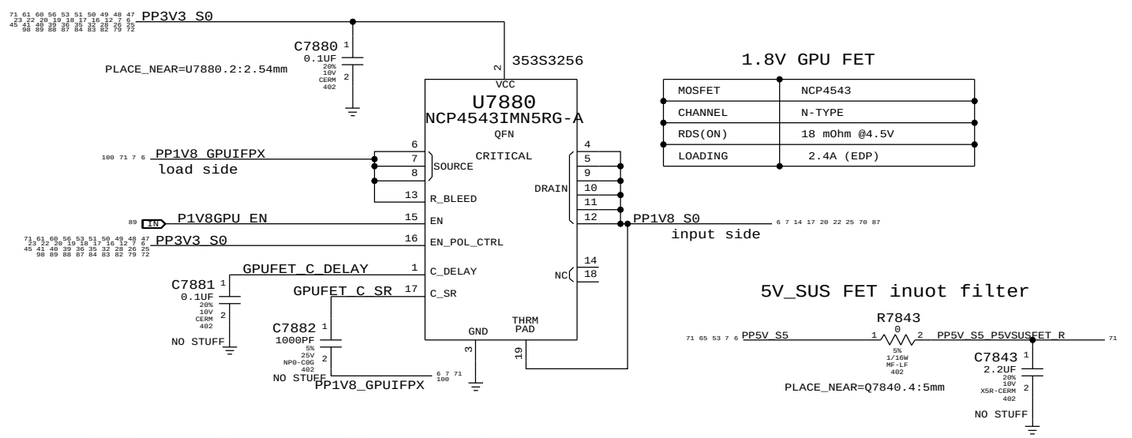
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET

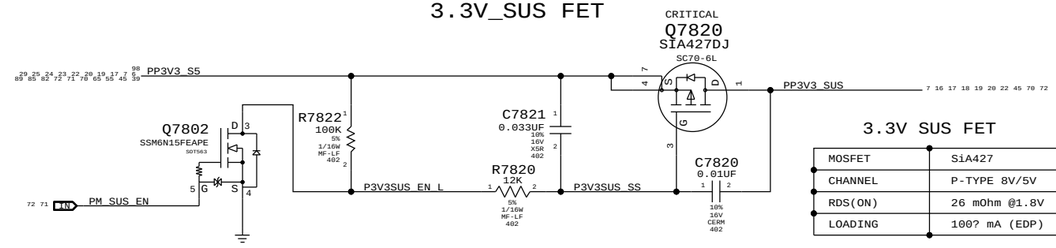


1.8V GPU FET	
MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET inuot filter

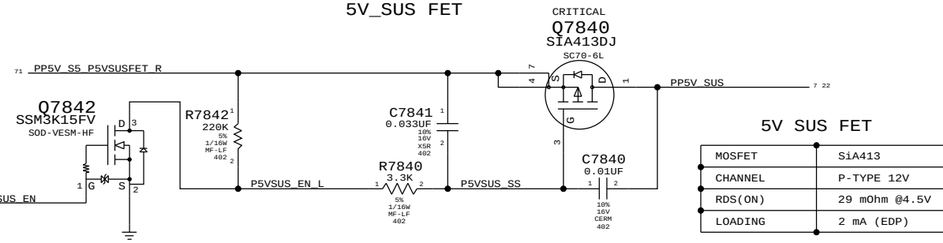
U7880 default Turn on delay EN--> on is 200~650us.

3.3V_SUS FET



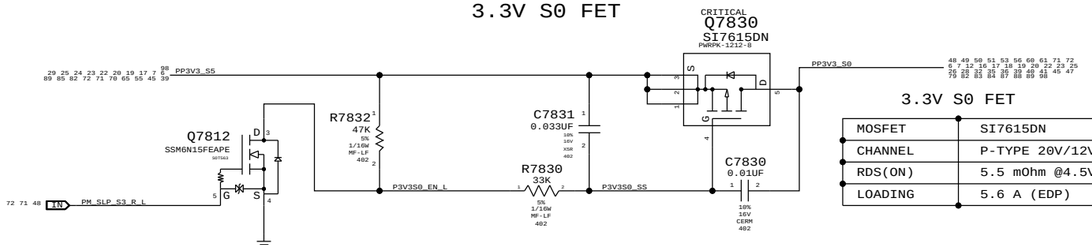
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



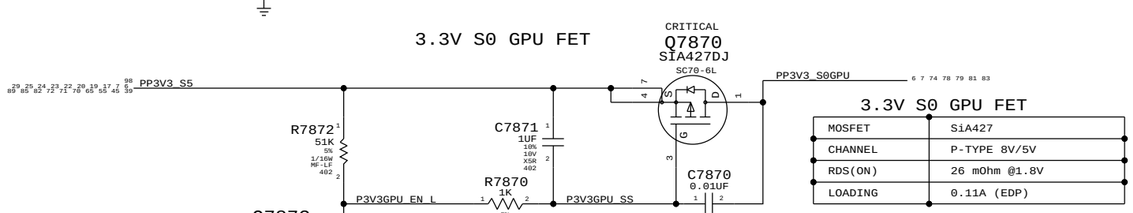
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET



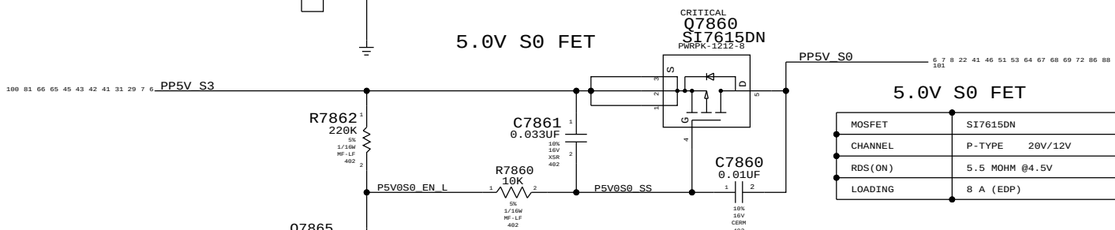
3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

3.3V S0 GPU FET



3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC_MASTER=K91_MARY SYNC_DATE=10/14/2016

PAGE TITLE: Power FETs

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S5 Rail Enables & PGOOD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

SMC_PM_G2_EN → R7940 100 → P3V3S5_EN
C7942 0.0033UF, NO STUFF
PP3V42_G3H → R7941 100K → S5_PWRGD
S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

3.3V/5.0V S4 ENABLE

PM_SLP_S5_L → NOSTUFF R7916 0 → P3V3_S4_EN
PM_SLP_S5_L:100K pull down on PCH page

3.3V/5.0V Sus ENABLE

PP3V3_S5 → C7940 0.1uF
U7940 74AUP1G3208 SOT891
SMC_BATLOW_L:100K pull up on SMC page
PM_SLP_SUS_L:100K pull down on PCH page
PM_SLP_SUS_L → PM_SUS_EN
NO STUFF R7917 0

CPUVCORE ENABLE

ALL_SYS_PWRGD → R7974 0 → CPUIMVP_VR_ON
R7976 0 NO STUFF
CPUVCCIOS0_PGOOD → R7975 0 → PM_PECI_PWRGD

S0 Rail PGOOD (BJT Version)

PP3V3_S5, PP3V3_S0
R7951 15.0K, R7956 150K
R7953 1K, R7952 7.15K, R7954 1K, R7955 1K
VMON_3V3_DIV, VMON_Q2_BASE, VMON_Q3_BASE, VMON_Q4_BASE
PP1V5_S3RS0_CPUDDR, PP1V5_S3RS0, PP1V05_S0
Q7950 ASMCC0179 DFN2015H4-8 (Q1–Q4) CRITICAL
NC, NC
S0PGD_C, ALL_SYS_PWRGD
353S2809 S0PGD_BJT_GND_R
R7957 100

Worst-Case Thresholds:
Q2: 0.XXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

PP3V3_S5 → C7930 0.1uF
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
U7930 TPS3808G33DBVRG4 SOT23-6 (SENSE, RESET*, MR*, VDD, GND, CT)
C7931 0.001UF
Sus_PGOOD_CT
PP3V3_SUS → R7933 100K
PM_RSMRST_L → PM_RSMRST_L goes to U1800.C21

S0 Rail PGOOD Circuitry

Thresholds: (ISL Version in development)
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP5V_S0 → R7960 6.04K, R7970 10K, R7972 6.04K
PP5V_DIV_VMON
PP3V3_S5 → R7956 150K
PP1V5_S3RS0_CPUDDR, PP1V05_S0 → R7961 15.0K, R7971 10K, R7973 15.0K
PP1V05_DIV_VMON, PP1V05_VID_VMON
S0PGOOD_ISL
C7960 0.1uF
U7960 ISL88042IRTEZ TDFN (IPU) CRITICAL (VDD, V2MON, V3MON, V4MON, MR*, RST*, GND, THRM_PAD)
353S2310
R7962 330 → ALL_SYS_PWRGD
PP3V3_S0 → R7967 10K
P1V5S0_PGOOD from U7710
R7968 100 P1V5S0_PGOOD
R7966 100 P1V8S0_PGOOD
R7965 100 P5VS3_PGOOD
R7964 100 CPUVCCIOS0_PGOOD
R7963 100 PVCCSA_PGOOD

SMC_S4_WAKESRC_EN → SMC_S4_WAKESRC_EN

S0 ENABLE

PM_SLP_S3_L → R7978 100 → (PM_SLP_S3_R_L)
PM_SLP_S3_L:100K pull down in PCH page
R7987 33K, R7981 20K, R7985 20K, R7988 10K, R7986 5.1K
P1V8S0_EN, P1V5S0_EN, P1V2S0_EN, CPUVCCIOS0_EN, PVCCSA_EN
C7987 0.47UF, C7981 0.47UF, C7985 1UF, C7988 0.47UF, C7986 0.47UF

CHGR VFRQ Generation

PP3V42_G3H → R7931 100K → CHGR_VFRQ
Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

3.3V,5V S3 ENABLE

PM_SLP_S4_L → (PM_SLP_S4_L)
PM_SLP_S4_L:100K pull down in PCH page
R7911 5.1K, R7912 0, R7913 3.3K
TPAD_VBUS_EN
P3V3S3_EN, DDRREG_EN
C7910 0.47UF, C7912 0.47UF NO STUFF

ENET Enable Generation

3.3V ENET FET

Q7922 NTR4101P SOT-23-HF (CRITICAL)
PP3V3_S3 → R7921 10K → PM_SLP_S3_ENET
R7922 100K
C7921 0.033UF, C7922 0.01UF
PP3V3ENET_SS, PP3V3_ENET

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

Q7921 SSM3K15FV SOD-VESM-HF
PM_SLP_S3_L
Q7925 2N7002DW-X-G SOT-363 (WOL_EN)
Q7925 2N7002DW-X-G SOT-363 (PM_WLAN_EN_L, AP_PWR_EN)
Q7920 2N7002DW-X-G SOT-363 (AC_EN_L)
Q7920 2N7002DW-X-G SOT-363 (SMC_ADAPTER_EN)
NO STUFF R7929 0 (PM_SLP_S3_L)

SYNC_MASTER=K91_MARY SYNC_DATE=07/22/2010
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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEG_R2D_C_P<0>	C8020	0.1UF	10%6.3V5R201	PEG_R2D_P<0>
PEG_R2D_C_N<0>	C8021	0.1UF	10%6.3V5R201	PEG_R2D_N<0>
PEG_R2D_C_P<1>	C8022	0.1UF	10%6.3V5R201	PEG_R2D_P<1>
PEG_R2D_C_N<1>	C8023	0.1UF	10%6.3V5R201	PEG_R2D_N<1>
PEG_R2D_C_P<2>	C8024	0.1UF	10%6.3V5R201	PEG_R2D_P<2>
PEG_R2D_C_N<2>	C8025	0.1UF	10%6.3V5R201	PEG_R2D_N<2>
PEG_R2D_C_P<3>	C8026	0.1UF	10%6.3V5R201	PEG_R2D_P<3>
PEG_R2D_C_N<3>	C8027	0.1UF	10%6.3V5R201	PEG_R2D_N<3>
PEG_R2D_C_P<4>	C8028	0.1UF	10%6.3V5R201	PEG_R2D_P<4>
PEG_R2D_C_N<4>	C8029	0.1UF	10%6.3V5R201	PEG_R2D_N<4>
PEG_R2D_C_P<5>	C8030	0.1UF	10%6.3V5R201	PEG_R2D_P<5>
PEG_R2D_C_N<5>	C8031	0.1UF	10%6.3V5R201	PEG_R2D_N<5>
PEG_R2D_C_P<6>	C8032	0.1UF	10%6.3V5R201	PEG_R2D_P<6>
PEG_R2D_C_N<6>	C8033	0.1UF	10%6.3V5R201	PEG_R2D_N<6>
PEG_R2D_C_P<7>	C8034	0.1UF	10%6.3V5R201	PEG_R2D_P<7>
PEG_R2D_C_N<7>	C8035	0.1UF	10%6.3V5R201	PEG_R2D_N<7>

PEG_D2R_C_P<0>	C8055	0.1UF	10%6.3V5R201	PEG_D2R_P<0>
PEG_D2R_C_N<0>	C8056	0.1UF	10%6.3V5R201	PEG_D2R_N<0>
PEG_D2R_C_P<1>	C8057	0.1UF	10%6.3V5R201	PEG_D2R_P<1>
PEG_D2R_C_N<1>	C8058	0.1UF	10%6.3V5R201	PEG_D2R_N<1>
PEG_D2R_C_P<2>	C8059	0.1UF	10%6.3V5R201	PEG_D2R_P<2>
PEG_D2R_C_N<2>	C8060	0.1UF	10%6.3V5R201	PEG_D2R_N<2>
PEG_D2R_C_P<3>	C8061	0.1UF	10%6.3V5R201	PEG_D2R_P<3>
PEG_D2R_C_N<3>	C8062	0.1UF	10%6.3V5R201	PEG_D2R_N<3>
PEG_D2R_C_P<4>	C8063	0.1UF	10%6.3V5R201	PEG_D2R_P<4>
PEG_D2R_C_N<4>	C8064	0.1UF	10%6.3V5R201	PEG_D2R_N<4>
PEG_D2R_C_P<5>	C8065	0.1UF	10%6.3V5R201	PEG_D2R_P<5>
PEG_D2R_C_N<5>	C8066	0.1UF	10%6.3V5R201	PEG_D2R_N<5>
PEG_D2R_C_P<6>	C8067	0.1UF	10%6.3V5R201	PEG_D2R_P<6>
PEG_D2R_C_N<6>	C8068	0.1UF	10%6.3V5R201	PEG_D2R_N<6>
PEG_D2R_C_P<7>	C8069	0.1UF	10%6.3V5R201	PEG_D2R_P<7>
PEG_D2R_C_N<7>	C8070	0.1UF	10%6.3V5R201	PEG_D2R_N<7>

PM_ALL_GPU_PGOOD — R8003 NOSTUFF 0 5% 1/16W MF-LF 402 — EG_RESET_L — R8000 0 5% 1/16W MF-LF 402 — GPU_RESET_R_L

R8004 10K 5% 1/16W MF-LF 402

PEG_R2D_C_P<0>	AA38	PCIE_RX0P
PEG_R2D_C_N<0>	Y37	PCIE_RX0N
PEG_R2D_C_P<1>	Y35	PCIE_RX1P
PEG_R2D_C_N<1>	W36	PCIE_RX1N
PEG_R2D_C_P<2>	W38	PCIE_RX2P
PEG_R2D_C_N<2>	V37	PCIE_RX2N
PEG_R2D_C_P<3>	V35	PCIE_RX3P
PEG_R2D_C_N<3>	U36	PCIE_RX3N
PEG_R2D_C_P<4>	U38	PCIE_RX4P
PEG_R2D_C_N<4>	T37	PCIE_RX4N
PEG_R2D_C_P<5>	T35	PCIE_RX5P
PEG_R2D_C_N<5>	R36	PCIE_RX5N
PEG_R2D_C_P<6>	R38	PCIE_RX6P
PEG_R2D_C_N<6>	P37	PCIE_RX6N
PEG_R2D_C_P<7>	P35	PCIE_RX7P
PEG_R2D_C_N<7>	N36	PCIE_RX7N
NC	N38	PCIE_RX8P
NC	M37	PCIE_RX8N
NC	M35	PCIE_RX9P
NC	L36	PCIE_RX9N
NC	L38	PCIE_RX10P
NC	K37	PCIE_RX10N
NC	K35	PCIE_RX11P
NC	J36	PCIE_RX11N
NC	J38	PCIE_RX12P
NC	H37	PCIE_RX12N
NC	H35	PCIE_RX13P
NC	G36	PCIE_RX13N
NC	G38	PCIE_RX14P
NC	F37	PCIE_RX14N
NC	F35	PCIE_RX15P
NC	E37	PCIE_RX15N
PEG_CLK100M_P	AB35	PCIE_REFCLKP
PEG_CLK100M_N	AA36	PCIE_REFCLKN
GPU_PWRGOOD	AH16	PWRGOOD
GPU_RESET_R_L	AA30	PERST*

U8000
FCBGA
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PCIE
WHISTLER
40NM-ES

OMIT

PCIE_TX0P	Y33	PEG_D2R_C_P<0>
PCIE_TX0N	Y32	PEG_D2R_C_N<0>
PCIE_TX1P	W33	PEG_D2R_C_P<1>
PCIE_TX1N	W32	PEG_D2R_C_N<1>
PCIE_TX2P	U33	PEG_D2R_C_P<2>
PCIE_TX2N	U32	PEG_D2R_C_N<2>
PCIE_TX3P	U30	PEG_D2R_C_P<3>
PCIE_TX3N	U29	PEG_D2R_C_N<3>
PCIE_TX4P	T33	PEG_D2R_C_P<4>
PCIE_TX4N	T32	PEG_D2R_C_N<4>
PCIE_TX5P	T30	PEG_D2R_C_P<5>
PCIE_TX5N	T29	PEG_D2R_C_N<5>
PCIE_TX6P	P33	PEG_D2R_C_P<6>
PCIE_TX6N	P32	PEG_D2R_C_N<6>
PCIE_TX7P	P30	PEG_D2R_C_P<7>
PCIE_TX7N	P29	PEG_D2R_C_N<7>
PCIE_TX8P	N33	NC
PCIE_TX8N	N32	NC
PCIE_TX9P	N30	NC
PCIE_TX9N	N29	NC
PCIE_TX10P	L33	NC
PCIE_TX10N	L32	NC
PCIE_TX11P	L30	NC
PCIE_TX11N	L29	NC
PCIE_TX12P	K33	NC
PCIE_TX12N	K32	NC
PCIE_TX13P	J33	NC
PCIE_TX13N	J32	NC
PCIE_TX14P	K30	NC
PCIE_TX14N	K29	NC
PCIE_TX15P	H33	NC
PCIE_TX15N	H32	NC
PCIE_CALRP	Y30	PEG_CALRP
PCIE_CALRN	Y29	PEG_CALRN

R8001 2.0K 1% 1/16W MF-LF 402
R8002 1.27K 1% 1/16W MF-LF 402

PP1V0_S0GPU_ISNS

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

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Apple Inc.

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Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V0_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V8_GPU_PCIE_VDDC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

PP1V5_S0GPU_ISNS
TBD mA
C8100 10UF 20% 10V X5R 603
C8101 10UF 20% 10V X5R 603
C8102 10UF 20% 10V X5R 603
C8103 10UF 20% 10V X5R 603
C8104 10UF 20% 10V X5R 603
C8105 1UF 10% 25V X5R 402
C8106 1UF 10% 25V X5R 402
C8107 1UF 10% 25V X5R 402
C8108 1UF 10% 25V X5R 402
C8109 1UF 10% 25V X5R 402
C8110 1UF 10% 25V X5R 402
C8111 1UF 10% 25V X5R 402
C8112 1UF 10% 25V X5R 402
C8113 1UF 10% 25V X5R 402
C8114 1UF 10% 25V X5R 402
C8115 0.1UF 10% 6.3V X5R 201
C8116 0.1UF 10% 6.3V X5R 201
C8117 0.1UF 10% 6.3V X5R 201
C8118 0.1UF 10% 6.3V X5R 201
C8119 0.1UF 10% 6.3V X5R 201
C8120 0.1UF 10% 6.3V X5R 201
C8121 0.1UF 10% 6.3V X5R 201
C8122 0.1UF 10% 6.3V X5R 201
C8123 0.1UF 10% 6.3V X5R 201
C8124 0.1UF 10% 6.3V X5R 201

L8120 120OHM-0.3A 0402 CRITICAL
PP1V8_S0GPU_ISNS

PP1V8_GPU_VDD_CT
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
219mA
C8125 10UF 20% 10V X5R 603
C8126 1UF 10% 25V X5R 402
C8127 1UF 10% 25V X5R 402
C8128 1UF 10% 25V X5R 402
C8129 0.1UF 10% 6.3V X5R 201

L8130 470OHM-1A-150MOHM 0603 CRITICAL
PP1V0_S0GPU_ISNS
PP1V0_GPU_PLL
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V
C8130 10UF 20% 10V X5R 603
C8131 1UF 10% 25V X5R 402
C8132 0.1UF 10% 6.3V X5R 201
GND_GPU_PLL

PP3V3_S0GPU
60 mA
C8133 10UF 20% 10V X5R 603
C8134 1UF 10% 25V X5R 402
C8135 1UF 10% 25V X5R 402
C8136 1UF 10% 25V X5R 402

L8131 4700HM-1A-150MOHM 0603 CRITICAL
PP1V8_S0GPU_ISNS
PP1V8_GPU_MEM_PLL
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8137 10UF 20% 10V X5R 603
C8138 1UF 10% 25V X5R 402
C8139 1UF 10% 25V X5R 402
C8140 0.1UF 10% 6.3V X5R 201
C8141 0.1UF 10% 6.3V X5R 201

PP1V8_GPU_VDDR4
TBD mA

L8132 120OHM-0.3A 0402 CRITICAL
PP1V8_S0GPU_ISNS
PP1V8_GPU_PLL
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
75mA
C8142 10UF 20% 10V X5R 603
C8143 1UF 10% 25V X5R 402
C8144 0.1UF 10% 6.3V X5R 201

XW8100 SM
PP1V0_GPU_PLL
120mA
GND_GPU_PLL

L8140 FERR-220-OHM-2A 0603 CRITICAL
PP1V8_S0GPU_ISNS
PP1V8_GPU_PCIE_VDDR
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
504mA
C8145 10UF 20% 10V X5R 603
C8146 1UF 10% 25V X5R 402
C8147 1UF 10% 25V X5R 402
C8148 1UF 10% 25V X5R 402
C8149 0.1UF 10% 6.3V X5R 201
C8150 0.1UF 10% 6.3V X5R 201

GPU_VDD_SENSE
GPU_GND_SENSE

L8155 FERR-120-OHM-3A 0603 CRITICAL
PP1V0_S0GPU_ISNS
PP1V0_GPU_PCIE_VDDC
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V
1920mA
C8151 10UF 20% 10V X5R 603
C8152 1UF 10% 25V X5R 402
C8153 1UF 10% 25V X5R 402
C8154 1UF 10% 25V X5R 402
C8155 1UF 10% 25V X5R 402
C8156 1UF 10% 25V X5R 402
C8157 1UF 10% 25V X5R 402
C8158 1UF 10% 25V X5R 402

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AC7	VDDR1_AC7	OMIT
AD11	VDDR1_AD11	
AF7	VDDR1_AF7	
AG10	VDDR1_AG10	
AJ7	VDDR1_AJ7	
AK8	VDDR1_AK8	
AL9	VDDR1_AL9	
G11	VDDR1_G11	
G14	VDDR1_G14	
G17	VDDR1_G17	
G20	VDDR1_G20	
G23	VDDR1_G23	
G26	VDDR1_G26	
G29	VDDR1_G29	
H10	VDDR1_H10	
J7	VDDR1_J7	
J9	VDDR1_J9	
K8	VDDR1_K8	
K11	VDDR1_K11	MEM I/O
K13	VDDR1_K13	
L7	VDDR1_L7	
L12	VDDR1_L12	
L16	VDDR1_L16	
L21	VDDR1_L21	
L23	VDDR1_L23	
L26	VDDR1_L26	
M11	VDDR1_M11	
N11	VDDR1_N11	
P7	VDDR1_P7	
R11	VDDR1_R11	
U7	VDDR1_U7	
U11	VDDR1_U11	
Y7	VDDR1_Y7	
Y11	VDDR1_Y11	
AF26	VDD_CT_AF26	LEVEL TRNSL
AF27	VDD_CT_AF27	
AG26	VDD_CT_AG26	
AG27	VDD_CT_AG27	
AF23	VDDR3_AF23	CORE
AF24	VDDR3_AF24	
AG23	VDDR3_AG23	
AG24	VDDR3_AG24	
AF13	VDDR4_AF13	
AF15	VDDR4_AF15	
AG13	VDDR4_AG13	
AG15	VDDR4_AG15	
AD12	VDDR4_AD12	I/O
AF11	VDDR4_AF11	
AF12	VDDR4_AF12	
AG11	VDDR4_AG11	
M20	NC/VDDRHA	NC
M21	NC/VSSRHA	NC
U12	NC/VSSRHB	NC
V12	NC/VDDRHB	NC
H7	MPV18_H7	PLL
H8	MPV18_H8	
AM10	SPV18	
AN9	SPV10	
AN10	SPVSS	
AF28	FB_VDDC	VOLT SENSE
AG28	FB_VDDCI	NC
AH29	FB_GND	
AA31	PCIE_VDDR_AA31	PCIE ISOLATED CORE I/O
AA32	PCIE_VDDR_AA32	
AA33	PCIE_VDDR_AA33	
AA34	PCIE_VDDR_AA34	
AB37	PCIE_VDDR_AB37	
V28	PCIE_VDDR_V28	
W29	PCIE_VDDR_W29	
W30	PCIE_VDDR_W30	
Y31	PCIE_VDDR_Y31	
G30	PCIE_VDDC_G30	
G31	PCIE_VDDC_G31	
H29	PCIE_VDDC_H29	
H30	PCIE_VDDC_H30	
J29	PCIE_VDDC_J29	
J30	PCIE_VDDC_J30	
L28	PCIE_VDDC_L28	
M28	PCIE_VDDC_M28	
N28	PCIE_VDDC_N28	
R28	PCIE_VDDC_R28	
T28	PCIE_VDDC_T28	
U28	PCIE_VDDC_U28	

L8150 120OHM-0.3A 0402 CRITICAL
PP1V8_S0GPU_ISNS
PP1V8_GPU_VDDR4
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C81C0 1UF 10% 25V X5R 402
C81C1 0.1UF 10% 6.3V X5R 201

PPVCORE_GPU

VDDC_AA15	AA15	C8160 C8161 C8162 C8163 C8164 C8165 C8166 C8167 C8168 C8169 1UF 10% 25V X5R 402
VDDC_AA17	AA17	
VDDC_AA20	AA20	
VDDC_AA22	AA22	
VDDC_AA24	AA24	
VDDC_AA27	AA27	
VDDC_AB16	AB16	
VDDC_AB18	AB18	
VDDC_AB21	AB21	
VDDC_AB23	AB23	
VDDC_AB26	AB26	
VDDC_AB28	AB28	
VDDC_AC17	AC17	C8170 C8171 C8172 C8173 C8174 C8175 C8176 C8177 C8178 C8179 1UF 10% 25V X5R 402
VDDC_AC20	AC20	
VDDC_AC22	AC22	
VDDC_AC24	AC24	
VDDC_AC27	AC27	
VDDC_AD18	AD18	
VDDC_AD21	AD21	
VDDC_AD23	AD23	
VDDC_AD26	AD26	
VDDC_AF17	AF17	C8180 C8181 C8182 C8183 C8184 C8185 C8186 C8187 C8188 C8189 1UF 10% 25V X5R 402
VDDC_AF20	AF20	
VDDC_AF22	AF22	
VDDC_AG16	AG16	
VDDC_AG18	AG18	
VDDC_AG21	AG21	
VDDC_AH22	AH22	
VDDC_AH27	AH27	
VDDC_AH28	AH28	
VDDC_M26	M26	C8190 C8191 C8192 C8193 C8194 C8195 C8196 C8197 C8198 C8199 10UF 20% 10V X5R 603
VDDC_N24	N24	
BIF_VDDC_N27	N27	
VDDC_R18	R18	
VDDC_R21	R21	
VDDC_R23	R23	
VDDC_R26	R26	
VDDC_T17	T17	
VDDC_T20	T20	
VDDC_T22	T22	
VDDC_T24	T24	
BIF_VDDC_T27	T27	
VDDC_U16	U16	
VDDC_U18	U18	
VDDC_U21	U21	
VDDC_U23	U23	
VDDC_U26	U26	
VDDC_V17	V17	
VDDC_V20	V20	
VDDC_V22	V22	
VDDC_V24	V24	
VDDC_V27	V27	
VDDC_Y16	Y16	
VDDC_Y18	Y18	
VDDC_Y21	Y21	
VDDC_Y23	Y23	
VDDC_Y26	Y26	
VDDC_Y28	Y28	
VDDCI_AA13	AA13	C81A0 C81A1 C81A2 C81A3 C81A4 C81A5 C81A6 C81A7 C81A8 C81A9 1UF 10% 25V X5R 402
VDDCI_AB13	AB13	
VDDCI_AC12	AC12	
VDDCI_AC15	AC15	
VDDCI_AD13	AD13	
VDDCI_AD16	AD16	
VDDCI_M15	M15	C81B0 C81B1 C81B2 10UF 20% 10V X5R 603
VDDCI_M16	M16	
VDDCI_M18	M18	
VDDCI_M23	M23	
VDDCI_N13	N13	
VDDCI_N15	N15	
VDDCI_N17	N17	
VDDCI_N20	N20	
VDDCI_N22	N22	
VDDCI_R12	R12	
VDDCI_R13	R13	
VDDCI_R16	R16	
VDDCI_T12	T12	
VDDCI_T15	T15	
VDDCI_V15	V15	
VDDCI_Y13	Y13	

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010
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Whistler CORE/FB POWER

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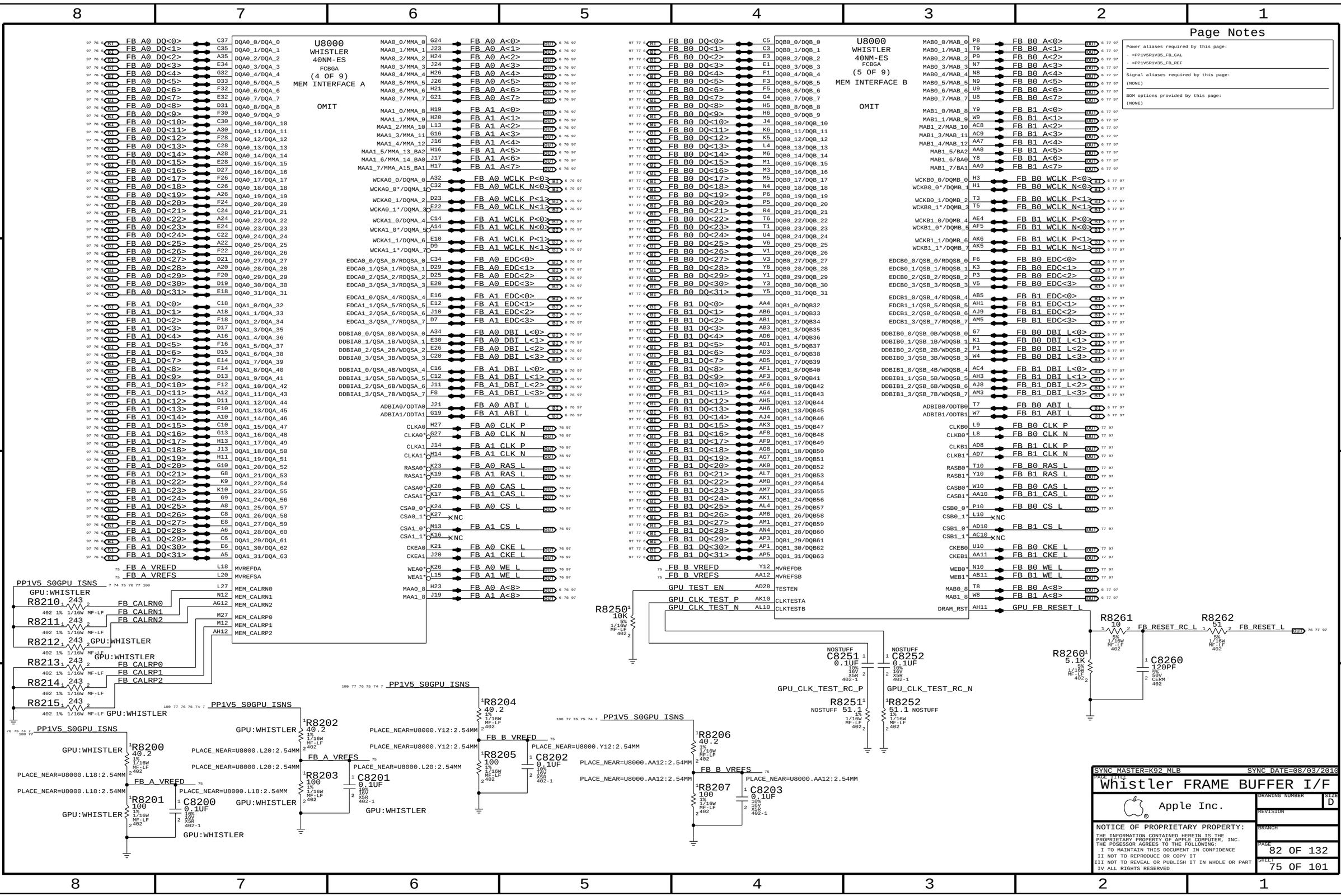
U8000
WHISTLER
40NM-ES
FCBGA
(4 OF 9)
MEM INTERFACE A
OMIT
U8000
WHISTLER
40NM-ES
FCBGA
(5 OF 9)
MEM INTERFACE B
OMIT
Page Notes
Power aliases required by this page:
- =PP1V5R1V35_FB_CAL
- =PP1V5R1V35_FB_REF
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
PP1V5_S0GPU_ISNS
GPU:WHISTLER
FB_A_VREFD
FB_A_VREFS
FB_B_VREFD
FB_B_VREFS
GPU_TEST_EN
GPU_CLK_TEST_P
GPU_CLK_TEST_N
GPU_CLK_TEST_RC_P
GPU_CLK_TEST_RC_N
FB_RESET_RC_L
FB_RESET_L
GPU_FB_RESET_L
SYNC_MASTER=K92_MLB
SYNC_DATE=08/03/2016
PAGE TITLE
Whistler FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER
SIZE
D
REVISION
BRANCH
PAGE
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75 OF 101
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Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
GPU:WHISTLER is the BOM option called out on all Rs and Cs on this page

GPU:WHISTLER is the BOM option called out on ALL Rs and Cs on this page!

U8400 — 32MX32-1.25GHZ-MFL (BGA, H5GQ1H24AFR-T2C) (1 OF 2) OMIT

FB_A0_A<2>	H11	BA0/A2
FB_A0_A<5>	K10	BA1/A5
FB_A0_A<4>	K11	BA2/A4
FB_A0_A<3>	H10	BA3/A3
FB_A0_A<7>	K4	A8/A7
FB_A0_A<1>	H5	A9/A1
FB_A0_A<0>	H4	A10/A0
FB_A0_A<6>	K5	A11/A6
FB_A0_CKE_L	J3	CKE*
FB_A0_CLK_P	J12	CK
FB_A0_CLK_N	J11	CK*
FB_A0_CS_L	G12	CS*
FB_A0_WE_L	L12	WE*
FB_A0_CAS_L	L3	CAS*
FB_A0_RAS_L	G3	RAS*
FB_A0_ZQ	J13	ZQ
FB_A0_MF	J1	MF (MF=0)
FB_A0_SEN	J10	SEN
FB_RESET_L	J2	RESET*
FB_A0_ABI_L	J4	ABI*
FB_A0_EDC<0>	C2	EDC0
FB_A0_EDC<1>	C13	EDC1
FB_A0_EDC<3>	R13	EDC2
FB_A0_EDC<2>	R2	EDC3
FB_A0_WCLK_P<0>	D4	WCK01
FB_A0_WCLK_N<0>	D5	WCK01*
FB_A0_WCLK_P<1>	P4	WCK23
FB_A0_WCLK_N<1>	P5	WCK23*

DBI0*	D2	FB_A0_DBI_L<0>
DBI1*	D13	FB_A0_DBI_L<1>
DBI2*	P13	FB_A0_DBI_L<3>
DBI3*	P2	FB_A0_DBI_L<2>

DQ0	A4	FB_A0_DQ<0>
DQ1	A2	FB_A0_DQ<1>
DQ2	B4	FB_A0_DQ<2>
DQ3	B2	FB_A0_DQ<3>
DQ4	E4	FB_A0_DQ<4>
DQ5	E2	FB_A0_DQ<5>
DQ6	F4	FB_A0_DQ<6>
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DQ9	A13	FB_A0_DQ<9>
DQ10	B11	FB_A0_DQ<10>
DQ11	B13	FB_A0_DQ<11>
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DQ13	E13	FB_A0_DQ<12>
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DQ15	F13	FB_A0_DQ<31>
DQ16	U11	FB_A0_DQ<30>
DQ17	U13	FB_A0_DQ<29>
DQ18	T11	FB_A0_DQ<28>
DQ19	T13	FB_A0_DQ<26>
DQ20	N11	FB_A0_DQ<27>
DQ21	N13	FB_A0_DQ<24>
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DQ23	M13	FB_A0_DQ<20>
DQ24	U4	FB_A0_DQ<23>
DQ25	U2	FB_A0_DQ<21>
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DQ27	T2	FB_A0_DQ<17>
DQ28	N4	FB_A0_DQ<18>
DQ29	N2	FB_A0_DQ<16>
DQ30	M4	FB_A0_DQ<19>
DQ31	M2	

A5, J5, U5 — NC; NC — FB_A0_A<8>

U8450 — 32MX32-1.25GHZ-MFL (BGA, H5GQ1H24AFR-T2C) (1 OF 2) OMIT

FB_A1_A<2>	H11	BA0/A2
FB_A1_A<5>	K10	BA1/A5
FB_A1_A<4>	K11	BA2/A4
FB_A1_A<3>	H10	BA3/A3
FB_A1_A<7>	K4	A8/A7
FB_A1_A<1>	H5	A9/A1
FB_A1_A<0>	H4	A10/A0
FB_A1_A<6>	K5	A11/A6
FB_A1_CKE_L	J3	CKE*
FB_A1_CLK_P	J12	CK
FB_A1_CLK_N	J11	CK*
FB_A1_CS_L	G12	CS*
FB_A1_WE_L	L12	WE*
FB_A1_CAS_L	L3	CAS*
FB_A1_RAS_L	G3	RAS*
FB_A1_ZQ	J13	ZQ
FB_A1_MF	J1	MF (MF=0)
FB_A1_SEN	J10	SEN
FB_RESET_L	J2	RESET*
FB_A1_ABI_L	J4	ABI*
FB_A1_EDC<0>	C2	EDC0
FB_A1_EDC<1>	C13	EDC1
FB_A1_EDC<2>	R13	EDC2
FB_A1_EDC<3>	R2	EDC3
FB_A1_WCLK_P<0>	D4	WCK01
FB_A1_WCLK_N<0>	D5	WCK01*
FB_A1_WCLK_P<1>	P4	WCK23
FB_A1_WCLK_N<1>	P5	WCK23*

DBI0*	D2	FB_A1_DBI_L<0>
DBI1*	D13	FB_A1_DBI_L<1>
DBI2*	P13	FB_A1_DBI_L<2>
DBI3*	P2	FB_A1_DBI_L<3>

DQ0	A4	FB_A1_DQ<1>
DQ1	A2	FB_A1_DQ<0>
DQ2	B4	FB_A1_DQ<3>
DQ3	B2	FB_A1_DQ<2>
DQ4	E4	FB_A1_DQ<4>
DQ5	E2	FB_A1_DQ<6>
DQ6	F4	FB_A1_DQ<5>
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DQ8	A11	FB_A1_DQ<9>
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DQ11	B13	FB_A1_DQ<10>
DQ12	E11	FB_A1_DQ<12>
DQ13	E13	FB_A1_DQ<13>
DQ14	F11	FB_A1_DQ<14>
DQ15	F13	FB_A1_DQ<15>
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DQ17	U13	FB_A1_DQ<22>
DQ18	T11	FB_A1_DQ<23>
DQ19	T13	FB_A1_DQ<20>
DQ20	N11	FB_A1_DQ<18>
DQ21	N13	FB_A1_DQ<19>
DQ22	M11	FB_A1_DQ<17>
DQ23	M13	FB_A1_DQ<16>
DQ24	U4	FB_A1_DQ<31>
DQ25	U2	FB_A1_DQ<30>
DQ26	T4	FB_A1_DQ<28>
DQ27	T2	FB_A1_DQ<29>
DQ28	N4	FB_A1_DQ<25>
DQ29	N2	FB_A1_DQ<27>
DQ30	M4	FB_A1_DQ<24>
DQ31	M2	FB_A1_DQ<26>

A5, J5, U5 — NC; NC — FB_A1_A<8>

U8400 — 32MX32-1.25GHZ-MFL (BGA, H5GQ1H24AFR-T2C) (2 OF 2) OMIT

VDD: C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10

VDDQ: B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14

VSS: B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10

VSSQ: A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14

FB_A0_VREFC	J14	VREFC
FB_A0_VREFD1	A10	
FB_A0_VREFD2	U10	VREFD

U8450 — 32MX32-1.25GHZ-MFL (BGA, H5GQ1H24AFR-T2C) (2 OF 2) OMIT

VDD: C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10

VDDQ: B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14

VSS: B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10

VSSQ: A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14

FB_A1_VREFC	J14	VREFC
FB_A1_VREFD1	A10	
FB_A1_VREFD2	U10	VREFD

PP1V5_S0GPU_ISNS

R8401 60.4 1% 1/16W MF-LF 402; R8402 60.4 1% 1/16W MF-LF 402

R8400 120 1% 1/20W MF 201; R8404 120 1% 1/20W MF 201; R8403 120 1% 1/20W MF 201

R8451 60.4 1% 1/16W MF-LF 402; R8452 60.4 1% 1/16W MF-LF 402

R8450 120 1% 1/20W MF 201; R8454 120 1% 1/20W MF 201; R8453 120 1% 1/20W MF 201

C8400 4.7UF 20% 6.3V X5R 402; C8401 4.7UF 20% 6.3V X5R 402; C8402 4.7UF 20% 6.3V X5R 402

C8403 4.7UF 20% 6.3V X5R 402; C8404 4.7UF 20% 6.3V X5R 402; C8405 4.7UF 20% 6.3V X5R 402

C8406 1UF 10% 6.3V CERM-X5R 402; C8407 1UF 10% 6.3V CERM-X5R 402; C8408 1UF 10% 6.3V CERM-X5R 402; C8409 1UF 10% 6.3V CERM-X5R 402

C8410 1UF 10% 6.3V CERM-X5R 402; C8411 1UF 10% 6.3V CERM-X5R 402; C8412 1UF 10% 6.3V CERM-X5R 402; C8413 1UF 10% 6.3V CERM-X5R 402

C8414 1UF 10% 6.3V CERM-X5R 402; C8415 1UF 10% 6.3V CERM-X5R 402; C8416 0.1UF 10% 6.3V X5R 201; C8417 0.1UF 10% 6.3V X5R 201

C8418 0.1UF 10% 6.3V X5R 201; C8419 0.1UF 10% 6.3V X5R 201; C8420 0.1UF 10% 6.3V X5R 201; C8421 0.1UF 10% 6.3V X5R 201

C8422 0.1UF 10% 6.3V X5R 201; C8423 0.1UF 10% 6.3V X5R 201; C8424 0.1UF 10% 6.3V X5R 201; C8425 0.1UF 10% 6.3V X5R 201

R8430 2.37K 1% 1/16W MF-LF 402; C8430 1UF 10% 6.3V CERM-X5R 402

R8431 5.49K 1% 1/16W MF-LF 402; C8431 1UF 10% 6.3V CERM-X5R 402

R8432 2.37K 1% 1/16W MF-LF 402; C8432 1UF 10% 6.3V CERM-X5R 402

R8433 5.49K 1% 1/16W MF-LF 402; C8433 1UF 10% 6.3V CERM-X5R 402

R8434 2.37K 1% 1/16W MF-LF 402; C8434 1UF 10% 6.3V CERM-X5R 402

R8435 5.49K 1% 1/16W MF-LF 402; C8435 1UF 10% 6.3V CERM-X5R 402

C8450 4.7UF 20% 6.3V X5R 402; C8451 4.7UF 20% 6.3V X5R 402; C8452 4.7UF 20% 6.3V X5R 402

C8453 4.7UF 20% 6.3V X5R 402; C8454 4.7UF 20% 6.3V X5R 402; C8455 4.7UF 20% 6.3V X5R 402

C8456 1UF 10% 6.3V CERM-X5R 402; C8457 1UF 10% 6.3V CERM-X5R 402; C8458 1UF 10% 6.3V CERM-X5R 402; C8459 1UF 10% 6.3V CERM-X5R 402

C8460 1UF 10% 6.3V CERM-X5R 402; C8461 1UF 10% 6.3V CERM-X5R 402; C8462 1UF 10% 6.3V CERM-X5R 402; C8463 1UF 10% 6.3V CERM-X5R 402

C8464 1UF 10% 6.3V CERM-X5R 402; C8465 1UF 10% 6.3V CERM-X5R 402; C8466 0.1UF 10% 6.3V X5R 201; C8467 0.1UF 10% 6.3V X5R 201

C8468 0.1UF 10% 6.3V X5R 201; C8469 0.1UF 10% 6.3V X5R 201; C8470 0.1UF 10% 6.3V X5R 201; C8471 0.1UF 10% 6.3V X5R 201

C8472 0.1UF 10% 6.3V X5R 201; C8473 0.1UF 10% 6.3V X5R 201; C8474 0.1UF 10% 6.3V X5R 201; C8475 0.1UF 10% 6.3V X5R 201

R8480 2.37K 1% 1/16W MF-LF 402; C8480 1UF 10% 6.3V CERM-X5R 402

R8481 5.49K 1% 1/16W MF-LF 402; C8481 1UF 10% 6.3V CERM-X5R 402

R8482 2.37K 1% 1/16W MF-LF 402; C8482 1UF 10% 6.3V CERM-X5R 402

R8483 5.49K 1% 1/16W MF-LF 402; C8483 1UF 10% 6.3V CERM-X5R 402

R8484 2.37K 1% 1/16W MF-LF 402; C8484 1UF 10% 6.3V CERM-X5R 402

R8485 5.49K 1% 1/16W MF-LF 402; C8485 1UF 10% 6.3V CERM-X5R 402

SYNC_MASTER=K92_MLB	SYNC_DATE=08/19/2016
PAGE TITLE	GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER: — SIZE: D
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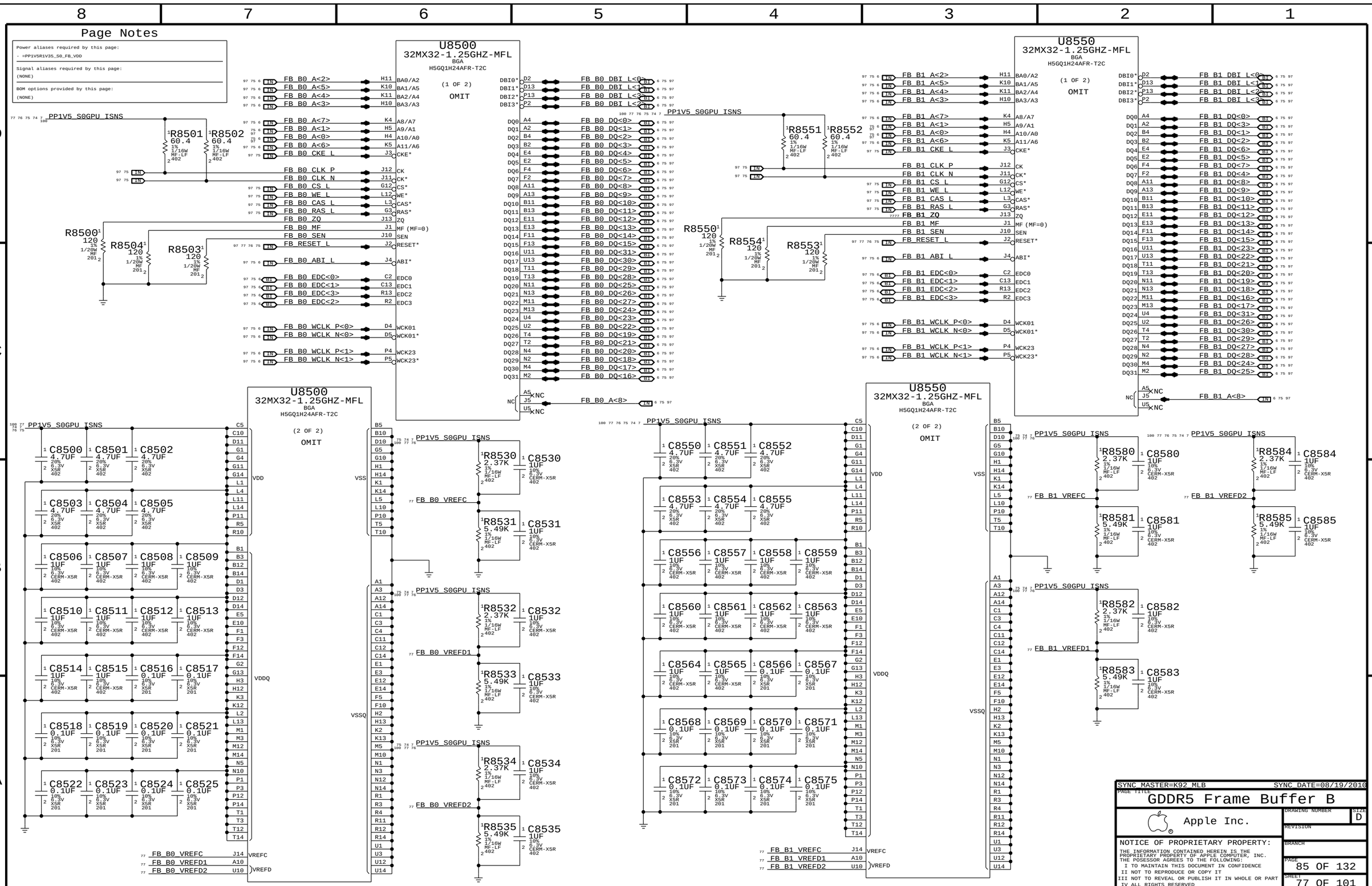
Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K92_MLB	SYNC_DATE=08/19/2010
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER: — SIZE: D
	REVISION:
	BRANCH:
	PAGE: 85 OF 132
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VRAM BOM OPTION TABLE

	VRAM_DVP0 (STUFF R8613?)	VRAM_DVP1 (STUFF R8612?)	VRAM_DVP2 (STUFF R8611?)
K92 SAMSUNG 1G	NO	NO	YES
K92 HYNIX 1G	YES	NO	YES
K91F SAMSUNG 512M	NO	NO	NO
K91F HYNIX 512M	NO	YES	NO
K91F SAMSUNG 1G	YES	NO	NO
K91F HYNIX 1G	YES	YES	NO

NOTE: AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

K91FSamsung 512M - NOSTUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 512M - NOSTUFF R8613, STUFF R8612, NOSTUFF R8611
K91FSamsung 1G - STUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 1G - STUFF R8613, STUFF R8612, NOSTUFF R8611

NO STRAP CHANGES ARE REQUIRED FOR SEYMOUR BASED SYSTEMS

PP1V8_S0GPU_ISNS — R8610 10K 5% 1/16W MF-LF 402 NOSTUFF; R8611 10K 5% 1/16W MF-LF 402 VRAM_DVP2; R8612 10K 5% 1/16W MF-LF 402 VRAM_DVP1; R8613 10K 5% 1/16W MF-LF 402 VRAM_DVP0

PP3V3_S0GPU — R8600 4.7K 5% 1/16W MF-LF 402; R8601 4.7K 5% 1/16W MF-LF 402

PP1V8_S0GPU_ISNS — R8602 499 1% 1/16W MF-LF 402; C8600 0.1UF 10% 16V X5R 402-1; R8603 249 1% 1/16W MF-LF 402

L8600 CRITICAL 470OHM-1A-150MOHM 0603 — PP1V8_S0GPU_ISNS VOLTAGE=1.8V — C8601 10UF 20% 10V X5R 603; C8602 1UF 10% 16V X5R 402; C8603 0.1UF 10% 16V X5R 402-1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

L8601 CRITICAL 470OHM-1A-150MOHM 0603 — PP1V0_S0GPU_ISNS — C8604 10UF 20% 10V X5R 603; C8605 1UF 10% 25V X5R 402; C8606 0.1UF 10% 16V X5R 402-1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1V

XW8600 SM — GND_GPU_DPLL — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

L8602 CRITICAL 120OHM-0.3A 0402 — PP1V8_S0GPU_ISNS — C8607 10UF 20% 10V X5R 603; C8608 1UF 10% 25V X5R 402; C8609 0.1UF 10% 16V X5R 402-1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

XW8601 SM — GND_GPU_TSVSS — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

U8000 WHISTLER 40NM-ES FCBGA (2 OF 9)

TP_DVPCNTL_M<0>	AR8	DVPCNTL_MVP_0	
TP_DVPCNTL_M<1>	AU8	DVPCNTL_MVP_1	
TP_DVPCNTL<0>	AP8	DVPCNTL_0	
TP_DVPCNTL<1>	AW8	DVPCNTL_1	
TP_DVPCNTL<2>	AR3	DVPCNTL_2	
TP_DVPCLK	AR1	DVPCLK	
DVPDATA<0>	AU1	DVPDATA_0	
DVPDATA<1>	AU3	DVPDATA_1	
DVPDATA<2>	AW3	DVPDATA_2	
DVPDATA<3>	AP6	DVPDATA_3	
TP_DVPDATA<4>	AW5	DVPDATA_4	
TP_DVPDATA<5>	AU5	DVPDATA_5	
TP_DVPDATA<6>	AR6	DVPDATA_6	
TP_DVPDATA<7>	AW6	DVPDATA_7	
TP_DVPDATA<8>	AU6	DVPDATA_8	
TP_DVPDATA<9>	AT7	DVPDATA_9	
TP_DVPDATA<10>	AV7	DVPDATA_10	
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TP_DVPDATA<18>	AV11	DVPDATA_18	
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TP_DVPDATA<20>	AR12	DVPDATA_20	
TP_DVPDATA<21>	AW12	DVPDATA_21	
TP_DVPDATA<22>	AU12	DVPDATA_22	
TP_DVPDATA<23>	AP12	DVPDATA_23	
NC	AJ21	SWAPLOCKA	
NC	AK21	SWAPLOCKB	
GPU_I2C_SCL	AK26	SCL	I2C
GPU_I2C_SDA	AJ26	SDA	
GPU_PCIE_TX_PWR	AH20	GPIO_0	
GPU_GPIO_TX_DEEMP	AH18	GPIO_1	
GPU_PCIE_GEN2	AN16	GPIO_2	
GPU_SMB_DAT	AH23	GPIO_3_SMBDATA	
GPU_SMB_CLK	AJ23	GPIO_4_SMBCLK	
GPU_AC_BATT	AH17	GPIO_5_AC_BATT	
GPU_VCORE_VID0	AJ17	GPIO_6	
EG_BKLT_EN	AK17	GPIO_7_BLON	
GPU_ROM_SO	AJ13	GPIO_8_ROMSO	
GPU_ROM_SI	AH15	GPIO_9_ROMSI	
GPU_ROM_SCLK	AJ16	GPIO_10_ROMSCK	
GPU_CONFIG_0	AK16	GPIO_11	
GPU_CONFIG_1	AL16	GPIO_12	
GPU_CONFIG_2	AM16	GPIO_13	
DP_T29SNK0_HPD_GPU	AM14	GPIO_14_HPD2	
GPU_VCORE_VID1	AM13	GPIO_15_PWRCNTL_0	
GPU_VCORE_VID2	AK14	GPIO_16	
SMC_GFX_THROTTLE_R_L	AG30	GPIO_17_THERMAL_INT	
DP_T29SNK1_HPD_GPU	AN14	GPIO_18_HPD3	
SMC_GFX_OVERTEMP_R_L	AM17	GPIO_19_CTF	
GPU_VCORE_VID3	AL13	GPIO_20_PWRCNTL_1	
FBVDD_ALTVO	AJ14	GPIO_21_BB_EN	
GPU_ROM_CS_L	AK13	GPIO_22_ROMCS*	
PEX_CLKREQ_L_R	AN13	GPIO_23_CLKREQ*	
TP_GPU_JTAG_TRST_L	AM23	JTAG_TRST*	GPIO
TP_GPU_JTAG_TDI	AN23	JTAG_TDI	
TP_GPU_JTAG_TCK	AK23	JTAG_TCK	
TP_GPU_JTAG_TMS	AL24	JTAG_TMS	
TP_GPU_JTAG_TDO	AM24	JTAG_TDO	
NC_GPU_GENERICA	AJ19	GENERICA	
NC_GPU_GENERICB	AK19	GENERICB	
NC_GPU_GENERICC	AJ20	GENERICC	
DP_CA_DET_EG_R	AK20	GENERICD	
NC_GPU_GENERICE	AJ24	GENERICE_HPD4	
NC_GPU_GENERICF	AH26	GENERICF_HPD5	
NC_GPU_GENERICG	AH24	GENERICG_HPD6	
DP_EG_HPD	AK24	HPD1	
GPU_VREFG	AH13	VREFG	
PP1V8_GPU_DPLL 75mA (GND_GPU_DPLL)	AM32	DPLL_PVDD	
	AN32	DPLL_PVSS	
PP1V0_GPU_DPLL 125mA	AN31	DPLL_VDDC	
NC	AV33	XTALIN	PLL/CLK
NC	AU34	XTALOUT	
GPU_CLK27M	AW34	XO_IN	
GPU_CLK100M	AW35	XO_IN2	
GPU_TDIODE_P	AF29	DPLUS	THERMAL
GPU_TDIODE_N	AG29	DMINUS	
NC	AK32	TS_FDO	
NC	AL31	TSA/NC	
PP1V8_GPU_TSVDD 20mA (GND_GPU_TSVSS)	AJ32	TSVDD	
	AJ33	TSVSS	

OMIT: DVPDATA<3>, TP_DVPDATA<4>, TP_DVPDATA<5>, TP_DVPDATA<6>, TP_DVPDATA<7>, TP_DVPDATA<8>, TP_DVPDATA<9>, TP_DVPDATA<10>, TP_DVPDATA<11>, TP_DVPDATA<12>, TP_DVPDATA<13>, TP_DVPDATA<14>, TP_DVPDATA<15>, TP_DVPDATA<16>, TP_DVPDATA<17>, TP_DVPDATA<18>, TP_DVPDATA<19>, TP_DVPDATA<20>, TP_DVPDATA<21>, TP_DVPDATA<22>, TP_DVPDATA<23>

TXCAP_DPA3P	AU24	DP_EXTA_ML_C_P<3>	OUT
TXCAM_DPA3N	AV23	DP_EXTA_ML_C_N<3>	OUT
TX0P_DPA2P	AT25	DP_EXTA_ML_C_P<2>	OUT
TX0M_DPA2N	AR24	DP_EXTA_ML_C_N<2>	OUT
TX1P_DPA1P	AU26	DP_EXTA_ML_C_P<1>	OUT
TX1M_DPA1N	AV25	DP_EXTA_ML_C_N<1>	OUT
TX2P_DPA0P	AT27	DP_EXTA_ML_C_P<0>	OUT
TX2M_DPA0N	AR26	DP_EXTA_ML_C_N<0>	OUT
TXCBP_DPB3P	AR30	DP_T29SNK0_ML_C_P<3>	OUT
TXCBM_DPB3N	AT29	DP_T29SNK0_ML_C_N<3>	OUT
TX3P_DPB2P	AV31	DP_T29SNK0_ML_C_P<2>	OUT
TX3M_DPB2N	AU30	DP_T29SNK0_ML_C_N<2>	OUT
TX4P_DPB1P	AR32	DP_T29SNK0_ML_C_P<1>	OUT
TX4M_DPB1N	AT31	DP_T29SNK0_ML_C_N<1>	OUT
TX5P_DPB0P	AT33	DP_T29SNK0_ML_C_P<0>	OUT
TX5M_DPB0N	AU32	DP_T29SNK0_ML_C_N<0>	OUT
TXCCP_DPC3P	AU14	DP_T29SNK1_ML_C_P<3>	OUT
TXCCM_DPC3N	AV13	DP_T29SNK1_ML_C_N<3>	OUT
TX0P_DPC2P	AT15	DP_T29SNK1_ML_C_P<2>	OUT
TX0M_DPC2N	AR14	DP_T29SNK1_ML_C_N<2>	OUT
TX1P_DPC1P	AU16	DP_T29SNK1_ML_C_P<1>	OUT
TX1M_DPC1N	AV15	DP_T29SNK1_ML_C_N<1>	OUT
TX2P_DPC0P	AT17	DP_T29SNK1_ML_C_P<0>	OUT
TX2M_DPC0N	AR16	DP_T29SNK1_ML_C_N<0>	OUT
TXCDP_DPD3P	AU20	NC	
TXCDM_DPD3N	AT19	NC	
TX3P_DPD2P	AT21	NC	
TX3M_DPD2N	AR20	NC	
TX4P_DPD1P	AU22	NC	
TX4M_DPD1N	AV21	NC	
TX5P_DPD0P	AT23	NC	
TX5M_DPD0N	AR22	NC	
R	AD39	NC	
R*	AD37	NC	
G	AE36	NC	
G*	AD35	NC	
B	AF37	NC	
B*	AE38	NC	
HSYNC	AC36	GPU_AUD_1	
VSYNC	AC38	GPU_AUD_0	
RSET	AB34	NC	
AVDD	AD34	PP1V8_S0GPU_ISNS	
AVSSQ	AE34		
VDD1DI	AC33		
VSS1DI	AC34		
R2/NC	AC30	NC	DAC1
R2*/NC	AC31	NC	
G2/NC	AD30	NC	
G2*/NC	AD31	NC	
B2/NC	AF30	NC	
B2*/NC	AF31	NC	
C/NC	AC32	NC	
Y/NC	AD32	NC	
COMP/NC	AF32	NC	
H2SYNC/GENLK_CLK	AD29	NC	DAC2
V2SYNC/GENLK_VSYNC	AC29	NC	
VDD2DI/NC	AG31	NC	
VSS2DI/NC	AG32	NC	
A2VDD/NC	AG33	NC	
A2VDDQ/NC	AD33	NC	
A2VSSQ/TSVSSQ	AF33	GND_GPU_TVSSQ	
R2SET/NC	AA29	NC	
DDC1CLK	AM26	DP_EG_DDC_CLK	OUT
DDC1DATA	AN26	DP_EG_DDC_DATA	BI
AUX1P	AM27	DP_EG_AUXCH_P	BI
AUX1N	AL27	DP_EG_AUXCH_N	BI
DDC2CLK	AM19	NC	
DDC2DATA	AL19	NC	
AUX2P	AN20	DP_T29SNK0_AUXCH_C_P	BI
AUX2N	AM20	DP_T29SNK0_AUXCH_C_N	BI
DDCCLK_AUX3P	AL30	DP_T29SNK1_AUXCH_C_P	BI
DDCDATA_AUX3N	AM30	DP_T29SNK1_AUXCH_C_N	BI
DDCCLK_AUX4P	AL29	NC	
DDCDATA_AUX4N	AM29	NC	
DDCCLK_AUX5P	AN21	LVDS_EG_DDC_CLK	OUT
DDCDATA_AUX5N	AM21	LVDS_EG_DDC_DATA	BI
DDC6CLK	AJ30	NC	
DDC6DATA	AJ31	NC	
DDCCLK_AUX7P	AK30	NC	
DDCDATA_AUX7N	AK29	NC	

XW8602 SM — GND_GPU_TVSSQ — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

PP3V3_S0GPU — Straps for audio on DP and HDMI — R8604 10K 5% 1/16W MF-LF 402; R8605 10K 5% 1/16W MF-LF 402

U8000 WHISTLER 40NM-ES FCBGA (3 OF 9) LVDS CNTL

VARY_BL	AK27	LVDS_EG_BLK_PWM	
DIGON	AJ27	EG_LCD_PWR_EN	OUT
TXCLK_UP_DPF3P	AK35	NC_LVDS_EG_B_CLK_P	
TXCLK_UN_DPF3N	AL36	NC_LVDS_EG_B_CLK_N	
TXOUT_U0P_DPF2P	AJ38	LVDS_EG_B_DATA_P<0>	OUT
TXOUT_U0N_DPF2N	AK37	LVDS_EG_B_DATA_N<0>	OUT
TXOUT_U1P_DPF1P	AH35	LVDS_EG_B_DATA_P<1>	OUT
TXOUT_U1N_DPF1N	AJ36	LVDS_EG_B_DATA_N<1>	OUT
TXOUT_U2P_DPF0P	AG38	LVDS_EG_B_DATA_P<2>	OUT
TXOUT_U2N_DPF0N	AH37	LVDS_EG_B_DATA_N<2>	OUT
TXOUT_U3P	AF35	NC_LVDS_EG_B_DATA_P<3>	
TXOUT_U3N	AG36	NC_LVDS_EG_B_DATA_N<3>	
TXCLK_LP_DPE3P	AP34	LVDS_EG_A_CLK_P	OUT
TXCLK_LN_DPE3N	AR34	LVDS_EG_A_CLK_N	OUT
TXOUT_L0P_DPE2P	AW37	LVDS_EG_A_DATA_P<0>	OUT
TXOUT_L0N_DPE2N	AU35	LVDS_EG_A_DATA_N<0>	OUT
TXOUT_L1P_DPE1P	AR37	LVDS_EG_A_DATA_P<1>	OUT
TXOUT_L1N_DPE1N	AU39	LVDS_EG_A_DATA_N<1>	OUT
TXOUT_L2P_DPE0P	AP35	LVDS_EG_A_DATA_P<2>	OUT
TXOUT_L2N_DPE0N	AR35	LVDS_EG_A_DATA_N<2>	OUT
TXOUT_L3P	AN36	NC_LVDS_EG_A_DATA_P<3>	
TXOUT_L3N	AP37	NC_LVDS_EG_A_DATA_N<3>	

OMIT: TXOUT_U1P_DPF1P, TXOUT_U1N_DPF1N

R8606 10K 5% 1/16W MF-LF 402

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V0_GPU_TS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_MLB SYNC_DATE=12/01/2010

PAGE TITLE: Whistler LVDS/DP/GPIO

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GPIOs

GPU_PCIE_TX_PWR	GP	GPU_PCIE_TX_PWR	MAKE_BASE=TRUE
GPU_GPIO_TX_DEEMP	GP	GPU_GPIO_TX_DEEMP	MAKE_BASE=TRUE
GPU_PCIE_GEN2	GP	GPU_PCIE_GEN2	MAKE_BASE=TRUE
GPU_SMB_DAT	GP	GPU_SMB_DAT	MAKE_BASE=TRUE
GPU_SMB_CLK	GP	GPU_SMB_CLK	MAKE_BASE=TRUE
GPU_AC_BATT	GP	GPU_AC_BATT	MAKE_BASE=TRUE
GPU_VCORE_VID0	GP	GPU_VCORE_VID0	MAKE_BASE=TRUE
EG_BKLT_EN	GP	EG_BKLT_EN	MAKE_BASE=TRUE
GPU_ROM_SO	GP	GPU_ROM_SO	MAKE_BASE=TRUE
GPU_ROM_SI	GP	GPU_ROM_SI	MAKE_BASE=TRUE
GPU_ROM_SCLK	GP	GPU_ROM_SCLK	MAKE_BASE=TRUE
GPU_CONFIG_0	GP	GPU_CONFIG_0	MAKE_BASE=TRUE
GPU_CONFIG_1	GP	GPU_CONFIG_1	MAKE_BASE=TRUE
GPU_CONFIG_2	GP	GPU_CONFIG_2	MAKE_BASE=TRUE
DP_T29SNK0_HPD_GPU	GP	DP_T29SNK0_HPD_GPU	MAKE_BASE=TRUE
GPU_VCORE_VID1	GP	GPU_VCORE_VID1	MAKE_BASE=TRUE

GPIOs

GPU_VCORE_VID2	GP	GPU_VCORE_VID2	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_R_L	GP	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE
DP_T29SNK1_HPD_GPU	GP	DP_T29SNK1_HPD_GPU	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP_R_L	GP	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE
GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE
FBVDD_ALTVO	GP	FBVDD_ALTVO	MAKE_BASE=TRUE
GPU_ROM_CS_L	GP	GPU_ROM_CS_L	MAKE_BASE=TRUE
PEX_CLKREQ_L_R	GP	PEX_CLKREQ_L_R	MAKE_BASE=TRUE
NC_GPU_GENERICA	GP	NC_GPU_GENERICA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICB	GP	NC_GPU_GENERICB	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICC	GP	NC_GPU_GENERICC	MAKE_BASE=TRUE NO_TEST=TRUE
DP_CA_DET_EG_R	GP	DP_CA_DET_EG_R	MAKE_BASE=TRUE
NC_GPU_GENERICE	GP	NC_GPU_GENERICE	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICF	GP	NC_GPU_GENERICF	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICG	GP	NC_GPU_GENERICG	MAKE_BASE=TRUE NO_TEST=TRUE
DP_EG_HPD	GP	DP_EG_HPD	MAKE_BASE=TRUE

T29 HPD GPU isolation

PP3V3_S0 — C8741 0.1UF 20% 10V CERM 402

DP_T29SNK0_HPD → CRITICAL U8741 74LVC2G08GT SOT833 → DP_T29SNK0_HPD_GPU

PP3V3_GPU_VDD33_R — R8741 0 5% 1/16W MF-LF 402 — PP3V3_S0GPU

PP3V3_S0 — U8741 74LVC2G08GT SOT833

DP_T29SNK1_HPD → U8741 → DP_T29SNK1_HPD_GPU

Unused signals

TP_GPU_JTAG_TCK	MAKE_BASE=TRUE	TP_GPU_JTAG_TCK	
TP_GPU_JTAG_TDI	MAKE_BASE=TRUE	TP_GPU_JTAG_TDI	
TP_GPU_JTAG_TDO	MAKE_BASE=TRUE	TP_GPU_JTAG_TDO	
TP_GPU_JTAG_TMS	MAKE_BASE=TRUE	TP_GPU_JTAG_TMS	
TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE	TP_GPU_JTAG_TRST_L	
NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_CLK_P	
NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_CLK_N	
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_A_DATA_P<3>	
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_A_DATA_N<3>	
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_DATA_P<3>	
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_DATA_N<3>	

Config Straps

PP3V3_S0GPU

NOSTUFF R8700 10K 5% 1/16W MF-LF 402 — GPU_PCIE_TX_PWR
NOSTUFF R8701 10K 5% 1/16W MF-LF 402 — GPU_GPIO_TX_DEEMP
R8702 10K 5% 1/16W MF-LF 402 — GPU_PCIE_GEN2

NOSTUFF R8703 10K 5% 1/16W MF-LF 402 — GPU_SMB_DAT
NOSTUFF R8704 10K 5% 1/16W MF-LF 402 — GPU_SMB_CLK
NOSTUFF R8705 10K 5% 1/16W MF-LF 402 — GPU_AC_BATT

NOSTUFF R8706 10K 5% 1/16W MF-LF 402 — EG_BKLT_EN
NOSTUFF R8707 10K 5% 1/16W MF-LF 402 — GPU_ROM_SO
NOSTUFF R8708 10K 5% 1/16W MF-LF 402 — GPU_ROM_SI

NOSTUFF R8709 10K 5% 1/16W MF-LF 402 — GPU_ROM_SCLK
R8710 10K 5% 1/16W MF-LF 402 — GPU_CONFIG_0
NOSTUFF R8711 10K 5% 1/16W MF-LF 402 — GPU_CONFIG_1

GPU_ROM:YES NOSTUFF R8712 10K 5% 1/16W MF-LF 402 — GPU_CONFIG_2
NOSTUFF R8713 10K 5% 1/16W MF-LF 402 — FBVDD_ALTVO
NOSTUFF R8714 10K 5% 1/16W MF-LF 402 — PEX_CLKREQ_L_R

PP3V3_S0GPU

GPU_ROM:YES R8723 33 5% 1/16W MF-LF 402 — GPU_ROM_SI
GPU_ROM:YES R8724 33 5% 1/16W MF-LF 402 — GPU_ROM_SCLK
GPU_ROM:YES R8725 33 5% 1/16W MF-LF 402 — GPU_ROM_CS_L

GPU_ROM:YES R8720 10K 5% 1/16W MF-LF 402 — GPU_ROM_SI_R
GPU_ROM:YES R8721 0 5% 1/16W MF-LF 402 — GPU_ROM_CS_L_R
NO STUFF R8722 0 5% 1/16W MF-LF 402 — GPU_ROM_WP_L

C8721 0.1UF 20% 10V CERM 402 — GPU_ROM:YES

U8701 M25P10A UFDFPN8 CRITICAL OMIT_TABLE
VCC, S*, W*, HOLD*, VSS, THRM PAD
GPU_ROM_SI_R → D; GPU_ROM_SCLK_R → C; GPU_ROM_CS_L_R → S*; GPU_ROM_WP_L → W*; Q → GPU_ROM_SO_R

R8726 33 5% 1/16W MF-LF 402 — GPU_ROM_SO_R → GPU_ROM_SO — GPU_ROM:YES

PP3V3_S0

PP3V3_S0GPU

NO STUFF R8750 2.2K 5% 1/16W MF-LF 402 — DP_EG_DDC_CLK
NO STUFF R8751 2.2K 5% 1/16W MF-LF 402 — DP_EG_DDC_DATA
R8752 4.7K 5% 1/16W MF-LF 402 — DP_IG_DDC_CLK
R8753 4.7K 5% 1/16W MF-LF 402 — DP_IG_DDC_DATA

PP3V3_S0GPU

NO STUFF R8796 2.2K 5% 1/16W MF-LF 402
R8797 2.2K 5% 1/16W MF-LF 402

SMC_GFX_OVERTEMP_R_L → R8798 0 5% 1/16W MF-LF 402 → SMC_GFX_OVERTEMP_L
SMC_GFX_THROTTLE_R_L → R8799 0 5% 1/16W MF-LF 402 → SMC_GFX_THROTTLE_L

EG_LCD_PWR_EN
EG_BKLT_EN
FBVDD_ALTVO

R8792 10K 5% 1/16W MF-LF 402
R8793 10K 5% 1/16W MF-LF 402
R8794 10K 5% 1/16W MF-LF 402

ISOLATION R's for GPU Int Temp Sense

NOSTUFF
GPU_SMB_DAT — R8780 0 5% 1/16W MF-LF 402 — SMBUS_SMC_0_S0_SDA
GPU_SMB_CLK — R8781 0 5% 1/16W MF-LF 402 NOSTUFF — SMBUS_SMC_0_S0_SCL

PP3V3_S0GPU

L8703 120OHM-0.3A 0402 — PP3V3_GPU_OSC_27M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)
L8702 120OHM-0.3A 0402 — PP3V3_GPU_OSC_100M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C8702 0.1UF 10% 16V X5R 402-1
C8703 0.1UF 10% 16V X5R 402-1

GPU Reference Clocks

U8700 SL16010DC DFN
VDD1, VDD2, XIN/CLKIN, XOUT, SSCLK, REFCLK, SSEL0, SSEL1, VSS1, VSS2, THM PAD

GPU_OSC_27M_XTALIN, GPU_OSC_27M_XTALOUT
CRITICAL Y8700 SM-2.5X2.0MM 27MHZ-15PPM-18PF
C8700 30PF 5% 50V CERM 402
C8701 30PF 5% 50V CERM 402

R8730 0 5% 1/16W MF-LF 402 — GPU_CLK100M_R → GPU_CLK100M (OUT)
R8731 0 5% 1/16W MF-LF 402 — GPU_CLK27M_R → GPU_CLK27M (OUT)

SYNC_MASTER=K92_MLB SYNC_DATE=11/23/2010

PAGE TITLE: Whistler GPIOs & STRAPs

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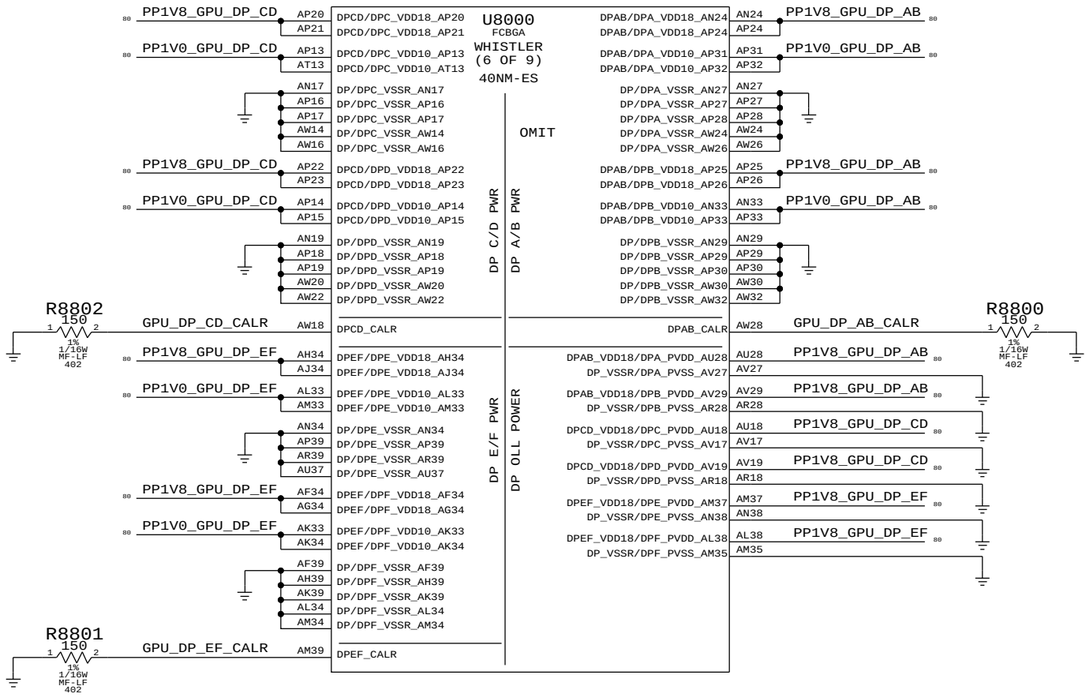

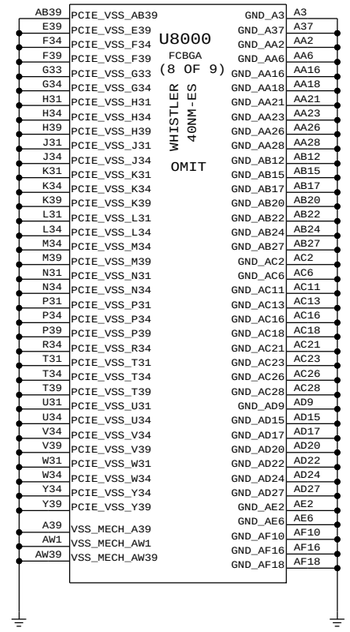

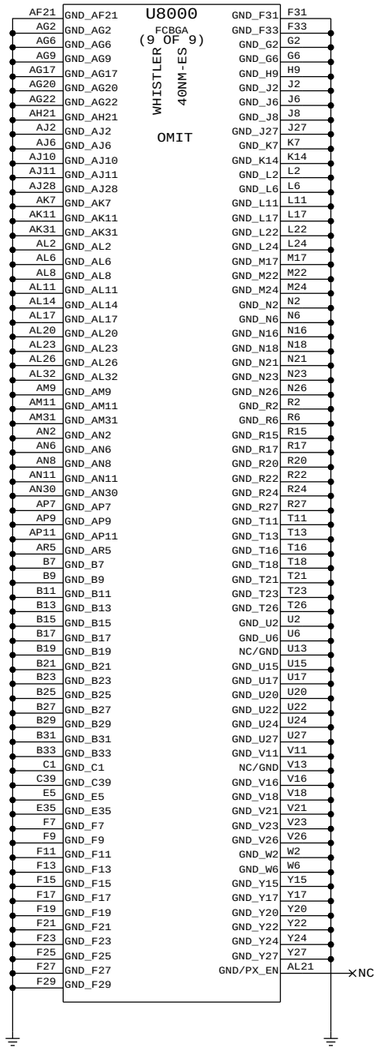

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE
Whistler DP PWR/GNDs

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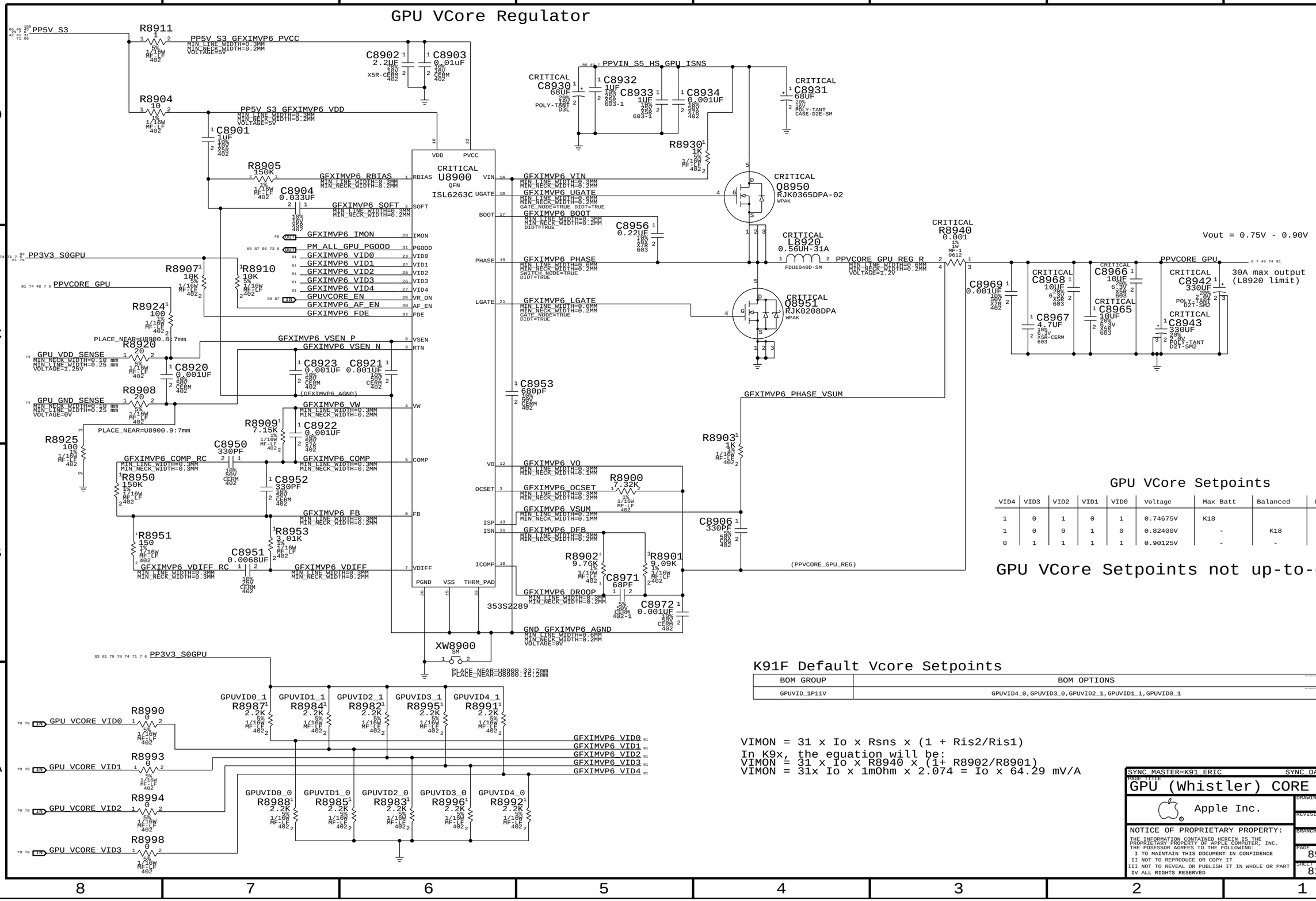
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K91F Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

VIMON = 31 x Io x Rsns x (1 + Ris2/Ris1)
In K9x, the eqaution will be:
VIMON = 31 x Io x R8940 x (1+ R8902/R8901)
VIMON = 31x Io x 1mOhm x 2.074 = Io x 64.29 mV/A

SYNC_MASTER=K91_ERIC SYNC_DATE=12/21/2010

PAGE TITLE
GPU (Whistler) CORE SUPPLY

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LCD (LVDS) INTERFACE

87 LCD_PWR_EN

R9094 10K 5% 1/16W MF-LF 402

CRITICAL U9000 FPF1009 MFET-2X2

PP3V3_S5

C9009 0.1UF 10% 16V X5R 402-1

C9011 0.1UF 10% 16V X5R 402-1

C9012 10UF 20% 6.3V X5R 603

CRITICAL L9000 FERR-250-OHM SM

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

C9001 0.1UF 10% 16V X5R 402-1

C9002 0.001UF 10% 50V X7R 402

CRITICAL J9000 20474-040E-11 F-RT-SM

PP3V3_S0

100K pull-ups are for
no-panel case (development).
Panel has 2K pull-ups

R9010 100K 5% 1/16W MF-LF 402

R9011 100K 5% 1/16W MF-LF 402

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

83 6 LVDS_DDC_CLK

83 6 LVDS_DDC_DATA

C9010 0.001UF 10% 50V X7R 402

97 83 6 LVDS_CONN_A_DATA_N<0>

97 83 6 LVDS_CONN_A_DATA_P<0>

97 83 6 LVDS_CONN_A_DATA_N<1>

97 83 6 LVDS_CONN_A_DATA_P<1>

97 83 6 LVDS_CONN_A_DATA_N<2>

97 83 6 LVDS_CONN_A_DATA_P<2>

CRITICAL L9010 90-OHM-100MA DLP11S SYM_VER_1

97 83 LVDS_CONN_A_CLK_N

97 83 LVDS_CONN_A_CLK_P

Place close to the connector

97 6 LVDS_CONN_A_CLK_F_N

97 6 LVDS_CONN_A_CLK_F_P

97 83 6 LVDS_CONN_B_DATA_N<0>

97 83 6 LVDS_CONN_B_DATA_P<0>

97 83 6 LVDS_CONN_B_DATA_N<1>

97 83 6 LVDS_CONN_B_DATA_P<1>

97 83 6 LVDS_CONN_B_DATA_N<2>

97 83 6 LVDS_CONN_B_DATA_P<2>

CRITICAL L9011 90-OHM-100MA DLP11S SYM_VER_1

97 83 LVDS_CONN_B_CLK_N

97 83 LVDS_CONN_B_CLK_P

Place close to the connector

97 6 LVDS_CONN_B_CLK_F_N

97 6 LVDS_CONN_B_CLK_F_P

88 6 LED_RETURN_6

88 6 LED_RETURN_5

88 6 LED_RETURN_4

88 6 LED_RETURN_3

88 6 LED_RETURN_2

88 6 LED_RETURN_1

NC

100 88 8 6 PPVOUT_S0_LCDBKLT

C9000 0.001UF 10% 50V CERM 402

518S0651

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

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LVDS Display Connector

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LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACE_NEAR=U9600.A6:7mm
R9220 357 1% 1/20W MF 201
LVDS_A_CLK_P → LVDS_CONN_A_CLK_P

PLACE_NEAR=U9600.A7:7mm
R9222 357 1% 1/20W MF 201
LVDS_A_CLK_N → LVDS_CONN_A_CLK_N

R9225 357 1% 1/20W MF 201
LVDS_A_DATA_P<0> → LVDS_CONN_A_DATA_P<0>
PLACE_NEAR=U9600.A8:7mm

PLACE_NEAR=U9600.B9:7mm
R9227 357 1% 1/20W MF 201
LVDS_A_DATA_N<0> → LVDS_CONN_A_DATA_N<0>

R9230 357 1% 1/20W MF 201
LVDS_A_DATA_P<1> → LVDS_CONN_A_DATA_P<1>
PLACE_NEAR=U9600.A9:7mm

PLACE_NEAR=U9600.C10:7mm
R9232 357 1% 1/20W MF 201
LVDS_A_DATA_N<1> → LVDS_CONN_A_DATA_N<1>

R9235 357 1% 1/20W MF 201
LVDS_A_DATA_P<2> → LVDS_CONN_A_DATA_P<2>
PLACE_NEAR=U9600.B10:7mm

PLACE_NEAR=U9600.A10:7mm
R9237 357 1% 1/20W MF 201
LVDS_A_DATA_N<2> → LVDS_CONN_A_DATA_N<2>

R9240 357 1% 1/20W MF 201
LVDS_B_CLK_P → LVDS_CONN_B_CLK_P
PLACE_NEAR=U9600.C8:7mm

PLACE_NEAR=U9600.C9:7mm
R9242 357 1% 1/20W MF 201
LVDS_B_CLK_N → LVDS_CONN_B_CLK_N

R9245 357 1% 1/20W MF 201
LVDS_B_DATA_P<0> → LVDS_CONN_B_DATA_P<0>
PLACE_NEAR=U9600.A2:7mm

PLACE_NEAR=U9600.A3:7mm
R9247 357 1% 1/20W MF 201
LVDS_B_DATA_N<0> → LVDS_CONN_B_DATA_N<0>

R9250 357 1% 1/20W MF 201
LVDS_B_DATA_P<1> → LVDS_CONN_B_DATA_P<1>
PLACE_NEAR=U9600.A1:7mm

PLACE_NEAR=U9600.B3:7mm
R9252 357 1% 1/20W MF 201
LVDS_B_DATA_N<1> → LVDS_CONN_B_DATA_N<1>

R9255 357 1% 1/20W MF 201
LVDS_B_DATA_P<2> → LVDS_CONN_B_DATA_P<2>
PLACE_NEAR=U9600.C5:7mm

R9257 357 1% 1/20W MF 201
LVDS_B_DATA_N<2> → LVDS_CONN_B_DATA_N<2>
PLACE_NEAR=U9600.A5:7mm

DP AUX, DDC, & HPD muxing to IG/EG

PP3V3_S0
R9202 10K 5% 1/10W MF-LF 402
C9220 0.1UF 20% 16V X5R CERM 402
C9230 0.1UF 20% 16V X5R CERM 402

U9220 CBTL03062 BGA (CRITICAL)
VDD, GND

DP_IG_AUX_CH_P → DAUX1+
DP_IG_AUX_CH_N → DAUX1-
DP_EG_AUXCH_P → DAUX2+
DP_EG_AUXCH_N → DAUX2-
DP_IG_DDC_CLK → DDC_CLK1
DP_IG_DDC_DATA → DDC_DAT1
DP_EG_DDC_CLK → DDC_CLK2
DP_EG_DDC_DATA → DDC_DAT2
DP_IG_HPD → HPD_1
DP_EG_HPD → HPD_2
DP_MUX_SEL_EG → GPU_SEL
DP_MUX_EN → XSD*

AUX+ → DP_EXTA_AUXCH_C_P
AUX- → DP_EXTA_AUXCH_C_N
DDC_CLK → DP_EXTA_DDC_CLK
DDC_DAT → DP_EXTA_DDC_DATA
HPDIN ← (DP_EXTA_HPD)

R9204 100K 5% 1/10W MF-LF 402
R9205 100K 5% 1/10W MF-LF 402

T29/DP HOT PLUG IN

T29_DP_HPD:MUX_GMUX
R9206 0 5% 1/10W MF-LF 402
DP_EXTA_HPD

PP3V3_S0
T29_DP_HPD:ALL_OR
C9210 0.1UF 20% 16V X5R CERM 402
CRITICAL
U9210 74LVC2G32GT SOT833
DP_T29SNK0_HPD
DP_T29SNK1_HPD
T29_HOTPLUG_DET_OR

U9210 74LVC2G32GT SOT833
(DP_EXTA_HPD)
DP_HOTPLUG_DET

T29_DP_HPD:MCU_GMUX
Q9280 SSM3K15FV SOT-VESM-MF
R9281 100K 5% 1/10W MF-LF 402
DP_A_EXT_HPD

LVDS DDC MUX

PP3V3_S0GPU
PP3V3_S0
C9270 0.1UF 10% 16V CERM 402
R9270 20K 5% 1/10W MF-LF 402
R9271 20K 5% 1/10W MF-LF 402
R9272 20K 5% 1/10W MF-LF 402
R9273 20K 5% 1/10W MF-LF 402

U9270 SN74LV4066A QFN1 (CRITICAL)
VCC, GND_THRM

LVDS_DDC_SEL_EG → C1
LVDS_DDC_SEL_IG → C2
C3
C4

A1/B1 ↔ LVDS_EG_DDC_CLK
A2/B2 ↔ LVDS_IG_DDC_CLK / LVDS_DDC_CLK
A3/B3 ↔ LVDS_EG_DDC_DATA
A4/B4 ↔ LVDS_IG_DDC_DATA / LVDS_DDC_DATA

SYNC_MASTER=K92_MLB SYNC_DATE=11/21/2010

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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1uF → DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF → DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF → DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF → DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF → DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF → DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF → DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1uF → DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF → DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF → DP_EXTA_AUXCH_N

PP3V3_S0 → R9309 1M 5% MF-LF 1/16W 402 → DP_EXTA_AUXCH_P
PP3V3_S0 → R9308 1M 5% MF-LF 1/16W 402 → DP_EXTA_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29_D2R_N<0> → C9370 0.47uF → T29_D2R_C_N<0>
T29_D2R_P<0> → C9371 0.47uF → T29_D2R_C_P<0>
GND_VOID=TRUE (C9370/C9371)
T29_A_BIAS_R2D_P0

OVERSIZE_PAD=0.875 mm^2 (Both L's)
T29_R2D_C_N<0> → L9372 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_N<0> → C9372 0.47uF (C9372.2) GND_VOID=TRUE → T29_R2D_P<0> → R9372 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE
T29_R2D_C_P<0> → L9373 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_P<0> → C9373 0.47uF (C9373.2) GND_VOID=TRUE → T29_R2D_N<0> → R9373 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE
Inductor values TBD

T29_A_BIAS_R2D_N0

T29 signals are P/N-swapped after AC caps to improve layout.

T29 Path Biasing

T29_D2R_N<1> → C9380 0.47uF → T29_D2R_C_N<1>
T29_D2R_P<1> → C9381 0.47uF → T29_D2R_C_P<1>
GND_VOID=TRUE (C9380/C9381)
T29_A_BIAS_R2D_P1

OVERSIZE_PAD=0.875 mm^2 (Both L's)
T29_R2D_C_N<1> → L9382 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_N<1> → C9382 0.47uF (C9383.2) GND_VOID=TRUE → T29_R2D_P<1> → R9382 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE
T29_R2D_C_P<1> → L9383 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_P<1> → C9383 0.47uF (C9383.2) GND_VOID=TRUE → T29_R2D_N<1> → R9383 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE
Inductor values TBD

T29_A_BIAS_R2D_N1

T29_D2R_C_P<0> → T29_D2R_P<0>
T29_D2R_C_N<0> → T29_D2R_N<0>
T29_D2R_C_P<1> → T29_D2R_P<1>
T29_D2R_C_N<1> → T29_D2R_N<1>

D9364 BAR90-02LRH (D9364.2) GND_VOID=TRUE
D9372 BAR90-02LRH
D9373 BAR90-02LRH
D9365 BAR90-02LRH
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY

T29: TX_0
T29DPA_ML_C_P<0> → T29DPA_ML_P<0>
T29DPA_ML_C_N<0> → T29DPA_ML_N<0>
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K → GND_VOID=TRUE
R9375 1.5K → GND_VOID=TRUE

D9360 BAR90-02LRH (D9360.2) GND_VOID=TRUE
D9382 BAR90-02LRH
D9383 BAR90-02LRH
D9361 BAR90-02LRH
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)

T29: TX_1
T29DPA_ML_C_P<2> → T29DPA_ML_P<2>
T29DPA_ML_C_N<2> → T29DPA_ML_N<2>
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K → GND_VOID=TRUE
R9385 1.5K → GND_VOID=TRUE

DP Path Biasing

DP A Super-Driver

PP3V3_S0 → C9310 2.2UF 20% 6.3V CERM 402-LF; C9311 0.1UF 20% 10V CERM 402; C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K; R9310 1K; R9312 1K

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	1 IN_D0P	OUT_D0P 30	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	2 IN_D0N	OUT_D0N 29	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	4 IN_D1P	OUT_D1P 28	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	5 IN_D1N	OUT_D1N 27	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	7 IN_D2P	OUT_D2P 25	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	8 IN_D2N	OUT_D2N 24	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	9 IN_D3P	OUT_D3P 23	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	10 IN_D3N	OUT_D3N 22	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	14 IN_SCL	AC_AUXP 20	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	13 IN_SDA	AC_AUXN 19	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	16 IN_AUXP	OUT_AUXP_SCL	18 (DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	15 IN_AUXN	OUT_AUXN_SDA	17 (DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	3 IN_HPD	(IPD) OUT_HPD	31 (DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	26 I2C_CTL_EN (IPU)	CA_DET	32 DP_A_CA_DET
DPSDRVA_I2C_ADDR0	36 I2C_ADDR0 (IPD)	CEXT	11 DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	35 I2C_ADDR1 (IPD)		
I2C_DPSDRVA_SCL	38 SCL_CTL		
I2C_DPSDRVA_SDA	37 SDA_CTL		
DPSDRVA_REXT	12 REXT		
DP_AUXCH_ISOL	39 AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	34 PD (IPD)		

C9319 2.2UF 20% 6.3V CERM 402-LF PLACE_NEAR=U9310.11:2 mm

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

SDRV_PD R9318 0 5% 1/16W MF-LF 402; R9319 4.99K 1% 1/16W MF-LF 402

R9354 30 5% 1/20W MF 201; R9353 270 5% 1/20W MF 201
R9355 30 5% 1/20W MF 201
R9350 30 5% 1/20W MF 201
R9351 30 5% 1/20W MF 201; R9352 270 5% 1/20W MF 201

DP_SDRVA_ML_R_P<0> → C9364 0.22uF → DP_SDRVA_ML_P<0>
DP_SDRVA_ML_R_N<0> → C9365 0.22uF → DP_SDRVA_ML_N<0>
DP_SDRVA_ML_R_P<2> → C9360 0.22uF → DP_SDRVA_ML_P<2>
DP_SDRVA_ML_R_N<2> → C9361 0.22uF → DP_SDRVA_ML_N<2>

C9363 0.1uF; C9362 0.1uF
C9367 0.1uF; C9366 0.1uF
C9369 0.1uF; C9368 0.1uF

AUXCH Snoop Port, used by PS8301 during training.

PP3V3_S0 → C9359 0.1uF
DP_A_PWRDWN → CRITICAL U9359 74LVC1G04DBDCK SC70 → DP_A_BIAS

IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

DP_A_BIAS0 VOLTAGE=3.3V → R9362 51 5% 1/20W MF 201 PLACE_NEAR=C9361.1:2mm
DP_A_BIAS2 VOLTAGE=3.3V → R9363 51 5% 1/20W MF 201 PLACE_NEAR=C9361.1:2mm

R9361 1.5K; R9360 1.5K; R9365 1.5K; R9364 1.5K

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

C9390 0.1uF; C9391 0.1uF

U9390 CBTL04DP081 HVQFN

DP_SDRVA_ML_N<3>	31 DIN1_0+	DOUT_0+ 1	T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	30 DIN1_0-	DOUT_0- 2	T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	27 DIN1_1+		T29: Unused
DP_SDRVA_ML_P<1>	26 DIN1_1-	DOUT_1+ 4	T29DPA_ML_N<1>
DP_SDRVA_AUXCH_P	19 AUX1+	DOUT_1- 5	T29DPA_ML_P<1>
DP_SDRVA_AUXCH_N	18 AUX1-		T29: LSX_A_R2P/P2R (P/N)
DP_SDRVA_HPD	17 HPD_1	AUX+ 6	DP_A_EXT_AUXCH_P
CKPLUS_WAIVE=NdifPr_badTerm		AUX- 7	DP_A_EXT_AUXCH_N
T29_A_RSVD_N	25 DIN2_0+		T29: RX_1 Bias Sink
T29_A_RSVD_P	24 DIN2_0-	HPD_IN 8	DP_A_EXT_HPD
(T29_A_LSX_P2R)	23 DIN2_1+		
(T29_A_LSX_R2P)	22 DIN2_1-		
T29_D2R1_BIASP	15 AUX2+		
T29_D2R1_BIASN	14 AUX2-		
	13 HPD_2		
	CRITICAL		

R9399 100K 5% 1/16W MF-LF 402

R9396 1K; R9397 1K; R9398 100K

NC
DP_A_PWRDWN → GPU_SEL 10
T29_A_BIAS → AUX_SEL 32
NC 11
LO=Port A HI=Port B
OMIT_TABLE

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 11 for HPD.

THMPAD GND
SIGNAL_MODEL=T29DP_MUX

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100 ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

C9330 0.1uF; C9331 0.1uF

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_A_CA_DET	1 RESET#/PIO0_0	R/PIO1_0/AD1 16	T29DPA_CONFIG1_RC
	2 PIO0_1/CLKOUT	R/PIO1_1/AD2 17	T29DPA_CONFIG2_RC
T29_LSEO<0>	7 PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18	T29_A_HV_EN_R
I2C_T29_SCL	8 PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19	T29_A_UC_ADDR
I2C_T29_SDA	9 PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20	DP_A_EXT_HPD
T29DPA_HPD	10 PIO0_6/SCK	PIO1_6/RXD 23	T29_A_LSX_P2R
T29_A_BIAS	11 PIO0_7/CTS#	PIO1_7/TXD 24	T29_A_LSX_R2P
T29_LSOE<0>	12 PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6	T29_LSEO<1>
T29_LSOE<1>	13 PIO0_9/MOSI/CT16B0_MAT1		
	14 SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
T29_MCU_INT_L	15 R/PIO0_11/AD0 (OD)	XTALIN 4	
	VSS 3	THRM PAD 25	

R9338 10K; R9334 10K
T29_A_HV_EN → R9339 1M

P2R = Plug to Receptacle
R2P = Receptacle to Plug

I2C Addr: 0x26/0x27 (Wr/Rd)

R9335 1K; R9336 10K

R9392 51; R9393 51

=T29_WAKE_L: use PCIe WAKE#
PCIE_WAKE_L → OMIT R9330 0 → SWCLK / SWDIO
T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

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Port A HV Power Switch

3.3V/HV Power MUX

Port A 3.3V Power Switch

DisplayPort/T29 A Connector

PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP15V_T29
20V Max

R9416 470K 5% 1/10W MF-LF 402

C9410 0.1UF 10% 50V X7R 603-1

U9410 SN1010017 QFN
VIN VOUT EN* (IPU-Weak!) FLT* RTRY* ILIM CT IFLT GND THRM PAD

C9411 0.1UF 10% 50V X7R 603-1

PPHV_SW_DPAPWR

D9410 SM STPS2L30AF

TP_DPAPWRSW_FLT_L

DPAPWRSW_ILIM

DPAPWRSW_IFLT

DPAPWRSW_HVEN_L_R

DPAPWRSW_CT

C9412 0.47UF 10% 16V CERM-X5R 402
OMIT_TABLE
<CT>

R9410 100K 5% 1/10W MF-LF 402
R9411 210K 1% 1/10W MF-LF 402
<RFLT> <RLIM>

(*) U9410 tolerance unknown

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

Q9415 SSM3K15FV SOD-VESM-HF

Bleeder Resistor
2.5V / 249 ohm = 10mA
R9419 249 1% 1/10W MF-LF 402 P = ~27mW

Q9419 DMB53D0UV SOT-563
DPAPWR_BLDR_B
DPAPWR_BLDR_E
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

T29_A_HV_EN

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL D9425 POWERDI-123 DFLS1100

CRITICAL Q9425 SI8409DB 8A

3.3V/HV MUXed

3.3V Always

Blocking FET, off when Source >3.4V or HV_EN high.

R9427 100K 1% 1/10W MF-LF 402
R9428 21.5K 1% 1/10W MF-LF 402
R9425 4.7K 5% 1/10W MF-LF 402
R9426 1K 5% 1/16W MF-LF 402
R9430 4.7K 5% 1/16W MF-LF 402

DPAPWRSW_VREF
DPAPWRSW_P3V3_ON_L
DPAPWRSW_HV_DET_R_L

CRITICAL U9426 ZXRE060A SOT353 IN OUT GND PGND FB

R9429 4.7K 5% 1/10W MF-LF 402
C9424 0.47UF 10% 6.3V CERM-X5R 402
C9426 0.1UF 20% 10V CERM 402
C9429 0.1UF 20% 10V CERM 402
R9424 22 5% 1/10W MF-LF 402
NO STUFF
DPAPWRSW_ON_L_C
DPAPWRSW_HV_DET_L

Q9426 MMDT3946XG SOT363

DPAPWRSW_NPN_E

R9418 1K 5% 1/10W MF-LF 402
DPAPWRSW_HV_DET

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

CRITICAL U9480 TPS2051B SOT23 OUT IN OC* EN GND

T29_A_HV_EN
SMC_S4_WAKESRC_EN

DP_PWR must be S4 to support wake from T29 devices.

PP3V3_S5

C9486 10UF 20% 6.3V X5R 603
C9485 0.1UF 20% 10V CERM 402
C9481 0.1UF 20% 10V CERM 402
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

T29_A_BIAS

CRITICAL U9435 ZXRE060A SOT353 IN OUT FB PGND GND

C9435 0.1UF 20% 10V CERM 402
C9436 1UF 10% 10V X5R 402

DPAPWRSW_P3V3_ON

Q9430 SSM6N37FEAPE SOT563
Q9430 SSM6N37FEAPE SOT563

DPAPWRSW_ON_C
T29_A_HV_EN

R9437 82 5% 1/10W MF-LF 402

T29_2V9_ENABLE
R9435 100K 1% 1/10W MF-LF 402
DPAPWR_FB_DIV
R9436 24.9K 1% 1/10W MF-LF 402

R9433 220 5% 1/16W MF-LF 402
R9432 10K 5% 1/16W MF-LF 402

L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

C9400 0.01UF 10% 50V X7R 402

PP3V3RHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

Circuit threshold range: 2.877-2.941V (2.903V nominal)

C9490 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=C9490.1:2mm
R9490 51 5% 1/20W MF 201
T29_A_BIAS_R
VOLTAGE=3.3V

T29_D2R_C_P<0>
T29_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

T29 Dir DP Dir

R9403 12 5% 1/16W MF-LF 402 GND_DPACONN_8
R9404 12 5% 1/16W MF-LF 402 GND_DPACONN_14

J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
2	HOT_PLUG_DETECT	GND 1
4	CONFIG1	ML_LANE0P 3
6	CONFIG2	ML_LANE0N 5
8	GND	GND 7
10	ML_LANE3P	ML_LANE1P 9
12	ML_LANE3N	ML_LANE1N 11
14	GND	GND 13
16	AUX_CHP	ML_LANE2P 15
18	AUX_CHN	ML_LANE2N 17
20	DP_PWR	RETURN 19
	SHIELD PINS	22 21

For J9400 T29 SMT pads (3, 5, 7, 8, 19):
GND_VOID=TRUE

GND_DPACONN_1 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
GND_DPACONN_7 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
GND_DPACONN_13 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
GND_DPACONN_19 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

OMIT_TABLE
R9405 12 5% 1/20W MF 201
R9406 12 5% 1/20W MF 201
R9407 12 5% 1/20W MF 201
R9408 12 5% 1/20W MF 201

DP Dir T29 Dir

T29: TX_0
T29DPA_ML_P<0> T29DPA_ML_N<0>

T29: TX_1
T29DPA_ML_P<2> T29DPA_ML_N<2>

T29: LSX_R2P/P2R (P/N)
T29DPA_ML_P<1> T29DPA_ML_N<1>

C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201
C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201

GND_VOID=TRUE (Both C's)

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

T29_A_BIAS_D2R_P1
T29_A_BIAS_D2R_N1

R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201

T29_D2R_C_P<1>
T29_D2R_C_N<1>

D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7

CRITICAL L9498 650NH-5%-0.430MA-0.052OHM 0603 SIGNAL_MODEL=EMPTY
CRITICAL L9499 650NH-5%-0.430MA-0.052OHM 0603 SIGNAL_MODEL=EMPTY
GND_VOID=TRUE
SIGNAL_MODEL=T29PIN
(Both L's)

T29DPA_D2R1_AUXCH_P
T29DPA_D2R1_AUXCH_N

DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N

R9402 12 5% 1/10W MF-LF 402 T29DPA_HPD_R

DPACONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V

R9401 12 5% 1/16W MF-LF 402

C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402
C9402 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402

T29: Unused

T29DPA_HPD

T29DPA_CONFIG1_RC

T29DPA_CONFIG2_RC

R9452 1M 5% 1/10W MF-LF 402
R9451 1M 5% 1/10W MF-LF 402
C9494 330PF 10% 50V CERM 402
C9495 330PF 10% 50V CERM 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/16W MF-LF 402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0 OHM,5,1/16W,0402,SMD,LF	C9412		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,XSR,0201,SMD	R9405		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,XSR,0201,SMD	R9406		

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

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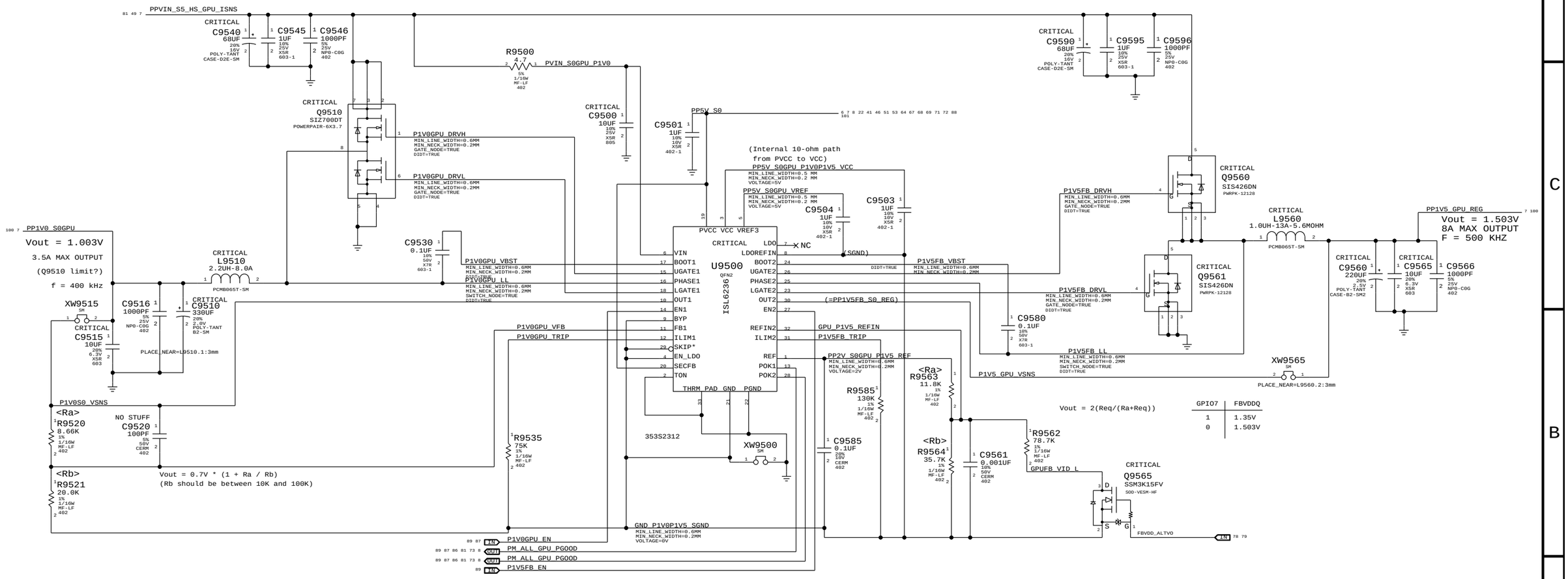

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GMUX CPLD

R9600 0 5% 1/16W MF-LF 402 — PP3V3_S0

C9610–C9629 0.1UF 20% 10V CERM 402 — PP3V3_S0_GMUX_R (MIN_LINE_WIDTH=0.4mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V)

R9610 0 5% 1/16W MF-LF 402 — PP1V8_S0

C9611–C9617 0.1UF 20% 10V CERM 402 — PP1V8_S0_GMUX_R (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=1.8V)

C9600 4.7UF 20% 6.3V X5R-1 402; C9604–C9609 0.1UF 20% 10V CERM 402 — PP1V2_S0

R9645 10K 1% 1/20W MF 201 — PP3V3_S0

R9640 10K 1% 1/20W MF 201 — PP3V3_S0

NO STUFF R9646 10K 1% 1/20W MF 201

NO STUFF R9641 10K 1% 1/20W MF 201

CRITICAL
J9600
1909782
M-RT-SM
GMUX_JTAG_CONN

1	PP3V3_S0	
2	JTAG_GMUX_TDO	
3	JTAG_GMUX_TDI	87
4	JTAG_GMUX_TMS	18 87
5		
6	JTAG_ISP_TCK	8 19 23 33 87
7		
8		

NO STUFF R9647 10K 1% 1/20W MF 201

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

CRITICAL
U9600
XP25-5
CSBGA

	VCC	C4, J3, J13, N11, P8	
	VCCAUX	C11, J2, J14, M8	
	VCCIO6	B5	
	VCCIO1	B7	
	VCCIO2	A12, C14, F13	
	VCCIO3	M12	
	VCCIO4	M9	
	VCCIO5	M3	
	VCCIO6	N5	
	VCCIO7	M1	
	VCCJ	C3	
		F2	
		K12	
	ULC_VCCPLL	A4	
	LRC_VCCPLL	P11	

87 33 23 19 8	JTAG_ISP_TCK	K14	TCK
87	JTAG_GMUX_TDI	L13	TDI
87	JTAG_GMUX_TDO	K13	TDO
87 18	JTAG_GMUX_TMS	L12	TMS
	GMUX_TOE	K2	TOE
	GMUX_CFG0	K1	CFG0
88 8 OUT	LCD_BKLT_EN	P2	PB7A
88 87 6 OUT	LCD_BKLT_PWM	N2	PB7B
87 83 OUT	LVDS_DDC_SEL_EG	P4	PB14A
87 83 OUT	LVDS_DDC_SEL_IG	N4	PB14B
83 OUT	DP_MUX_EN	N3	PB15A (OD)
87 83 OUT	DP_MUX_SEL_EG	M4	PB15B
87 73 8 OUT	EG_RESET_L	P5	PB16A
89 87 71 OUT	P3V3GPU_EN	M5	PB16B
89 87 81 OUT	GPUVCORE_EN	P6	PB17A
89 87 86 OUT	P1V0GPU_EN	M6	PB17B
89 87 OUT	P1V5FB1V8GPU_R_EN	P7	PB18A
16 8 OUT	PEG_CLKREQ_L	M7	PB18B (OD)
79 OUT	DP_CA_DET_EG	N7	PB19A
87 82 OUT	LCD_PWR_EN	N8	PB19B
93 46 44 16 6 BI	LPC_AD<0>	P9	PB20A
93 46 44 16 6 BI	LPC_AD<1>	N9	PB20B
93 46 44 16 6 BI	LPC_AD<2>	P10	PB26A
93 46 44 16 6 BI	LPC_AD<3>	M10	PB26B
93 46 44 16 6 BI	LPC_FRAME_L	P12	PB27A
25 IN	LPCPLUS_RESET_L	P13	PB27B
25 IN	LPC_CLK33M_GMUX	N12	PB28A
19 OUT	GMUX_INT	P14	PB28B
92 87 18 IN	LVDS_IG_B_DATA_P<2>	B1	PL2A
92 87 18 IN	LVDS_IG_B_DATA_N<2>	B2	PL2B
	GMUX_PL6A	C2	PL6A
6	TP_GMUX_PL6B	D3	PL6B
92 87 18 IN	LVDS_IG_A_DATA_P<0>	D1	PL7A
92 87 18 IN	LVDS_IG_A_DATA_N<0>	E1	PL7B
92 87 18 IN	LVDS_IG_A_DATA_P<1>	D2	PL8A
92 87 18 IN	LVDS_IG_A_DATA_N<1>	E3	PL8B
92 87 18 IN	LVDS_IG_A_DATA_P<2>	F1	PL9A
92 87 18 IN	LVDS_IG_A_DATA_N<2>	G1	PL9B
92 87 18 IN	LVDS_IG_B_DATA_P<0>	F3	PL10A
92 87 18 IN	LVDS_IG_B_DATA_N<0>	G2	PL10B
92 87 18 IN	LVDS_IG_B_DATA_P<1>	H2	PL11A
92 87 18 IN	LVDS_IG_B_DATA_N<1>	G3	PL11B
92 87 18 IN	LVDS_IG_A_CLK_P	H1	PL12A
92 87 18 IN	LVDS_IG_A_CLK_N	H3	PL12B
6 OUT	TP_LVDS_MUX_SEL_EG	L1	PL14A
	TP_GMUX_PL14B	L3	PL14B
25 IN	GMUX_RESET_L	K3	PL15A
88 87 8	GMUX_VSYNC	L2	PL15B
89 86 81 73 8 IN	PM_ALL_GPU_PGOOD	N1	PL25A
79 8 IN	PEX_CLKREQ_L	P1	PL25B

BANK5 (PB7A–PB18B), BANK4 (PB20A–PB28B), BANK7 (PL2A–PL12B), BANK6 (PL14A–PL25B)

GND — GNDIO0, GNDIO1, GNDIO2, GNDIO3, GNDIO4, GNDIO5, GNDIO6, GNDIO7, ULC_GNDPLL, LRC_GNDPLL

PP3V3_S0_GMUX_ULC_VCCPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V) — L9621 FERR-220-OHM 0402 — C9631 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_LRC_VCCPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V) — L9620 FERR-220-OHM 0402 — C9630 0.1UF 20% 10V CERM 402

OMIT

PT7A	A2	LVDS_B_DATA_P<0>	OUT 83 97
PT7B	A3	LVDS_B_DATA_N<0>	OUT 83 97
PT8A	A1	LVDS_B_DATA_P<1>	OUT 83 97
PT8B	B3	LVDS_B_DATA_N<1>	OUT 83 97
PT9A	C5	LVDS_B_DATA_P<2>	OUT 83 97
PT9B	A5	LVDS_B_DATA_N<2>	OUT 83 97
PT14A	B6	EG_PWRSEQ_EN	IN 87
PT14B	C7	GMUX_DEBUG_RESET_L	IN 87
PT15A	A6	LVDS_A_CLK_P	OUT 83 97
PT15B	A7	LVDS_A_CLK_N	OUT 83 97
PT16A	C8	LVDS_B_CLK_P	OUT 83 97
PT16B	C9	LVDS_B_CLK_N	OUT 83 97
PT17A	A8	LVDS_A_DATA_P<0>	OUT 83 97
PT17B	B9	LVDS_A_DATA_N<0>	OUT 83 97
PT18A	A9	LVDS_A_DATA_P<1>	OUT 83 97
PT18B	C10	LVDS_A_DATA_N<1>	OUT 83 97
PT19A	B10	LVDS_A_DATA_P<2>	OUT 83 97
PT19B	A10	LVDS_A_DATA_N<2>	OUT 83 97
PT20A	A11	GND	
PT20B	B12	GND	
PT28A	B13	GND	
PT28B	A13	GND	
PR2A	A14	DP_A_CA_DET	IN 84
PR2B	B14	DP_HOTPLUG_DET	IN 83
PR6A	D12	LVDS_EG_A_DATA_P<0>	IN 78 87 97
PR6B	D13	LVDS_EG_A_DATA_N<0>	IN 78 87 97
PR7A	D14	LVDS_EG_A_DATA_P<1>	IN 78 87 97
PR7B	E14	LVDS_EG_A_DATA_N<1>	IN 78 87 97
PR8A	E12	LVDS_EG_A_DATA_P<2>	IN 78 87 97
PR8B	F12	LVDS_EG_A_DATA_N<2>	IN 78 87 97
PR9A	F14	LVDS_EG_B_DATA_P<0>	IN 78 87 97
PR9B	G14	LVDS_EG_B_DATA_N<0>	IN 78 87 97
PR10A	G12	LVDS_EG_B_DATA_P<1>	IN 78 87 97
PR10B	G13	LVDS_EG_B_DATA_N<1>	IN 78 87 97
PR11A	H13	LVDS_EG_B_DATA_P<2>	IN 78 87 97
PR11B	H12	LVDS_EG_B_DATA_N<2>	IN 78 87 97
PR12A	H14	LVDS_EG_A_CLK_P	IN 78 87 97
PR12B	J12	LVDS_EG_A_CLK_N	IN 78 87 97
PR14A	L14	LVDS_IG_PANEL_PWR	IN 8 18
PR14B	M13	EG_LCD_PWR_EN	IN 78 79
PR24A	N14	LVDS_IG_BKL_ON	IN 8 18
PR24B	N13	EG_BKLT_EN	IN 78 79

BANK1, BANK2, BANK3

PP3V3_S3 — R9676 100K 5% 1/20W MF 201 — GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563 — ALL_SYS_PWRGD

NO STUFF R9675 0 5% 1/10W MF-LF 2402 — GMUX_S3_PD_GND

PP3V3_S0 — NO STUFF R9670 10K 1% 1/20W MF 201 — GMUX_VSYNC

Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDI, JTAG_GMUX_TDO

R9605 1K 5% 1/20W MF 201 — PP3V3_T29 — T29_JTAG_FET

JTAG_ISP_TDI, JTAG_ISP_TDO

LVDS Receiver Termination

92 87 18	LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
92 87 18	LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>
92 87 18	LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
92 87 18	LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
92 87 18	LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
92 87 18	LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>
92 87 18	LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>
97 87 78	LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
97 87 78	LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
97 87 78	LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
97 87 78	LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.F12:5mm	LVDS_EG_A_DATA_N<2>
97 87 78	LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
97 87 78	LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
97 87 78	LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

Required Pullups

SIGNAL_MODEL=EMPTY — PP3V3_S0

87	EG_PWRSEQ_EN	R9684	1K	5% 1/20W MF 201
87	JTAG_GMUX_TDI	R9685	10K	5% 1/20W MF 201
87	JTAG_GMUX_TDO	R9686	10K	5% 1/20W MF 201
87	GMUX_DEBUG_RESET_L	R9680	1K	5% 1/20W MF 201

NO STUFF R9679 10K 1% 1/10W MF-LF 402 — SILK_PART=GMUX_RST

Required Pulldowns

87 83	DP_MUX_SEL_EG	R9681	10K	5% 1/20W MF 201
87 83	LVDS_DDC_SEL_IG	R9682	10K	5% 1/20W MF 201
87 83	LVDS_DDC_SEL_EG	R9683	10K	5% 1/20W MF 201
87 73 8	EG_RESET_L	R9691	100K	5% 1/20W MF 201
88 87 6	LCD_BKLT_PWM	R9693	100K	5% 1/20W MF 201

NO STUFF

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

R9674 4.7K 5% 1/20W MF 201 — P1V5FB1V8GPU_R_EN

R9673 4.7K 5% 1/20W MF 201 — P1V0GPU_EN

R9672 4.7K 5% 1/20W MF 201 — GPUVCORE_EN

R9671 4.7K 5% 1/20W MF 201 — P3V3GPU_EN

R9678 4.7K 5% 1/20W MF 201 — LCD_PWR_EN

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PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

CRITICAL
Q9706
FDC638APZ_SBMS001
SSOT6-HF

PPBUS_G3H
F9700
3AMP-32V-467
603-HF
BOTTOM
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

PPBUS_SW_LCDBKLT_PWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

R9788 301K 1% 1/16W MF-LF 402
C9782 0.1UF 10% 16V X5R 402
R9789 147K 1% 1/16W MF-LF 402
LCDBKLT_EN_DIV
LCDBKLT_EN_L

Q9707 SSM6N15FEAPE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
BKLT_PLT_RST_L

PP5V_S0
PPBUS_SW_BKL
PP3V3_S0

CRITICAL
L9701
33UH-1.8A-110MOHM
1217AS-2SM
PPBUS_SW_LCDBKLT_PWR_SW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=50V
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
D9701
SOD-123
RB160M-60G
PLACE_NEAR=L9701.2:3mm
PLACE_NEAR=U9701.A5:3mm

PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V

C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
C9710 10UF 10% 25V X5R 603-1
C9714 0.01UF 10% 25V X7R-CERM 402
C9711 0.1UF 10% 16V X5R 402
C9796 220PF 10% 50V X7R-CERM 402
C9797 10UF 10% 50V X5R 1210-1
C9799 10UF 10% 50V X5R 1210-1

PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=U9701.D1:5mm
PLACE_NEAR=U9701.D1:3mm
PLACE_NEAR=U9701.C4:4mm
PLACE_NEAR=D9701.2:5mm
PLACE_NEAR=D9701.2:3mm

XW9720
SM
PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
PLACE_NEAR=C9797.1:5mm

BKL_VSYNC_R
MIN_NECK_WIDTH=0.075 mm
NO STUFF
R9754 0 5% 1/16W MF-LF 402
R9755 10K 5% 1/16W MF-LF 402
NO STUFF
C9741 1UF 10% 6.3V X5R 402
GMUX_VSYNC
NO STUFF
C9740 10UF 20% 6.3V X5R 603
NO STUFF
R9740 47.0K 1% 1/16W MF-LF 402
R9741 10K 5% 1/16W MF-LF 402
MIN_NECK_WIDTH=0.075 mm

R9753 0 5% 1/16W MF-LF 402
SMBUS_PCH_CLK
R9757 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA
Addr: 0x58(Wr)/0x59(Rd)

PPBUS_SW_LCDBKLT_PWR
R9731 301K 1% 1/16W MF-LF 402
R9715 100K 1% 1/16W MF-LF 402
PLACE_SIDE=BOTTOM

R9704 33 5% 1/16W MF-LF 402
LCD_BKLT_PWM
C9704 33PF 5% 50V C0GM 402

U9701
25-BUMP-MICRO
LP8550
VDDIO VLDO VIN
VSYNC SW_0 SW_1 FB
FILTER ISET FSET SCLK SDA PWM EN FAULT
GND_S GND_L GND_SW GND_SW
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6

BKL_FLTR
BKL_ISET
BKL_FSET
BKL_SCL
BKL_SDA
BKL_PWM
BKL_EN
TP_BKL_FAULT
CRITICAL

BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6

R9716 90.9K 1% 1/16W MF-LF 402
R9714 16.2K 1% 1/16W MF-LF 402
I_LED=22.7mA
Fpwm=9.62kHz
see spec for others
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)
XW9710
SM
GND_BKL_SGND
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD
R9717 0 5% 1/16W MF-LF 402
LED_RETURN_1
R9718 0 5% 1/16W MF-LF 402
LED_RETURN_2
R9719 0 5% 1/16W MF-LF 402
LED_RETURN_3
R9720 0 5% 1/16W MF-LF 402
LED_RETURN_4
R9721 0 5% 1/16W MF-LF 402
LED_RETURN_5
R9722 0 5% 1/16W MF-LF 402
LED_RETURN_6

PLACE_NEAR=U9701.E5:10mm
PLACE_NEAR=U9701.D5:10mm
PLACE_NEAR=U9701.C5:10mm
PLACE_NEAR=U9701.E3:10mm
PLACE_NEAR=U9701.E2:10mm
PLACE_NEAR=U9701.E1:10mm
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
BOTTOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMT	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMT	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K901_KIRA SYNC_DATE=06/25/2010
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LCD Backlight Driver

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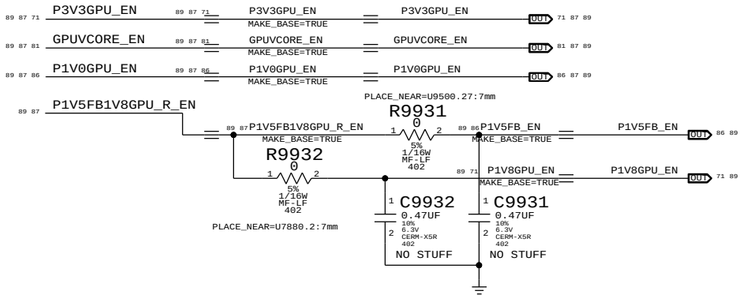
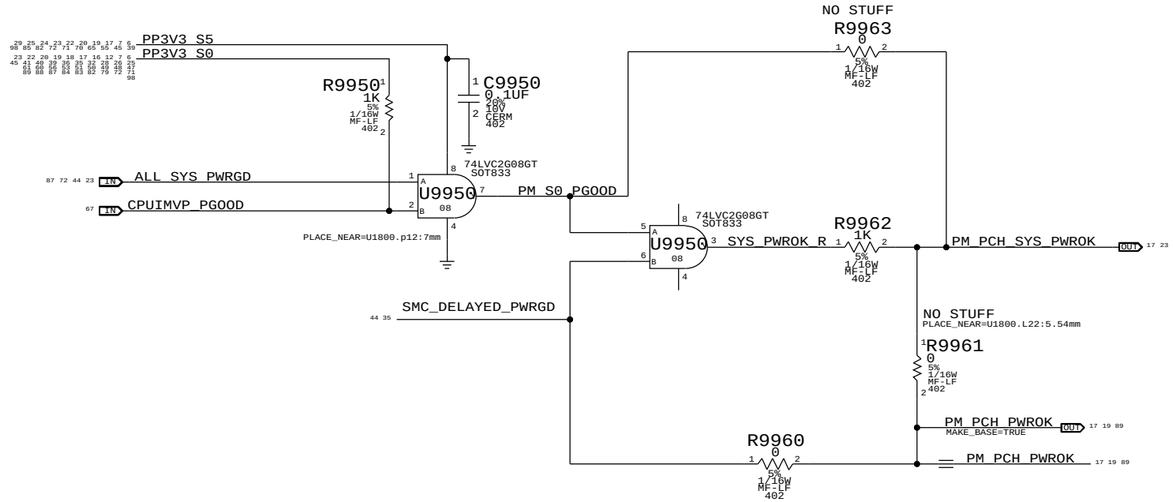
GPU Rail Sequencing

Whistler GPU requires rails to come up in the following order:

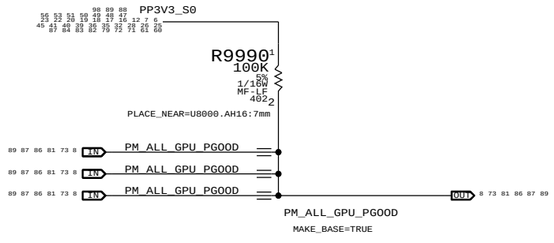
1) GPU_3.3V
2) GPUVcore
3) GPU_1.0V
4) GPU_1.8V;GDDR5 1.5/1.35V



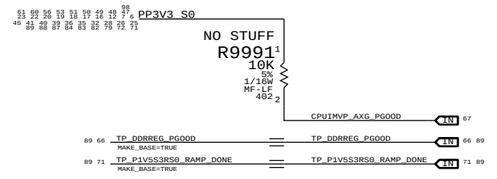
PCH S0 PWRGD



EXT GPU PWRGD Pullup



Unused PGOOD signal



SYNC_MASTER=K91_MARY SYNC_DATE=08/03/2010

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Power Sequencing EG/PCH S0

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	6 9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	6 9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	6 9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	CPU_50S	CPU_AGTL	FDI_INT	6 9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 44
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
XDP_BRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 67
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 67
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	73
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	73
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 73
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	73
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	73
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 67
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 67
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 67

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE: CPU Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 6 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 6 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 6 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 6 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 6 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 6 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 6 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 6 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 6 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 6 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 6 11 26 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 6 11 26 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 6 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 6 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 6 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 6 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 6 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 6 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 6 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 6 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 6 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 6 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 6 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 6 11 27 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 6 11 27 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 6 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 6 11 27

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 17 83
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 17 83
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3> 8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3> 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 87
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N 16 41
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_N 6 41
T21 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P 41
T21	SATA_90D	SATA	SATA_HDD_R2D_UF_N 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 16 41
	SATA_90D	SATA	SATA_HDD_D2R_N 16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N 16 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P 6 41
	SATA_90D	SATA	SATA_ODD_R2D_N 6 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 16 41
	SATA_90D	SATA	SATA_ODD_D2R_N 16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P 6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 6 41
T21 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 16
T21 PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P 18 24
	USB_85D	USB	USB_HUB1_UP_N 18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P 18 24
	USB_85D	USB	USB_HUB2_UP_N 18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P 24 42
	USB_85D	USB	USB_EXTA_N 24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P 24 42
	USB_85D	USB	USB_EXTB_N 24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P 8 24
	USB_85D	USB	USB_EXTC_N 8 24
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 31
	USB_85D	USB	USB_CAMERA_CONN_N 6 31
USB_BT	USB_85D	USB	USB_BT_P 24 31
	USB_85D	USB	USB_BT_N 24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P 24 52
	USB_85D	USB	USB_TPAD_N 24 52
USB_IR	USB_85D	USB	USB_IR_P 24 43
	USB_85D	USB	USB_IR_N 24 43
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 18
T21 USB_T29A	USB_85D	USB	USB_T29A_P 8 24
T21	USB_85D	USB	USB_T29A_N 8 24

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 44 46 87
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 44 46 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 25 46 87
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 44
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 46
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 23 26 28 30 41 47 61 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 23 26 28 30 41 47 61 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 47
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 47
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 47
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 47
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 56
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 56
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 56
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 56
	HDA_50S	HDA	AUD_SDI_R	56
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 56
	HDA_50S	HDA	HDA_SDOUT_R	16
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 46
	SPI_55S	SPI	SPI_CLK	46
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 46
	SPI_55S	SPI	SPI_MOSI	46
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 46
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 46
	SPI_55S	SPI	SPI_CS0_L	46
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 31
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 31
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 31
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 31
	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
T25	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
T24	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
T28	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33
T23	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
T27	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
T22	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
T26	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
T21	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
T20	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 73
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 73
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 31
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 16
T26	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 9 33
T24	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 9 33
T26	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	33
T24	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	33
T26	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 9 33
T24	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 9 33
T27	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
T25	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR	*	=3X_DIELECTRIC	?

SOURCE: Attila Farkas Email - 8/2/10

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	32 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA_R<7..0>	
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD_R	32
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R	32
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA<7..0>	32 36
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD	32 36
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK	32 36
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R_L	32

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 38 40
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	38 40
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 38 40
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	38 40

Port 2 Not Used

SYNC_MASTER=K91_ERIC SYNC_DATE=08/03/2010

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius’s T29 Routing Notes

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	6 84
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	6 84
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	84
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	84
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	6 84 85
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	6 84 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	84
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 84 95
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 84 95
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	84
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	84
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	84 85
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	84 85
T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
	T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
	T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	95
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	95
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	6 33 78
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	6 33 78
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	6 33 78
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	6 33 78
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 47 84
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 47 84
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	6 8 33 84
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_P<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_N<3..0>	6 8 33 84

Only used on hosts supporting T29 video-in

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 31 44 47 53 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 31 44 47 53 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 44 47 50
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 44 47 50
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 6 31 44 47 50 79
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 6 31 44 47 50 79
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 44 47 62 63
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 44 47 62 63
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 44 47 100
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 44 47 100

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 63
	1TO1_DIFFPAIR		CHGR_CSI_N 63
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 63
	1TO1_DIFFPAIR		CHGR_CSO_N 63

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	75 76
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0>	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0>	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L	75 76
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	6 75 76
L295 FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	6 75 76
L293 FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	6 75 76
L290 FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	6 75 76
L296 FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	6 75 76
L297 FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	6 75 76
L298 FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	6 75 76
L299 FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	6 75 76
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	6 75 76
L299 FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	6 75 76
L300 FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	6 75 76
L302 FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	6 75 76
L302 FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	6 75 76
L303 FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	6 75 76
L304 FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	6 75 76
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	6 75 76
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	6 75 76
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	6 75 76
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	6 75 76
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	6 75 76
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	6 75 76
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	6 75 76
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	6 75 76
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	6 75 76
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L	75 76 77

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	75 77
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	75 77
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	6 75 77
L305 FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	6 75 77
L306 FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	6 75 77
L307 FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	6 75 77
L310 FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	6 75 77
L309 FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	6 75 77
L308 FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	6 75 77
L311 FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	6 75 77
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	6 75 77
L311 FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	6 75 77
L312 FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	6 75 77
L314 FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	6 75 77
L314 FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	6 75 77
L314 FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	6 75 77
L314 FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	6 75 77
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	6 75 77
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	6 75 77
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	6 75 77
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	6 75 77
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	6 75 77
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	6 75 77
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	6 75 77
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	6 75 77
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	6 75 77

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	83 87
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	83 87
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 82 83

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	78 79
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M	78 79
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	78 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	78 87
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	78 79
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	78 79
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	78 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	78 87
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	78 79
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	78 79
DP_MI	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	78 84
	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	78 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	83 84
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	83 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUXCH_P	8 78 83
	DP_85D	DISPLAYPORT	DP_EG_AUXCH_N	8 78 83

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GPU (Whistler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K91 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
		ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	50
		THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	50
J26?	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 50
J26?		THERM_1TO1_55S	THERM	CPU_THERMD_N	9 50
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	50
		THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	50
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	50 78
		THERM_1TO1_55S	THERM	GPU_TDIODE_N	50 78
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	48 64
		SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	48 64
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	48
		SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	48
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	48
		SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	48
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	48 69
		SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	48 69
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	48
		SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	48
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	48
		SENSE_1TO1_55S	SENSE	GPUISENS_P	48
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	48 66
		SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	48 66
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
J24?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
J25?		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
J25?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	100
J25?		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	100
J24?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
J26?		SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
J26?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	100
J26?		SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	100
J26?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
J26?		SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
J26?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
J26?		SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
J26?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	100
J26?		SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	100
J29?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	
J29?		SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	
J29?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	100
J29?		SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	100
J30?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_P	
J30?		SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_N	
J30?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_P	100
J30?		SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_N	100
J30?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_P	
J30?		SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_N	
J30?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_P	100
J30?		SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_N	100
J32?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 68
J33?		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 68
J33?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	49
J33?		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	49
J33?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	49
J33?		SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	49
J33?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	49
J33?		SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	49
J33?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	49
J33?		SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	49
J34?	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
J34?		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
J31?	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 59
J31?		AUDIODIFF	AUDIO	AUD_LO1_R_N	56 59
J31?	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
J31?		AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
J31?	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 59
J31?		AUDIODIFF	AUDIO	AUD_LO2_R_N	56 59
J31?	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	59
J31?		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	59
J31?	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	59
J31?		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	59
J32?	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_P	59
J32?		AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_N	59

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	63
	1TO1_DIFFPAIR		CHGR_CSI_R_N	63
	1TO1_DIFFPAIR		CHGR_CSO_R_P	49 63
	1TO1_DIFFPAIR		CHGR_CSO_R_N	49 63
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 42
	USB_85D	USB	CONN_USB2_BT_P	6
	USB_85D	USB	CONN_USB2_BT_N	6
	USB_85D	USB	USB_LT2_P	6 42
	USB_85D	USB	USB_LT2_N	6 42
J42? AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375L_P	59
J42?	AUDIODIFF	AUDIO	SSM2375L_N	59
J42? AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375R_P	59
J42?	AUDIODIFF	AUDIO	SSM2375R_N	59
J42? AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375S_P	59
J42?	AUDIODIFF	AUDIO	SSM2375S_N	59
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	6 59 60
	USB_85D	USB	USB_TPAD_R_P	52
	USB_85D	USB	USB_TPAD_R_N	52
		SB_POWER	PP3V3_S5	45 55 65 70 71 72 82 85 89 6 7 17 19 20 22 23 24 25 29 39
		SB_POWER	PP3V3_S0	45 49 50 51 53 56 60 61 71 72 6 7 12 16 17 18 19 20 22 23 25 75 83 83 84 87 88 89 41 45 47 75 82
		SB_POWER	PP1V5_S3RS0	
		GND	GND	

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Project Specific Constraints

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K91 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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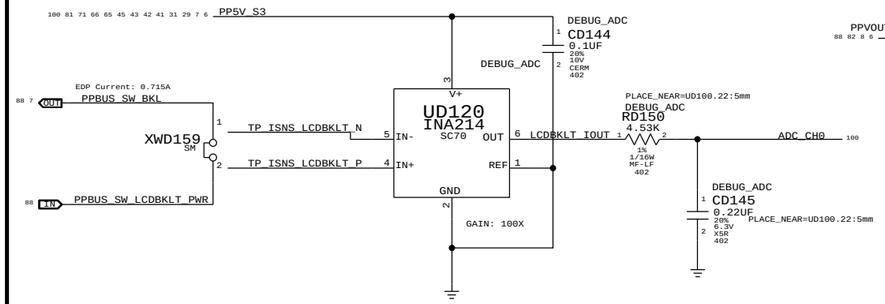
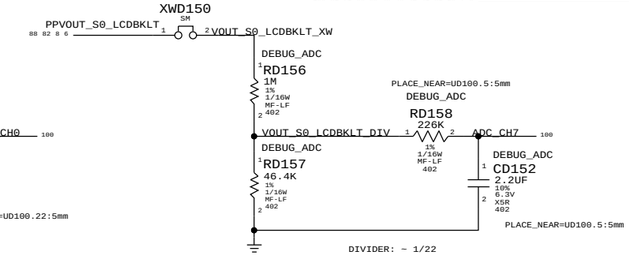
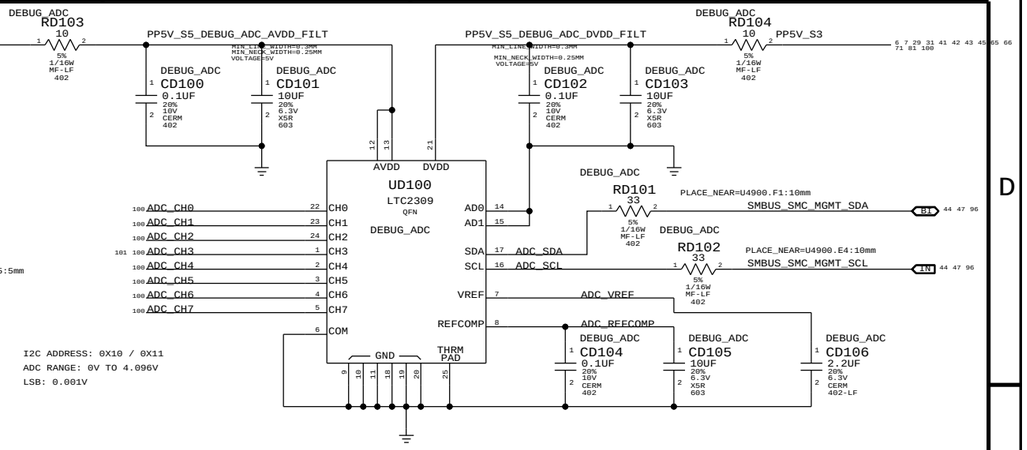
LCD BKLT Current Sense

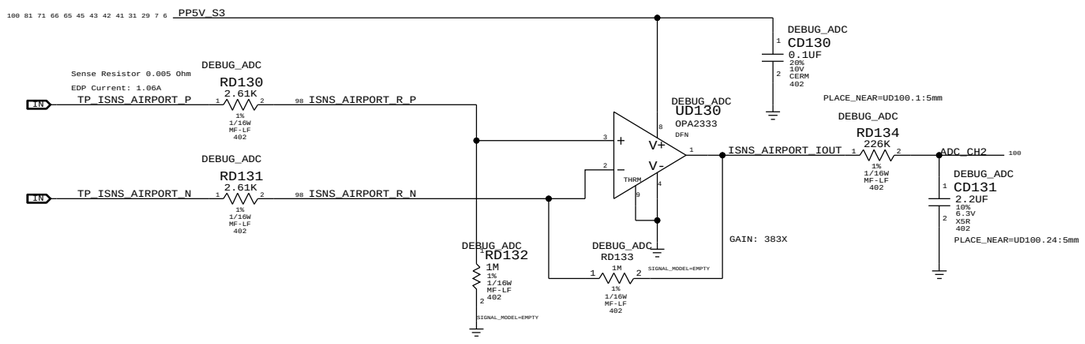


LCD BKLT Voltage Sense

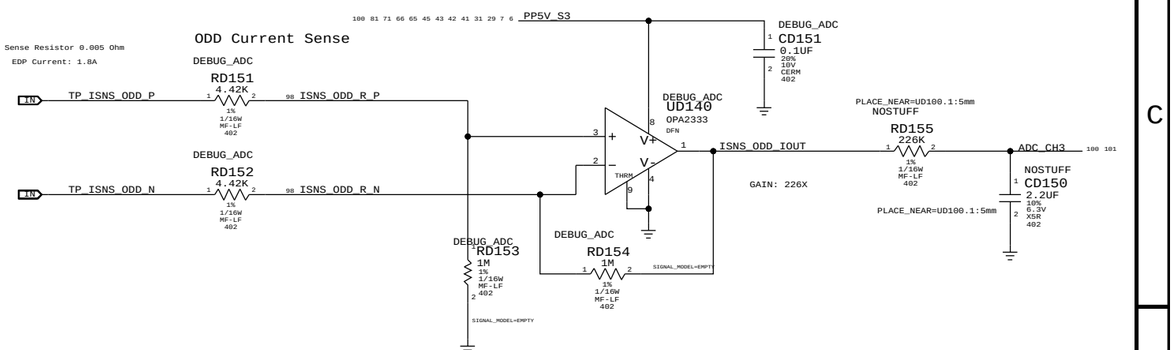




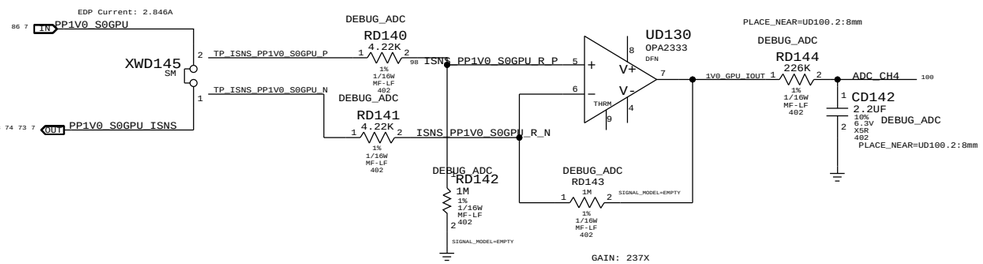
AIRPORT Current Sense



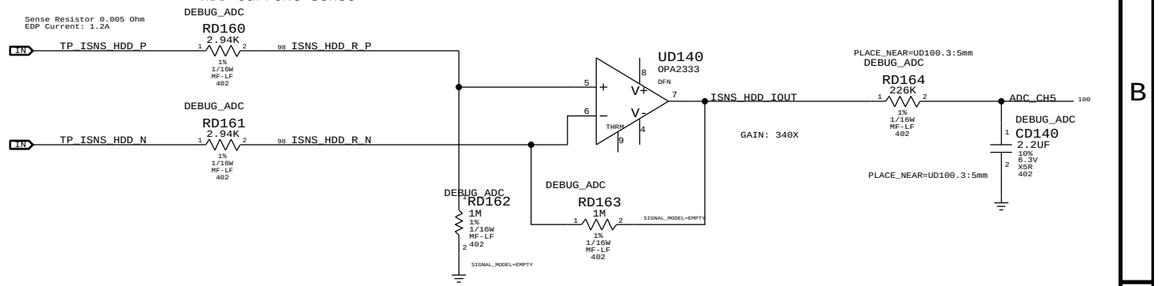
ODD Current Sense



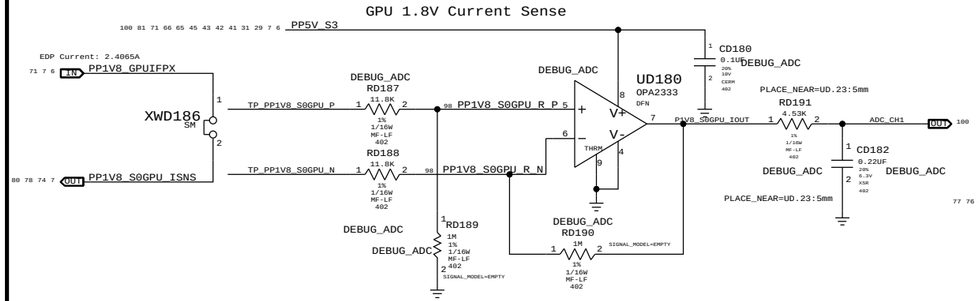
GPU 1.0V Current Sense



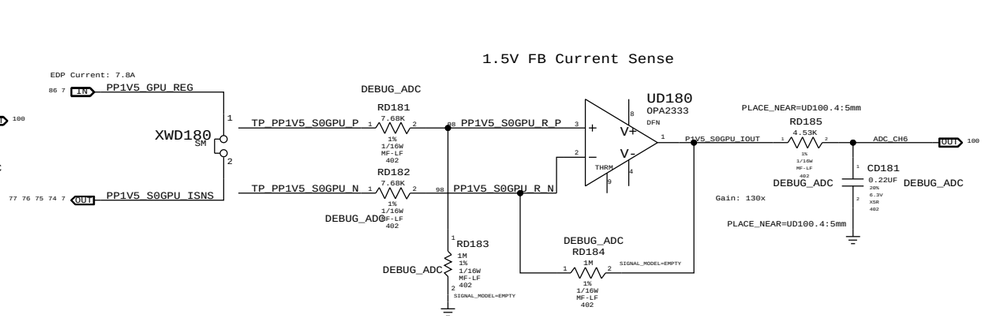
HDD Current Sense



GPU 1.8V Current Sense



1.5V FB Current Sense



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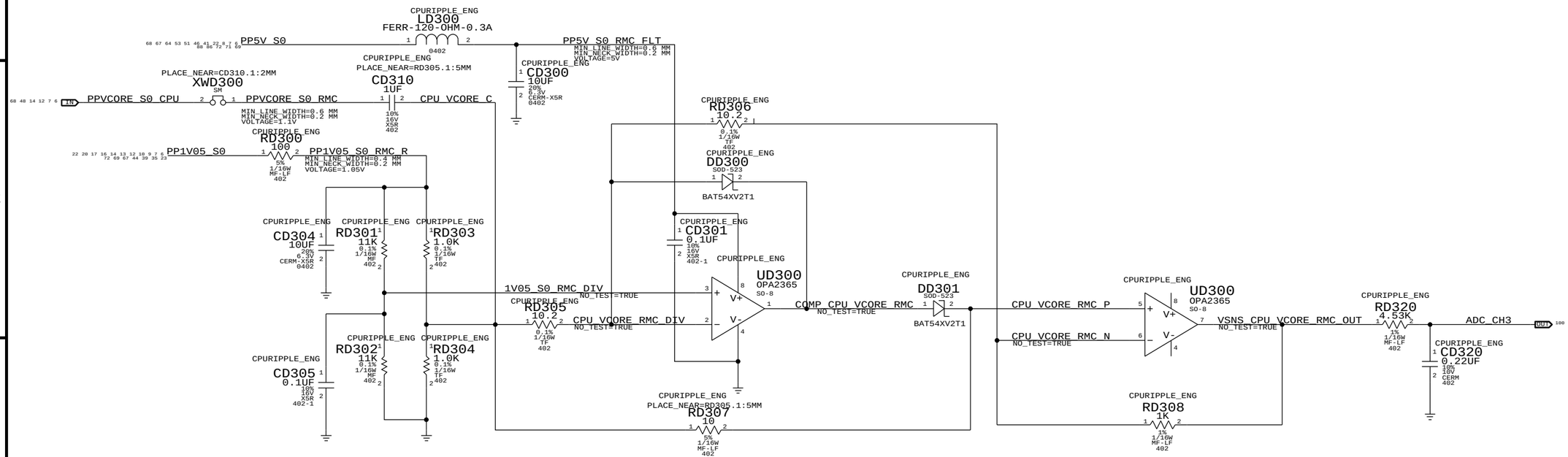

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