1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-03-18

SCHEM,MLB_LDO,K6

PVT, 3/18/10

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8563	1	SCHEM,MLB_LDO,K6	SCH	CRITICAL	
820-2879	1	PCBF,MLB_LDO,K6	PCB	CRITICAL	

DRAWING TITLE=MLB ABBREV=DRAWING LAST_MODIFIED=Thu Mar 18 17:53:39 2010

DRAWING TITLE: SCHEM,MLB_LDO,K6

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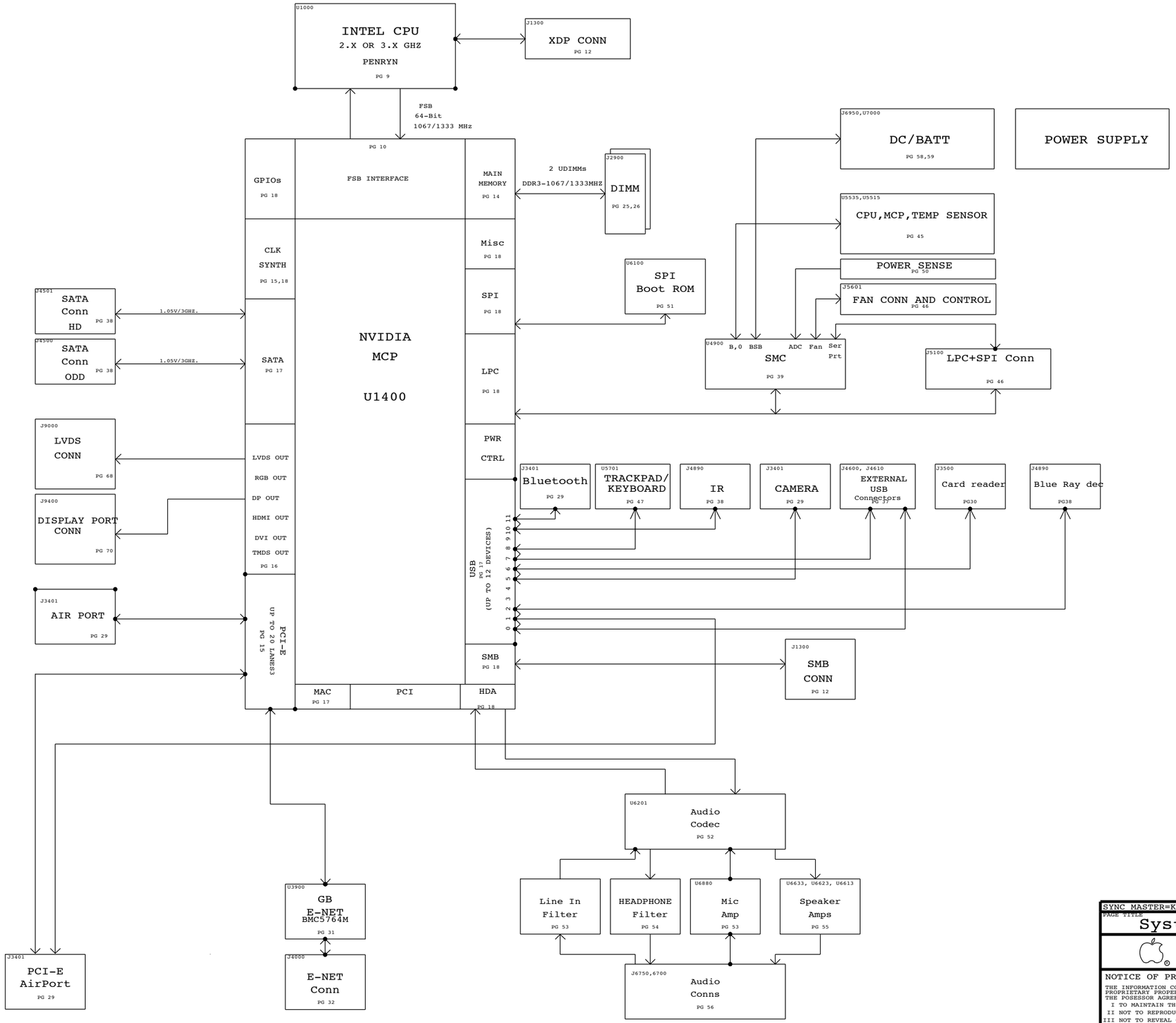

SYNC MASTER=K69 MLB SYNC DATE=08/19/2009

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System Block Diagram

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K6 POWER SYSTEM ARCHITECTURE

PP18V5_DCIN_CONN
Q7080
Q7085
PPDCIN_G3H_OR_PBUS
PBUS_VSENSE
ENABLE
3.425V G3HOT
LT3470
U6990
PP3V42_G3H_REG
SMC PWRGD
RN5VD30A-F
U5010
8A FUSE
F7040
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
Q5315
PBUS_G3H_VSENSE
AC ADAPTER IN
DCIN(16.5V)
F6905
6A FUSE
R7020
SMC_DCIN_ISENSE
CHGR_EN (S5)
ENABLES
VIN
VOUT
PBUS SUPPLY/ BATTERY CHARGER
ISL6259
U7000
R7050
SMC_BATT_ISENSE
CPUVTTS0_EN (S0)
EN_PSV
VOUT
PP1V05_S0
(8A MAX CURRENT)
CPUVTT
(1.05V)
TPS51117
U7600
PGOOD
CPUVTTS0_PGOOD
J6950
3S2P
(9 TO 12.6V)
PPVBAT_G3H_CONN
Q7055
PPVBAT_G3H_CHGR_R
CHGR_BGATE
CPU VCORE
ISL9504B
U7100
IMVP_VR_ON_R
VR_ON
PGOOD
VR_PWRGOOD_DELAY
SMC_CPU_VSENSE
SMC_CPU_ISENSE
PPVCORE_S0_CPU
(44A MAX CURRENT)
MCP89
PWRBTN*
PLTRST*
RSMRST*
CPUPWRGD(GPIO49)
CPU_RESET#
U1400
MCP_PS_PWRGD
U2850
PWRGD
CPU_PWRGD
LPC_RESET_L
PBA_CPURST_L
CPU
PWRGOOD
RESET*
U1000
4.5V AUDIO
MAX8840
U6200
PP4V5_AUDIO_ANALOG
PPBUS_G3H
MCP89
PM_SLP_S4_L
PM_SLP_S3_L
U1400
P3V3S3_EN
DDRREG_EN
P5VS3_EN_L
RC DELAY
SMC
U4900
P16
P60
SMC_PM_G2_EN (S5)
P5VS3_EN_L
VIN
EN1
EN2
5V (RT)
3.3V
TPS51125
U7201
PGOOD1,2
VREG3
VOUT1
VOUT2
PP5V_S3_REG
(13A MAX CURRENT)
PP3V3_S5_REG
(5.5A MAX CURRENT)
P3V3S5_EN_L
U7840
P5V3V3_PGOOD
Q7910
P3V3S3_EN
PP3V3_S3_FET
Q3450
P3V3_S3_WLAN
P3V3ENET_EN_L
Q7940
PP5V_S0_FET
P5VS0_EN
LP8545
U9701
BKLT_EN
ENA
VOUT
PPVOUT_SW_LCDBKLT
Q7930
PP3V3_S0_FET
ISL8009B
U7750
PP0V9_S5_REG
P3V3S0_EN
1.8V
TPS62202
U7760
PP1V8_S0_REG
1.5V
ISL8009B
U7710
PP1V5_S0_REG
1.05V
TPS7470
U7740
PP1V05_S0_MCP_PLL_REG
1.2V
ST1S12G12R
U7720
PP1V2_ENET_REG
SMC
RSMRST_OUT(P15)
PWRGD(P12)
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PWR_BUTTON(P90)
P17(BTN_OUT)
RST*
99ms DLY
PM_RSMRST_L
IMVP_VR_ON_R
PLT_RST*
PM_PWRBTN_L
SMC_RESET_L
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
SLP_S5_L
SLP_S4_L
SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U4900
P1V5S0_PGOOD
P5V3V3_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
MCPPLLDO_PGOOD
S0PGOOD_RST_L
Q7890
AP_PWR_EN
PM_WLAN_EN_L
Q7890,Q7891
PM_SLP_S3_L
SMC_ADAPTER_EN
Q7930
PP1V5R1V35_SW_MCP
1.5V
0.75V
TPS51116
U7300
=DDRREG_EN
=DDTVTT_EN
MCPDDROUT
PP1V5_S3_REG
(12A MAX CURRENT)
PP0V75_S0_REG
(1A MAX CURRENT)
RST*
ISL88042
U7870
PP3V3_S0
PP1V5_S0
PP1V05_S0
MCP_CORE
ISL9563A
U7500
MCPCORES0_EN
PPMCPCORE_S0_R
(25A MAX CURRENT)
R7525 PPMCPCORE_S0_REG
P1V8S0_EN
P1V5S0_EN
CPUVTTS0_EN
DDRVTT_EN
MCPCORES0_EN
PBUSVSENSE_EN (S0)
P5VS0_EN (S0)
P3V3S0_EN

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Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1120	PCBA,MLB_LDO,BETTER,K6	K6_COMMON,CPU:2.4GHZ,MCP89M:A02,EEEE:DD24
639-1119	PCBA,MLB_LDO,BEST,K6	K6_COMMON,CPU:2.66GHZ,MCP89M:A02,EEEE:DD23
085-1634	K6 MLB_LDO DEVELOPMENT BOM	K6_DEVEL:PVT

BOM Groups

BOM GROUP	BOM OPTIONS
K6_COMMON	COMMON,ALTERNATE,K6_MISC,K6_DEBUG:PROD,KB_BL,K6_PROGPARTS,RDRV:NO,SPI:25MHZ,CPU_CAP:15
K6_MISC	DP_ESD,MIKEY,BCM5764M,GL137,ENET_ESD,VFRQ:SLPS3,LVDDR3:YES,MCPPLL_R:REG,S0PGOOD_BJT,BOOST_VOL:LOW,HDA:1.5V
K6_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG,IR:PROG,WELLSPRING:PROG
K6_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,S0PGOOD_ISL,RDRV:IN_DEVEL
K6_DEVEL:PVT	LPCPLUS,XDP_CONN
K6_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K6_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K6_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO,LPCPLUS,MCPHVDD:P2V5,LDO:FIXED,HTOL_SENSE:YES

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3769	1	PDC,SLGVT,PRQ,2.26,25W,1066,R0,3M,BGA,P7550	U1000	CRITICAL	CPU:2.26GHZ
337S3680	1	PDC,LGDZ,PRQ,2.40,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU:2.4GHZ
337S3756	1	PDC,SLGFG,PRQ,2.53,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU:2.53GHZ
337S3761	1	PDC,SLGLA,PRQ,2.66,25W,1066,E0,3M,BGA	U1000	CRITICAL	CPU:2.66GHZ
337S3797	1	IC,MCP89M-A01,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A01
337S3866	1	IC,MCP89M-A01,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A02
341S2731	1	IC,1MBIT,SPI FLASH,K17/18	U3990	CRITICAL	BCM5764M
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER, 8x8, 64QFN	U3900	CRITICAL	BCM5764M
338S0753	1	IC,FW643-E2,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
353S2896	1	IC,LP8545,LED BKLT CTRLR,LLP24	U9701	CRITICAL	

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0240	1	SMC EXTERNAL,K6	U4900	CRITICAL	SMC:PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0238	1	EFI UNLOCKED,K6/K69	U6100	CRITICAL	BOOTROM:UNLOCKED
341S2589	1	IC,EFI,LOCKED,K6	U6100	CRITICAL	BOOTROM:LOCKED
338S0633	1	IC,CYPRS,CY7C63803-LQXC,4X4MM,USB,24-QFN	U4800	CRITICAL	IR:BLANK
341S2384	1	IC,ENCORE II,CY7C63803-LQXC	U4800	CRITICAL	IR:PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING:BLANK
341S2616	1	IC,TP PSOC,K17,K18	U5701	CRITICAL	WELLSPRING:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0693	152S0778		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7550 CPU AS ALTERNATE
152S1135	152S0586		ALL	TOKO AS ALTERNATE
516-0213	516-0201		ALL	MOLEX AS ALTERNATE
516S0790	516S0706		ALL	MOLEX AS ALTERNATE
376S0699	376S0360		ALL	SSM6P15FE AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1634	1	K6 MLB_LDO DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD23]	CRITICAL	EEEE:DD23
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD24]	CRITICAL	EEEE:DD24

K6 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

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BOM Configuration

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Revision History

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Functional Test Points

Fan Connectors

P1	TRUE	PP5V_S0	(NEED 2 TP) 6 7 65
P2	TRUE	FAN_RT_PWM	46
P3	TRUE	FAN_RT_TACH	46

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

P200	TRUE	BI_MIC_LO	55 56
P201	TRUE	BI_MIC_HI	55 56
P202	TRUE	BI_MIC_SHIELD	55 56

SPEAKER FUNC_TEST

P210	TRUE	SPKRAMP_L_N_OUT	54 55
P211	TRUE	SPKRAMP_L_P_OUT	54 55
P212	TRUE	SPKRAMP_R_N_OUT	54 55
P213	TRUE	SPKRAMP_R_P_OUT	54 55
P214	TRUE	SPKRAMP_SUB_N_OUT	54 55
P215	TRUE	SPKRAMP_SUB_P_OUT	54 55

LVDS FUNC_TEST

P301	TRUE	PP3V3_LCDVDD_SW_F	6 67
P302	TRUE	PP3V3_S0_LCD_F	6 67
P303	TRUE	PPVOUT_SW_LCDBKLT	67 70
P304	TRUE	BKL_VSYNC	67 70
P1400	TRUE	LVDS_DDC_CLK	8 67
P1401	TRUE	LVDS_DDC_DATA	8 67
P305	TRUE	LVDS_IG_A_DATA_N<0>	8 67 74
P306	TRUE	LVDS_IG_A_DATA_P<0>	8 67 74
P307	TRUE	LVDS_IG_A_DATA_N<1>	8 67 74
P308	TRUE	LVDS_IG_A_DATA_P<1>	8 67 74
P309	TRUE	LVDS_IG_A_DATA_N<2>	8 67 74
P310	TRUE	LVDS_IG_A_DATA_P<2>	8 67 74
P1404	TRUE	LVDS_CONN_A_CLK_F_N	67 79
P1405	TRUE	LVDS_CONN_A_CLK_F_P	67 79
P311	TRUE	LED_RETURN_1	67 70
P312	TRUE	BKL_ISEN2	70
P313	TRUE	BKL_ISEN3	70
P1406	TRUE	LED_RETURN_4	67 70
P1407	TRUE	LED_RETURN_5	67 70
P1408	TRUE	LED_RETURN_6	67 70

(NEED TO ADD 5 GND TP)

SATA ODD CONN

P240	TRUE	PP5V_SW_ODD	(NEED 4 TP) 6 8
P241	TRUE	SMC_ODD_DETECT	36 39
P242	TRUE	SATA_ODD_D2R_UF_P	36 79
P243	TRUE	SATA_ODD_D2R_UF_N	36 79
P244	TRUE	SATA_ODD_R2D_P	36 74
P245	TRUE	SATA_ODD_R2D_N	36 74

(NEED TO ADD 4 GND TP)

SATA HDD/IR/SIL

P316	TRUE	PP5V_S0_HDD_FLT	(NEED 3 TP) 6 36
P314	TRUE	SATA_HDD_R2D_P	36 74
P315	TRUE	SATA_HDD_R2D_N	36 74
P318	TRUE	SATA_HDD_D2R_C_P	36 74
P317	TRUE	SATA_HDD_D2R_C_N	36 74
P307	TRUE	SYS_LED_ANODE_R	36
P309	TRUE	IR_RX_OUT	36 38
P311	TRUE	PP5V_S3_IR_R	36

(NEED TO ADD 5 GND TP)

BATT POWER CONN

P222	TRUE	SMBUS_SMC_BSA_SCL	6 42 78
P221	TRUE	SMBUS_SMC_BSA_SDA	6 42 78
P220	TRUE	SYS_DETECT_L	57
P205	TRUE	PPVBAT_G3H_CONN	(NEED 3 TP) 57 58

(NEED TO ADD 4 GND TP)

BIL CONN

P420	TRUE	PP3V42_G3H	6 7
P422	TRUE	SMBUS_SMC_BSA_SCL	6 42 78
P424	TRUE	SMBUS_SMC_BSA_SDA	6 42 78
P425	TRUE	SMC_BIL_BUTTON_L	39 40 57
P408	TRUE	SMC_LID_R	57

(NEED TO ADD 4 GND TP)

RIGHT CLUTCH CONN

P252	TRUE	PP5V_S3_BTCAMERA_F	29
P251	TRUE	PCIE_AP_D2R_P	15 29 74
P252	TRUE	PCIE_AP_D2R_N	15 29 74
P260	TRUE	PCIE_AP_R2D_P	29 74
P257	TRUE	PCIE_AP_R2D_N	29 74
P258	TRUE	PCIE_CLK100M_AP_CONN_P	29 79
P253	TRUE	PCIE_CLK100M_AP_CONN_N	29 79
P257	TRUE	USB_CAMERA_CONN_P	29 79
P254	TRUE	USB_CAMERA_CONN_N	29 79
P248	TRUE	PP5V_WLAN	(NEED 2 TP) 6 29
P252	TRUE	PCIE_WAKE_L	15 24 29
P256	TRUE	SMBUS_SMC_A_S3_SCL	6 42 78
P251	TRUE	SMBUS_SMC_A_S3_SDA	6 42 78
P255	TRUE	USB_BT_CONN_P	29 79
P250	TRUE	USB_BT_CONN_N	29 79
P212	TRUE	AP_CLKREQ_Q_L	29
P256	TRUE	AP_RESET_CONN_L	29

(NEED TO ADD 6 GND TP)

IPD_FLEX_CONN

P200	TRUE	PP3V3_S3	6 7
P274	TRUE	PP18V5_S3	6 48
P272	TRUE	Z2_CS_L	47 48
P270	TRUE	Z2_DEBUG3	47 48
P271	TRUE	Z2_MOSI	47 48
P268	TRUE	Z2_MISO	47 48
P269	TRUE	Z2_SCLK	47 48
P273	TRUE	Z2_BOOST_EN	48
P266	TRUE	Z2_HOST_INTN	47 48
P265	TRUE	Z2_CLKIN	47 48
P263	TRUE	Z2_KEY_ACT_L	47 48
P264	TRUE	Z2_RESET	47 48
P262	TRUE	PSOC_MISO	47 48
P260	TRUE	PSOC_MOSI	47 48
P261	TRUE	PSOC_SCLK	47 48
P257	TRUE	SMBUS_SMC_A_S3_SDA	6 42 78
P258	TRUE	SMBUS_SMC_A_S3_SCL	6 42 78
P277	TRUE	PSOC_F_CS_L	47 48
P278	TRUE	PICKB_L	47 48

(NEED TO ADD 2 GND TP)

KEYBOARD CONN

P354	TRUE	PP3V3_S3	6 7
P355	TRUE	PP3V42_G3H	6 7
P344	TRUE	WS_KBD1	47
P345	TRUE	WS_KBD2	47
P346	TRUE	WS_KBD3	47
P347	TRUE	WS_KBD4	47
P349	TRUE	WS_KBD5	47
P348	TRUE	WS_KBD6	47
P350	TRUE	WS_KBD7	47
P357	TRUE	WS_KBD8	47
P351	TRUE	WS_KBD9	47
P353	TRUE	WS_KBD10	47
P327	TRUE	WS_KBD11	47
P328	TRUE	WS_KBD12	47
P329	TRUE	WS_KBD13	47
P343	TRUE	WS_KBD14	47
P342	TRUE	WS_KBD15_CAP	47
P341	TRUE	WS_KBD16_NUM	47
P339	TRUE	WS_KBD17	47
P340	TRUE	WS_KBD18	47
P338	TRUE	WS_KBD19	47
P336	TRUE	WS_KBD20	47
P337	TRUE	WS_KBD21	47
P335	TRUE	WS_KBD22	47
P333	TRUE	WS_KBD23	47
P330	TRUE	WS_KBD_ONOFF_L	47
P332	TRUE	WS_LEFT_SHIFT_KBD	47
P326	TRUE	WS_LEFT_OPTION_KBD	47
P331	TRUE	WS_CONTROL_KBD	47

(NEED TO ADD 2 GND TP)

KBD BACKLIGHT CONN

P350	TRUE	KBDLED_ANODE	48
P324	TRUE	SMC_KDBLED_PRESENT_L	48

(NEED TO ADD 1 GND TP)

T57 CONN

P409	TRUE	PP5V_S3	6 7
P409	TRUE	PP3V3_S3	6 7
P410	TRUE	T57_PWR_EN	18
P411	TRUE	T57_RESET	18
P413	TRUE	USB_T57_N	38 75
P412	TRUE	USB_T57_P	38 75

(NEED TO ADD 5 GND TP)

DEBUG VOLTAGE

P207	TRUE	PPVCORE_S0_CPU	7 43
P208	TRUE	PPVCORE_S0_MCP	7 43
P1416	TRUE	PP1V2_ENET	7
P209	TRUE	PP1V05_S0	7 65
P210	TRUE	PP1V5_S0	7 65 79
P211	TRUE	PP1V8_S0	7
P212	TRUE	PP3V3_S0	7 65 79
P213	TRUE	PP5V_S0	6 7 65
P214	TRUE	PP3V3_S3	6 7
P215	TRUE	PP5V_S3	6 7
P1418	TRUE	PP0V9_S5	7
P216	TRUE	PP3V3_S5	7 65 79
P217	TRUE	PP3V42_G3H	6 7
P218	TRUE	PPBUS_G3H	7 43
P1419	TRUE	PP3V3_ENET	7
P219	TRUE	PP5V_WLAN	6 29
P221	TRUE	PP5V_SW_ODD	6 8
P220	TRUE	PP5V_S0_HDD_FLT	6 36
P222	TRUE	PP18V5_S3	6 48
P1420	TRUE	PP3V3_S0_LCD_F	6 67
P223	TRUE	PP3V3_LCDVDD_SW_F	6 67
P224	TRUE	PP4V5_AUDIO_ANALOG	51
P1421	TRUE	PP1V5R1V35_S3	7 79
P225	TRUE	SMC_PM_G2_EN	39 65
P226	TRUE	PM_SLP_S4_L	18 39 40 65
P227	TRUE	PM_SLP_S3_L	18 39 65 69

(NEED TO ADD 6 GND TP)

SPI DEBUG CONN

P1422	TRUE	PP3V42_G3H	6 7
P1423	TRUE	SPI_CS0_L	41 75
P1424	TRUE	SPI_CLK	41 75
P1425	TRUE	SPI_MOSI	41 75
P1426	TRUE	SPI_MISO	18 41 75
P1427	TRUE	SPIROM_USE_MLB	18 41 50

DC POWER CONN

P1672	TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP) 57
P1674	TRUE	ADAPTER_SENSE	57

(NEED TO ADD 4 GND TP)

FSB SIGNALS WITH NOTEST

P390	NO_TEST=TRUE	FSB_A_L<35..3>	9 13 72
P395	NO_TEST=TRUE	FSB_ADS_L	9 13 72
P397	NO_TEST=TRUE	FSB_ADSTB_L<1..0>	9 13 72
P399	NO_TEST=TRUE	FSB_D_L<63..0>	9 13 72
P400	NO_TEST=TRUE	FSB_DINV_L<3..0>	9 13 72
P402	NO_TEST=TRUE	FSB_DSTB_L_N<3..0>	9 13 72
P406	NO_TEST=TRUE	FSB_DSTB_L_P<3..0>	9 13 72
P403	NO_TEST=TRUE	FSB_HIT_L	9 13 72
P404	NO_TEST=TRUE	FSB_HITM_L	9 13 72
P405	NO_TEST=TRUE	FSB_LOCK_L	9 13 72
P405	NO_TEST=TRUE	FSB_REQ_L<4..0>	9 13 72

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FUNC TEST

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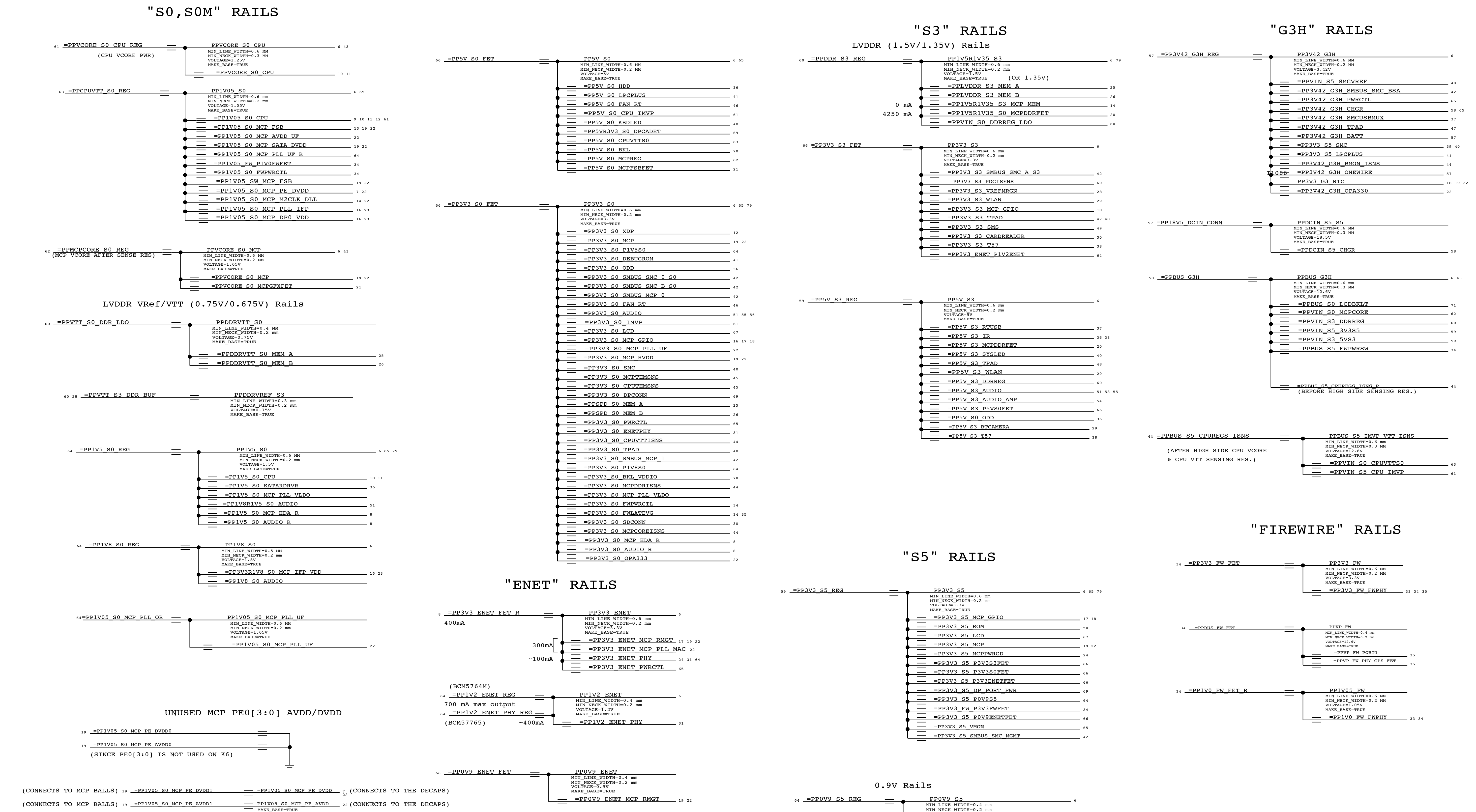

SYNC_MASTER=K24_MLB SYNC_DATE=07/22/2009

PAGE TITLE

Power Aliases

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

REVISION A.13.0

BRANCH

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HEATSINK STANDOFFS

Z0902
STDOFF-4.5OD.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.5OD.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

Z0905
STDOFF-4.5OD.98H-1.1-3.48-TH
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT Z0906 3R2P5
OMIT Z0907 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT Z0908 3R2P5
OMIT Z0909 3R2P5
OMIT Z0910 3R2P5
OMIT Z0911 3R2P5
OMIT Z0912 3R2P5

EMI IO (SHORT) POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-K19-K24 SM
ZS0901 1.4DIA-SHORT-EMI-MLB-K19-K24 SM
ZS0902 1.4DIA-SHORT-EMI-MLB-K19-K24 SM
ZS0903 1.4DIA-SHORT-EMI-MLB-K19-K24 SM
ZS0908 1.4DIA-SHORT-EMI-MLB-K19-K24 SM
ZS0909 1.4DIA-SHORT-EMI-MLB-K19-K24 SM

EMI TALL POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98 SM

PCI-E ALIASES

UNUSED GPU LANES

15 =PEG_D2R_N<3:0> — NC_PEG_D2R_N<3:0> NO_TEST=TRUE MAKE_BASE=TRUE
15 =PEG_D2R_P<3:0> — NC_PEG_D2R_P<3:0> NO_TEST=TRUE MAKE_BASE=TRUE
15 =PEG_R2D_C_N<3:0> — NC_PEG_R2D_C_N<3:0> NO_TEST=TRUE MAKE_BASE=TRUE
15 =PEG_R2D_C_P<3:0> — NC_PEG_R2D_C_P<3:0> NO_TEST=TRUE MAKE_BASE=TRUE
74 15 PEG_CLK100M_P — TP_PEG_CLK100M_P MAKE_BASE=TRUE
74 15 PEG_CLK100M_N — TP_PEG_CLK100M_N MAKE_BASE=TRUE
15 PEG_CLKREQ_L — TP_PEG_CLKREQ_L MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

75 17 USB_EXTC_P — TP_USB_EXTCP MAKE_BASE=TRUE
75 17 USB_EXTC_N — TP_USB_EXTCN MAKE_BASE=TRUE
75 17 USB_EXTD_P — TP_USB_EXTDP MAKE_BASE=TRUE
75 17 USB_EXTD_N — TP_USB_EXTDN MAKE_BASE=TRUE
75 17 USB_WM_P — TP_USB_WMP MAKE_BASE=TRUE
75 17 USB_WM_N — TP_USB_WMN MAKE_BASE=TRUE
75 17 USB_MINI_P — TP_USB_MINIP MAKE_BASE=TRUE
75 17 USB_MINI_N — TP_USB_MININ MAKE_BASE=TRUE

ETHERNET ALIASES

PLACE_NEAR=U7980.A1:5MM
R0911 0 5% 1/16W MF-LF 402
PP3V3_ENET_FET — 1 2 — =PP3V3_ENET_FET_R OUT 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
66 =PP3V3_ENET_FET

ENET_RXD_PD MAKE_BASE=TRUE
ENET_RXD<0> OUT 17 76
ENET_RXD<1> OUT 17 76
ENET_RXD<2> OUT 17 76
ENET_RXD<3> OUT 17 76
ENET_RXCLK_PD MAKE_BASE=TRUE
ENET_CLK125M_RXCLK OUT 17 76
ENET_RX_CTRL OUT 17 76
ENET_MDIO BI 17 76
MCP_RGMII_VREF OUT 17
ENET_LOW_PWR OUT 18 31
R0980 10K 5% 1/16W MF-LF 402
R0981 10K 5% 1/16W MF-LF 402
R0982 10K 5% 1/16W MF-LF 402
R0983 10K 5% 1/16W MF-LF 402
R0984 10K 5% 1/16W MF-LF 402
R0986 10K 5% 1/16W MF-LF 402
NO STUFF

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

74 MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET NO_TEST=TRUE MAKE_BASE=TRUE
74 MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF NO_TEST=TRUE MAKE_BASE=TRUE
MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN NO_TEST=TRUE MAKE_BASE=TRUE
MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT NO_TEST=TRUE MAKE_BASE=TRUE
74 CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR NO_TEST=TRUE MAKE_BASE=TRUE
74 CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y NO_TEST=TRUE MAKE_BASE=TRUE
74 CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB NO_TEST=TRUE MAKE_BASE=TRUE
74 CRT_IG_HSYNC — NC_CRT_IG_HSYNC NO_TEST=TRUE MAKE_BASE=TRUE
74 CRT_IG_VSYNC — NC_CRT_IG_VSYNC NO_TEST=TRUE MAKE_BASE=TRUE

LVDS ALIASES

16 =MCP_IFPA_TXC_P — LVDS_IG_A_CLK_P 67 74
16 =MCP_IFPA_TXC_N — LVDS_IG_A_CLK_N MAKE_BASE=TRUE 67 74
16 =MCP_IFPA_TXD_P<0..2> — LVDS_IG_A_DATA_P<0..2> MAKE_BASE=TRUE 6 67 74
16 =MCP_IFPA_TXD_N<0..2> — LVDS_IG_A_DATA_N<0..2> MAKE_BASE=TRUE 6 67 74
16 =MCP_IFPA_TXD_P<3> — NC_LVDS_IG_A_DATAP<3> NO_TEST=TRUE MAKE_BASE=TRUE
16 =MCP_IFPA_TXD_N<3> — NC_LVDS_IG_A_DATAN<3> NO_TEST=TRUE MAKE_BASE=TRUE
16 =MCP_IFPB_TXC_P — NC_LVDS_IG_B_CLKP NO_TEST=TRUE MAKE_BASE=TRUE
16 =MCP_IFPB_TXC_N — NC_LVDS_IG_B_CLKN NO_TEST=TRUE MAKE_BASE=TRUE
16 =MCP_IFPB_TXD_P<0..3> — NC_LVDS_IG_B_DATAP<0..3> NO_TEST=TRUE MAKE_BASE=TRUE
16 =MCP_IFPB_TXD_N<0..3> — NC_LVDS_IG_B_DATAN<0..3> NO_TEST=TRUE MAKE_BASE=TRUE
16 LCD_IG_BKLT_PWM — LCD_BKLT_PWM MAKE_BASE=TRUE 70
16 LCD_IG_BKLT_EN — LCD_BKLT_EN MAKE_BASE=TRUE 71
16 =MCP_IFPAB_DDC_CLK — LVDS_DDC_CLK MAKE_BASE=TRUE 6 67
16 =MCP_IFPAB_DDC_DATA — LVDS_DDC_DATA MAKE_BASE=TRUE 6 67

DISPLAY PORT ALIASES

16 DP_IG_ML0_P<0..3> — 74 — DP_IG_ML_P<0..3> — DP_EXT_ML_P<0..3> MAKE_BASE=TRUE 69 79
16 DP_IG_ML0_N<0..3> — 74 — DP_IG_ML_N<0..3> — DP_EXT_ML_N<0..3> MAKE_BASE=TRUE 69 79
16 DP_IG_HPD0 — DP_EXT_HPD 69
16 DP_IG_AUX_CH0_P — DP_IG_AUX_CH_P MAKE_BASE=TRUE 68 74
16 DP_IG_AUX_CH0_N — DP_IG_AUX_CH_N MAKE_BASE=TRUE 68 74
68 DP_AUX_CH_C_N — DP_EXT_AUX_CH_C_N MAKE_BASE=TRUE 69 79
68 DP_AUX_CH_C_P — DP_EXT_AUX_CH_C_P MAKE_BASE=TRUE 69 79
68 DP_CA_DET — DP_EXT_CA_DET MAKE_BASE=TRUE 69
16 DP_IG_ML1_P<0..3> — TP_DP_IG_ML1P<0..3> MAKE_BASE=TRUE
16 DP_IG_ML1_N<0..3> — TP_DP_IG_ML1N<0..3> MAKE_BASE=TRUE
16 DP_IG_AUX_CH1_P — TP_DP_IG_AUX_CH1P MAKE_BASE=TRUE
16 DP_IG_AUX_CH1_N — TP_DP_IG_AUX_CH1N MAKE_BASE=TRUE
16 DP_IG_HPD1 — R0920 100K 5% 1/16W MF-LF 402 — MAKE_BASE=TRUE

AUDIO ALIASES

HDA:1.5V
7 =PP1V5_S0_AUDIO_R — R0912 0 5% 1/16W MF-LF 402 — PP3V3R1V5_S0_AUDIO MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6mm VOLTAGE=1.5V MIN_NECK_WIDTH=0.2mm
HDA:3.3V
7 =PP3V3_S0_AUDIO_R — R0913 0 5% 1/16W MF-LF 402 — =PP3V3R1V5_S0_AUDIO 51
HDA:1.5V
7 =PP1V5_S0_MCP_HDA_R — R0914 0 5% 1/16W MF-LF 402 — PP3V3R1V5_S0_MCP_HDA MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6mm VOLTAGE=1.5V MIN_NECK_WIDTH=0.2mm
HDA:3.3V
7 =PP3V3_S0_MCP_HDA_R — R0915 0 5% 1/16W MF-LF 402 — =PP3V3R1V5_S0_MCP_HDA 18 22

CPU ALIASES

72 9 CPU_BSEL<0:2> — =MCP_BSEL<0:2> MAKE_BASE=TRUE 13
13 CPU_PECI_MCP — TP_CPU_PECI_MCP MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

MCP89 ALIASES

16 TP_MCP_RGB_RED — NC_MCP_RGB_RED MAKE_BASE=TRUE NO_TEST=TRUE
16 TP_MCP_RGB_GREEN — NC_MCP_RGB_GREEN MAKE_BASE=TRUE NO_TEST=TRUE
16 TP_MCP_RGB_BLUE — NC_MCP_RGB_BLUE MAKE_BASE=TRUE NO_TEST=TRUE
16 TP_MCP_RGB_HSYNC — NC_MCP_RGB_HSYNC MAKE_BASE=TRUE NO_TEST=TRUE
16 TP_MCP_RGB_VSYNC — NC_MCP_RGB_VSYNC MAKE_BASE=TRUE NO_TEST=TRUE
16 TP_MCP_RGB_DAC_RSET — NC_MCP_RGB_DAC_RSET MAKE_BASE=TRUE NO_TEST=TRUE
16 TP_MCP_RGB_DAC_VREF — NC_MCP_RGB_DAC_VREF MAKE_BASE=TRUE NO_TEST=TRUE

5V ODD ALIASES

6 PP5V_SW_ODD — =PP5V_SW_ODD 36
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.4 MM
VOLTAGE=5V
=PP5V_SW_ODD_FET 36

BACKLIGHT CONTROLLER ALIASES

PLACE_NEAR=L9701.1:5MM
71 70 PPBUS_SW_LCDBKLT_PWR — R0910 0 5% 1/16W MF-LF 402 — PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_SW_BKL 70

CHARGER SIGNAL

58 =CHGR_ACOK IN — SMC_BC_ACOK MAKE_BASE=TRUE OUT 39 40 57

MCPCOREISNS SIGNAL

62 MCPCORES0_VO — MCPCOREISNS_N MAKE_BASE=TRUE — =MCPCOREISNS_N 44
62 MCPCORES0_ISP_R — MCPCOREISNS_P MAKE_BASE=TRUE — =MCPCOREISNS_P 44

SYNC MASTER=K24 MLB
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SIGNAL ALIAS

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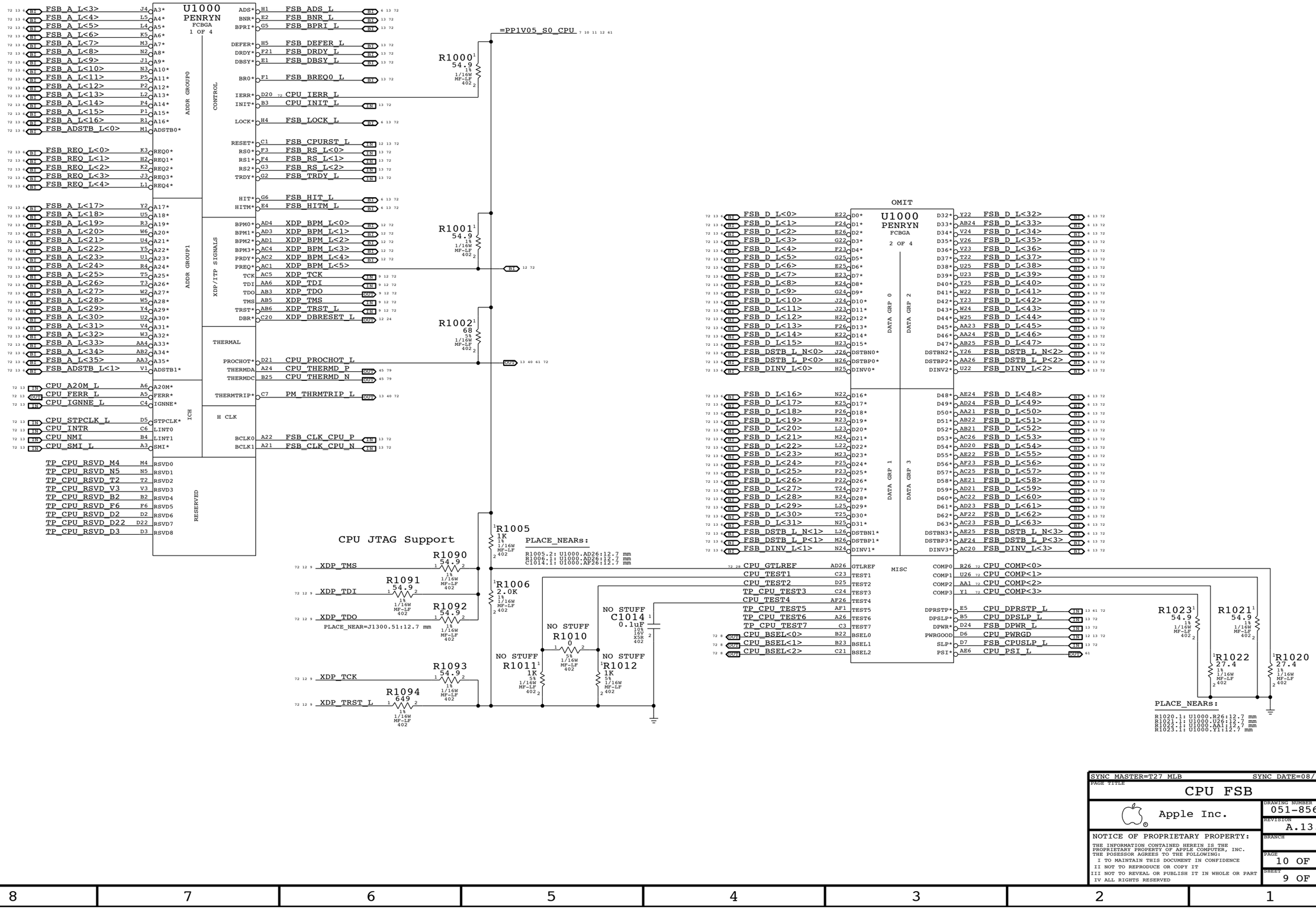

SYNC_MASTER=T27_MLB SYNC_DATE=08/27/2009

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CPU FSB

Apple Inc.

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REVISION A.13.0

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(CPU CORE POWER)

=PPVCORE_S0_CPU 7 10 11

44 A (SV Design Target)
41 A (SV HFM)
30.4 A (SV LFM)
23 A (LV Design Target)

OMIT
U1000
PENRYN
FCBGA
3 OF 4

VCC: A7, A9, A10, A12, A13, A15, A17, A18, A20, B7, B9, B10, B12, B14, B15, B17, B18, B20, C9, C10, C12, C13, C15, C17, C18, D9, D10, D12, D14, D15, D17, D18, E7, E9, E10, E12, E13, E15, E17, E18, E20, F7, F9, F10, F12, F14, F15, F17, F18, F20, AA7, AA9, AA10, AA12, AA13, AA15, AA17, AA18, AA20, AB9, AC10, AB10, AB12, AB14, AB15, AB17, AB18

VCC: AB20, AB7, AC7, AC9, AC12, AC13, AC15, AC17, AC18, AD7, AD9, AD10, AD12, AD14, AD15, AD17, AD18, AE9, AE10, AE12, AE13, AE15, AE17, AE18, AE20, AF9, AF10, AF12, AF14, AF15, AF17, AF18, AF20

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU 7 9 11 12 61

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21, V6, J6, K6, M6, J21, K21, M21, N21, N6, R21, R6, T21, T6, V21, W21

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU 7 11

130 mA

(BR1#)

VCCA: B26, C26

VID0 AD6 CPU_VID<0> OUT 61 72
VID1 AF5 CPU_VID<1> OUT 61 72
VID2 AE5 CPU_VID<2> OUT 61 72
VID3 AF4 CPU_VID<3> OUT 61 72
VID4 AE3 CPU_VID<4> OUT 61 72
VID5 AF3 CPU_VID<5> OUT 61 72
VID6 AE2 CPU_VID<6> OUT 61 72

VCCSENSE AF7 CPU_VCCSENSE_P OUT 61 72

VSSSENSE AE7 CPU_VCCSENSE_N OUT 61 72

=PPVCORE_S0_CPU 7 10 11

R1100
100
1%
1/16W
MF-LF
402

PLACE_NEAR=U1000.AF7:25.4 mm

PLACE_NEAR=U1000.AE7:25.4 mm

R1101
100
1%
1/16W
MF-LF
402

OMIT
U1000
PENRYN
FCBGA
4 OF 4

VSS: A4, A8, A11, A14, A16, A19, A23, AF2, B6, B8, B11, B13, B16, B19, B21, B24, C5, C8, C11, C14, C16, C19, C2, C22, C25, D1, D4, D8, D11, D13, D16, D19, D23, D26, E3, E6, E8, E11, E14, E16, E19, E21, E24, F5, F8, F11, F13, F16, F19, F2, F22, F25, G4, G1, G23, G26, H3, H6, H21, H24, J2, J5, J22, J25, K1, K4, K23, K26, L3, L6, L21, L24, M2, M5, M22, M25, N1, N4, N23, N26, P3, B1

VSS: P6, R21, R24, R2, R5, R22, R25, T1, T4, T23, T26, U3, U6, U21, U24, V2, V5, V22, V25, W1, W4, W23, W26, Y3, Y6, Y21, Y24, AA2, AA5, AA8, AA11, AA14, AA16, AA19, AA22, AA25, AB1, AB4, AB8, AB11, AB13, AB16, AB19, AB23, AB26, AC3, AC6, AC8, AC11, AC14, AC16, AC19, AC21, AC24, AD2, AD5, AD8, AD11, AD13, AD16, AD19, AD22, AD25, AE1, AE4, AE8, AE11, AE14, AE16, AE19, AE23, AE26, A2, AF6, AF8, AF11, AF13, AF16, AF19, AF21, A25, AF25

(Socket-P KEY)

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=T27 MLB
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CPU Power & Ground

Apple Inc.

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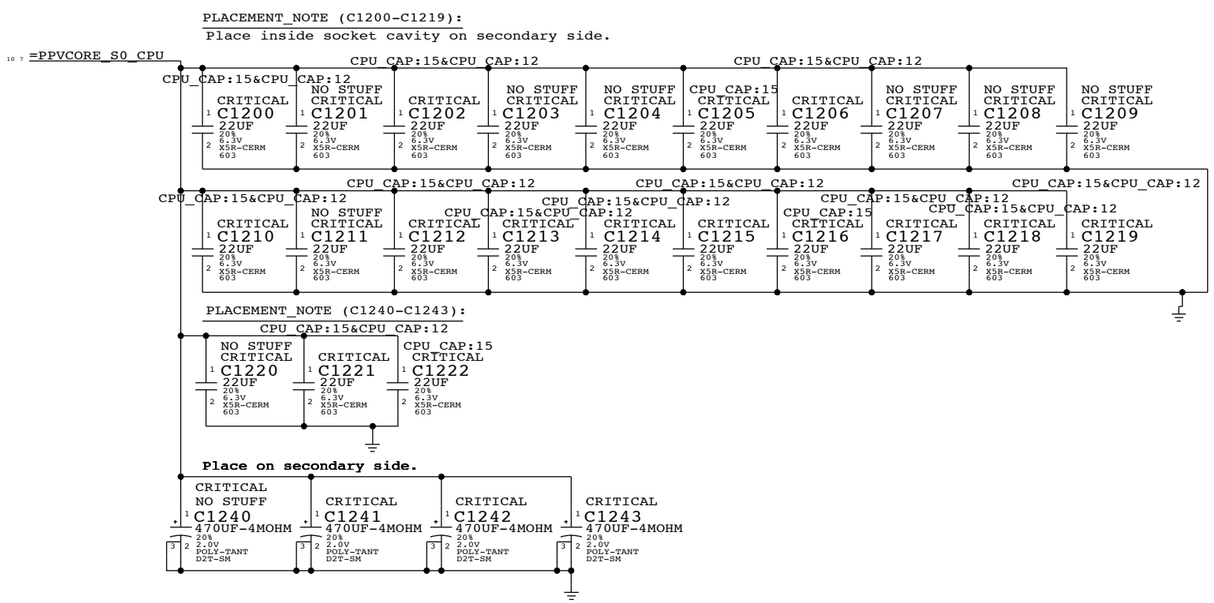
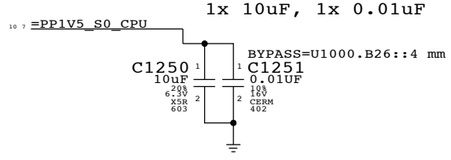
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



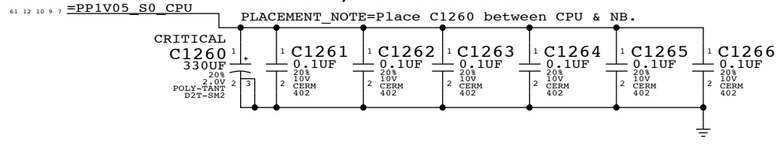
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC MASTER=T27 MLB SYNC DATE=11/23/2009

PAGE TITLE: CPU Decoupling

Apple Inc.

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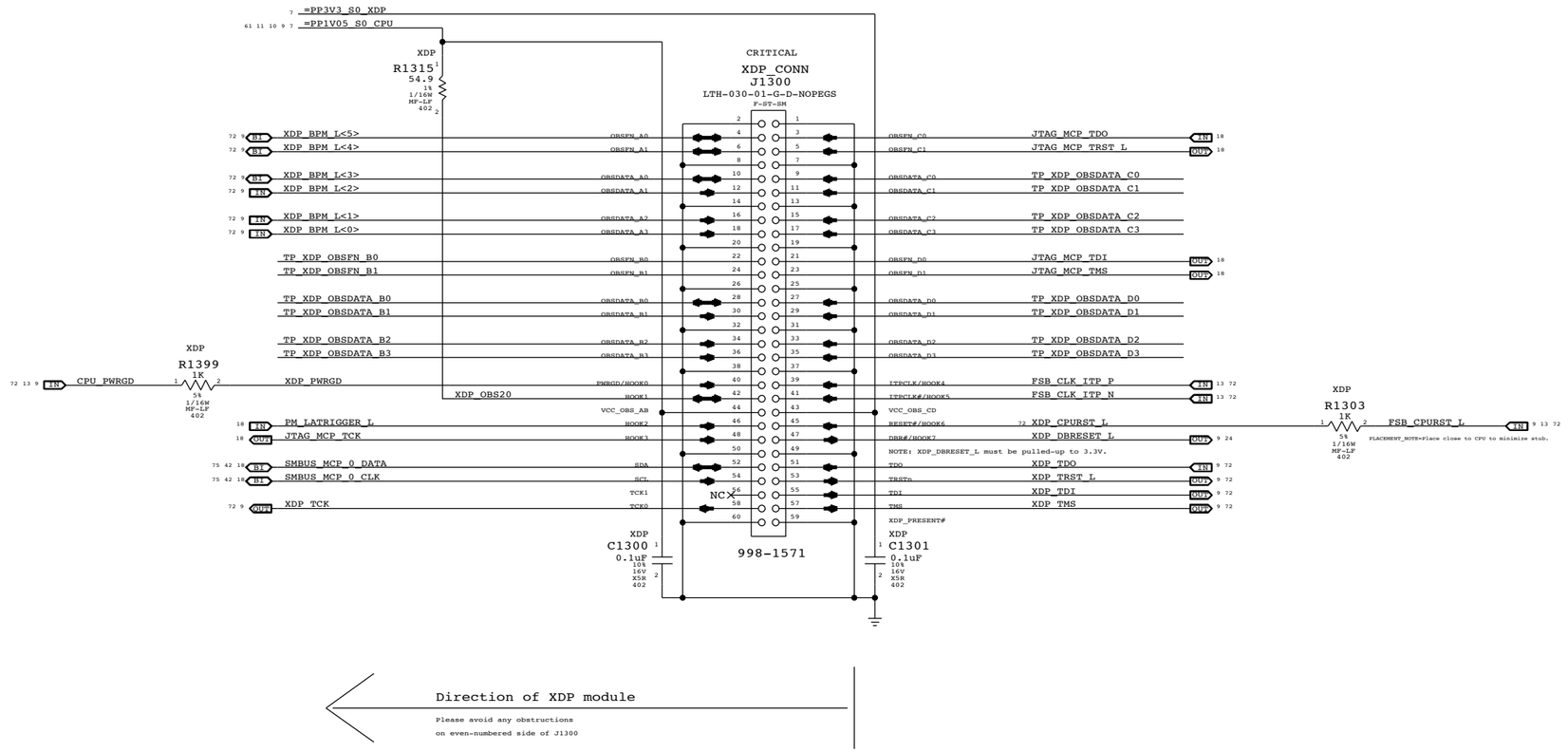
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP89-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

SYNC MASTER=T27 MLB SYNC DATE=07/28/2009

PAGE TITLE

eXtended Debug Port (mini-XDP)

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OMIT

U1400
MCP89M-A01
FBGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	K34	CPU_DSTBP0*	
FSB_DSTB_L_N<0>	K35	CPU_DSTBN0*	
FSB_DINV_L<0>	L37	CPU_DBI0*	
FSB_DSTB_L_P<1>	T31	CPU_DSTBP1*	
FSB_DSTB_L_N<1>	T30	CPU_DSTBN1*	
FSB_DINV_L<1>	P28	CPU_DBI1*	
FSB_DSTB_L_P<2>	K33	CPU_DSTBP2*	
FSB_DSTB_L_N<2>	K32	CPU_DSTBN2*	
FSB_DINV_L<2>	N35	CPU_DBI2*	
FSB_DSTB_L_P<3>	C36	CPU_DSTBP3*	
FSB_DSTB_L_N<3>	D36	CPU_DSTBN3*	
FSB_DINV_L<3>	A35	CPU_DBI3*	
FSB_A_L<3>	U38	CPU_A3*	
FSB_A_L<4>	U34	CPU_A4*	
FSB_A_L<5>	U35	CPU_A5*	
FSB_A_L<6>	T34	CPU_A6*	
FSB_A_L<7>	W37	CPU_A7*	
FSB_A_L<8>	W38	CPU_A8*	
FSB_A_L<9>	T37	CPU_A9*	
FSB_A_L<10>	Y38	CPU_A10*	
FSB_A_L<11>	W35	CPU_A11*	
FSB_A_L<12>	Y36	CPU_A12*	
FSB_A_L<13>	U33	CPU_A13*	
FSB_A_L<14>	W34	CPU_A14*	
FSB_A_L<15>	Y37	CPU_A15*	
FSB_A_L<16>	Y35	CPU_A16*	
FSB_A_L<17>	AF38	CPU_A17*	
FSB_A_L<18>	AB35	CPU_A18*	
FSB_A_L<19>	Y34	CPU_A19*	
FSB_A_L<20>	AE38	CPU_A20*	
FSB_A_L<21>	AC36	CPU_A21*	
FSB_A_L<22>	AF36	CPU_A22*	
FSB_A_L<23>	AC38	CPU_A23*	
FSB_A_L<24>	AB36	CPU_A24*	
FSB_A_L<25>	AB38	CPU_A25*	
FSB_A_L<26>	AB37	CPU_A26*	
FSB_A_L<27>	AC34	CPU_A27*	
FSB_A_L<28>	AE36	CPU_A28*	
FSB_A_L<29>	AF37	CPU_A29*	
FSB_A_L<30>	AC37	CPU_A30*	
FSB_A_L<31>	AC35	CPU_A31*	
FSB_A_L<32>	AE37	CPU_A32*	
FSB_A_L<33>	AE35	CPU_A33*	
FSB_A_L<34>	AE33	CPU_A34*	
FSB_A_L<35>	AE34	CPU_A35*	
FSB_ADSTB_L<0>	W36	CPU_ADSTB0*	
FSB_ADSTB_L<1>	AB34	CPU_ADSTB1*	
FSB_REQ_L<0>	U36	CPU_REQ0*	
FSB_REQ_L<1>	T36	CPU_REQ1*	
FSB_REQ_L<2>	U37	CPU_REQ2*	
FSB_REQ_L<3>	T38	CPU_REQ3*	
FSB_REQ_L<4>	T35	CPU_REQ4*	
FSB_ADS_L	AE31	CPU_ADS*	
FSB_BNR_L	AE32	CPU_BNR*	
FSB_BREQ0_L	AE30	CPU_BR0*	
FSB_DBSY_L	AE29	CPU_DBSY*	
FSB_DRDY_L	U29	CPU_DRDY*	
FSB_HIT_L	W32	CPU_HIT*	
FSB_HITM_L	AB31	CPU_HITM*	
FSB_LOCK_L	AC32	CPU_LOCK*	
FSB_TRDY_L	AC29	CPU_TRDY*	
CPU_PECI_MCP	AH34	CPU_PECI	
CPU_PROCHOT_L	U28	CPU_PROCHOT*	
	W33	CPU_THERMTRIP*	
CPU_FERR_L	AB32	CPU_FERR*	
=MCP_BSEL<2>	B34	CPU_BSEL2	
=MCP_BSEL<1>	C34	CPU_BSEL1	
=MCP_BSEL<0>	A34	CPU_BSEL0	
FSB_RS_L<0>	AB29	CPU_RS0*	
FSB_RS_L<1>	AC33	CPU_RS1*	
FSB_RS_L<2>	AC31	CPU_RS2*	
MCP_BCLK_VML_COMP_VDD	AH37	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AH38	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AH36	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AH35	CPU_COMP_GND	

CPU_D0*	N38	FSB_D_L<0>	
CPU_D1*	N36	FSB_D_L<1>	
CPU_D2*	P36	FSB_D_L<2>	
CPU_D3*	L36	FSB_D_L<3>	
CPU_D4*	N34	FSB_D_L<4>	
CPU_D5*	L35	FSB_D_L<5>	
CPU_D6*	D37	FSB_D_L<6>	
CPU_D7*	P38	FSB_D_L<7>	
CPU_D8*	H36	FSB_D_L<8>	
CPU_D9*	L34	FSB_D_L<9>	
CPU_D10*	K37	FSB_D_L<10>	
CPU_D11*	K36	FSB_D_L<11>	
CPU_D12*	K38	FSB_D_L<12>	
CPU_D13*	N37	FSB_D_L<13>	
CPU_D14*	H37	FSB_D_L<14>	
CPU_D15*	L38	FSB_D_L<15>	
CPU_D16*	N28	FSB_D_L<16>	
CPU_D17*	U30	FSB_D_L<17>	
CPU_D18*	N29	FSB_D_L<18>	
CPU_D19*	P34	FSB_D_L<19>	
CPU_D20*	T29	FSB_D_L<20>	
CPU_D21*	T32	FSB_D_L<21>	
CPU_D22*	U32	FSB_D_L<22>	
CPU_D23*	P33	FSB_D_L<23>	
CPU_D24*	P31	FSB_D_L<24>	
CPU_D25*	P30	FSB_D_L<25>	
CPU_D26*	N30	FSB_D_L<26>	
CPU_D27*	P33	FSB_D_L<27>	
CPU_D28*	N31	FSB_D_L<28>	
CPU_D29*	T28	FSB_D_L<29>	
CPU_D30*	P35	FSB_D_L<30>	
CPU_D31*	P29	FSB_D_L<31>	
CPU_D32*	H33	FSB_D_L<32>	
CPU_D33*	G34	FSB_D_L<33>	
CPU_D34*	L30	FSB_D_L<34>	
CPU_D35*	L31	FSB_D_L<35>	
CPU_D36*	L33	FSB_D_L<36>	
CPU_D37*	P32	FSB_D_L<37>	
CPU_D38*	N32	FSB_D_L<38>	
CPU_D39*	N33	FSB_D_L<39>	
CPU_D40*	H35	FSB_D_L<40>	
CPU_D41*	K31	FSB_D_L<41>	
CPU_D42*	H34	FSB_D_L<42>	
CPU_D43*	K30	FSB_D_L<43>	
CPU_D44*	L32	FSB_D_L<44>	
CPU_D45*	G33	FSB_D_L<45>	
CPU_D46*	H32	FSB_D_L<46>	
CPU_D47*	G35	FSB_D_L<47>	
CPU_D48*	C37	FSB_D_L<48>	
CPU_D49*	D37	FSB_D_L<49>	
CPU_D50*	H38	FSB_D_L<50>	
CPU_D51*	G38	FSB_D_L<51>	
CPU_D52*	G37	FSB_D_L<52>	
CPU_D53*	G36	FSB_D_L<53>	
CPU_D54*	B35	FSB_D_L<54>	
CPU_D55*	E35	FSB_D_L<55>	
CPU_D56*	B36	FSB_D_L<56>	
CPU_D57*	E36	FSB_D_L<57>	
CPU_D58*	C35	FSB_D_L<58>	
CPU_D59*	D34	FSB_D_L<59>	
CPU_D60*	E38	FSB_D_L<60>	
CPU_D61*	D38	FSB_D_L<61>	
CPU_D62*	E34	FSB_D_L<62>	
CPU_D63*	E37	FSB_D_L<63>	
CPU_BPRI*	Y31	FSB_BPRI_L	
CPU_DEFER*	Y30	FSB_DEFER_L	
BCLK_OUT_CPU_N	AF32	FSB_CLK_CPU_N	
BCLK_OUT_CPU_P	AF33	FSB_CLK_CPU_P	
BCLK_OUT_ITP_N	AF35	FSB_CLK_ITP_N	
BCLK_OUT_ITP_P	AF34	FSB_CLK_ITP_P	
BCLK_OUT_NB_N	AF28	FSB_CLK_MCP_N	
BCLK_OUT_NB_P	AF29	FSB_CLK_MCP_P	
BCLK_IN_P	AF30		
BCLK_IN_N	AF31		
CPU_A20M*	W30	CPU_A20M_L	
CPU_IGNNE*	AB30	CPU_IGNNE_L	
CPU_INIT*	AB28	CPU_INIT_L	
CPU_INTR	W31	CPU_INTR	
CPU_NMI	AC30	CPU_NMI	
CPU_SMI*	AC28	CPU_SMI_L	
CPU_PWRGD	Y32	CPU_PWRGD	
CPU_RESET*	AE28	FSB_CPURST_L	
CPU_DPRSLPVR	G1	PM_DPRSLPVR	
CPU_SLP*	Y33	FSB_CPUSLP_L	
CPU_DPSLP*	AB33	CPU_DPSLP_L	
CPU_DPWR*	U31	FSB_DPWR_L	
CPU_STPCLK*	Y29	CPU_STPCLK_L	
CPU_DPRSTP*	W29	CPU_DPRSTP_L	

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402

R1415 62 5% 1/16W MF-LF 402

R1430 49.9 1% 1/16W MF-LF 402

R1435 49.9 1% 1/16W MF-LF 402

R1431 49.9 1% 1/16W MF-LF 402

R1436 49.9 1% 1/16W MF-LF 402

NO STUFF
R1440 150 5% 1/16W MF-LF 402

SYNC_MASTER=T27_MLB SYNC_DATE=11/05/2009

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MEMORY PARTITION 0

MEM_A_DQ<63>	AP5	MDQ0_63	
MEM_A_DQ<62>	AP7	MDQ0_62	
MEM_A_DQ<61>	AR8	MDQ0_61	
MEM_A_DQ<60>	AP8	MDQ0_60	
MEM_A_DQ<59>	AR4	MDQ0_59	
MEM_A_DQ<58>	AR5	MDQ0_58	
MEM_A_DQ<57>	AM8	MDQ0_57	
MEM_A_DQ<56>	AN8	MDQ0_56	
MEM_A_DQ<55>	AK11	MDQ0_55	
MEM_A_DQ<54>	AL11	MDQ0_54	
MEM_A_DQ<53>	AH13	MDQ0_53	
MEM_A_DQ<52>	AH14	MDQ0_52	
MEM_A_DQ<51>	AL10	MDQ0_51	
MEM_A_DQ<50>	AK10	MDQ0_50	
MEM_A_DQ<49>	AN11	MDQ0_49	
MEM_A_DQ<48>	AJ13	MDQ0_48	
MEM_A_DQ<47>	AK13	MDQ0_47	
MEM_A_DQ<46>	AK14	MDQ0_46	
MEM_A_DQ<45>	AJ16	MDQ0_45	
MEM_A_DQ<44>	AH16	MDQ0_44	
MEM_A_DQ<43>	AJ14	MDQ0_43	
MEM_A_DQ<42>	AL13	MDQ0_42	
MEM_A_DQ<41>	AM14	MDQ0_41	
MEM_A_DQ<40>	AN14	MDQ0_40	
MEM_A_DQ<39>	AK17	MDQ0_39	
MEM_A_DQ<38>	AL17	MDQ0_38	
MEM_A_DQ<37>	AN17	MDQ0_37	
MEM_A_DQ<36>	AJ19	MDQ0_36	
MEM_A_DQ<35>	AH17	MDQ0_35	
MEM_A_DQ<34>	AJ17	MDQ0_34	
MEM_A_DQ<33>	AM16	MDQ0_33	
MEM_A_DQ<32>	AM17	MDQ0_32	
MEM_A_DQ<31>	AN26	MDQ0_31	
MEM_A_DQ<30>	AH29	MDQ0_30	
MEM_A_DQ<29>	AK29	MDQ0_29	
MEM_A_DQ<28>	AL29	MDQ0_28	
MEM_A_DQ<27>	AM25	MDQ0_27	
MEM_A_DQ<26>	AM26	MDQ0_26	
MEM_A_DQ<25>	AL28	MDQ0_25	
MEM_A_DQ<24>	AK28	MDQ0_24	
MEM_A_DQ<23>	AM28	MDQ0_23	
MEM_A_DQ<22>	AP29	MDQ0_22	
MEM_A_DQ<21>	AL31	MDQ0_21	
MEM_A_DQ<20>	AN32	MDQ0_20	
MEM_A_DQ<19>	AP28	MDQ0_19	
MEM_A_DQ<18>	AN28	MDQ0_18	
MEM_A_DQ<17>	AM31	MDQ0_17	
MEM_A_DQ<16>	AM31	MDQ0_16	
MEM_A_DQ<15>	AR34	MDQ0_15	
MEM_A_DQ<14>	AM32	MDQ0_14	
MEM_A_DQ<13>	AL33	MDQ0_13	
MEM_A_DQ<12>	AL35	MDQ0_12	
MEM_A_DQ<11>	AP32	MDQ0_11	
MEM_A_DQ<10>	AP33	MDQ0_10	
MEM_A_DQ<9>	AM35	MDQ0_9	
MEM_A_DQ<8>	AL32	MDQ0_8	
MEM_A_DQ<7>	AJ35	MDQ0_7	
MEM_A_DQ<6>	AJ31	MDQ0_6	
MEM_A_DQ<5>	AH32	MDQ0_5	
MEM_A_DQ<4>	AH33	MDQ0_4	
MEM_A_DQ<3>	AJ34	MDQ0_3	
MEM_A_DQ<2>	AL34	MDQ0_2	
MEM_A_DQ<1>	AJ33	MDQ0_1	
MEM_A_DQ<0>	AJ32	MDQ0_0	
MEM_A_DM<7>	AR7	MDQM0_7	
MEM_A_DM<6>	AM11	MDQM0_6	
MEM_A_DM<5>	AL14	MDQM0_5	
MEM_A_DM<4>	AN16	MDQM0_4	
MEM_A_DM<3>	AJ29	MDQM0_3	
MEM_A_DM<2>	AP31	MDQM0_2	
MEM_A_DM<1>	AM34	MDQM0_1	
MEM_A_DM<0>	AJ30	MDQM0_0	

MDQS0_7_P	AN7	MEM_A_DQS_P<7>	
MDQS0_7_N	AM7	MEM_A_DQS_N<7>	
MDQS0_6_P	AN10	MEM_A_DQS_P<6>	
MDQS0_6_N	AM10	MEM_A_DQS_N<6>	
MDQS0_5_P	AN13	MEM_A_DQS_P<5>	
MDQS0_5_N	AM13	MEM_A_DQS_N<5>	
MDQS0_4_P	AL16	MEM_A_DQS_P<4>	
MDQS0_4_N	AK16	MEM_A_DQS_N<4>	
MDQS0_3_P	AH28	MEM_A_DQS_P<3>	
MDQS0_3_N	AJ28	MEM_A_DQS_N<3>	
MDQS0_2_P	AM29	MEM_A_DQS_P<2>	
MDQS0_2_N	AN29	MEM_A_DQS_N<2>	
MDQS0_1_P	AP34	MEM_A_DQS_P<1>	
MDQS0_1_N	AP35	MEM_A_DQS_N<1>	
MDQS0_0_P	AH31	MEM_A_DQS_P<0>	
MDQS0_0_N	AG31	MEM_A_DQS_N<0>	

MRAS0*	AN19	MEM_A_RAS_L	
MCAS0*	AL19	MEM_A_CAS_L	
MWE0*	AL20	MEM_A_WE_L	
MBA0_2	AL25	MEM_A_BA<2>	
MBA0_1	AN20	MEM_A_BA<1>	
MBA0_0	AM19	MEM_A_BA<0>	
MA0_15	AK26	MEM_A_A<15>	
MA0_14	AK25	MEM_A_A<14>	
MA0_13	AJ20	MEM_A_A<13>	
MA0_12	AJ26	MEM_A_A<12>	
MA0_11	AH25	MEM_A_A<11>	
MA0_10	AM20	MEM_A_A<10>	
MA0_9	AH26	MEM_A_A<9>	
MA0_8	AN23	MEM_A_A<8>	
MA0_7	AJ25	MEM_A_A<7>	
MA0_6	AM22	MEM_A_A<6>	
MA0_5	AM23	MEM_A_A<5>	
MA0_4	AN22	MEM_A_A<4>	
MA0_3	AL23	MEM_A_A<3>	
MA0_2	AK22	MEM_A_A<2>	
MA0_1	AK23	MEM_A_A<1>	
MA0_0	AL22	MEM_A_A<0>	

=PP1V05_S0_MCP_M2CLK_DLL

+VIO_M2CLK_DLL_1	AF24	550 mA
+VIO_M2CLK_DLL_2	AG25	

PP1V05_S0_MCP_PLL_FSBMEM

+VIO_PLL_MEM_1	AF25	20 mA
+VIO_PLL_MEM_2	AG26	
+VIO_PLL_FSB_1	AF26	25 mA
+VIO_PLL_FSB_2	AG28	
+VIO_PLL_CPU_1	AC26	25 mA
+VIO_PLL_CPU_2	AD26	
+VIO_PLL_CPU_3	AE26	
+VIO_PLL_CPU_4	AF27	

70 mA

MCLK0A_1_P	AH23	MEM_A_CLK_P<1>	
MCLK0A_1_N	AJ23	MEM_A_CLK_N<1>	
MCLK0A_0_P	AJ22	MEM_A_CLK_P<0>	
MCLK0A_0_N	AH22	MEM_A_CLK_N<0>	
MCS0A_1*	AH19	MEM_A_CS_L<1>	
MCS0A_0*	AK20	MEM_A_CS_L<0>	
MODT0A_1	AH20	MEM_A_ODT<1>	
MODT0A_0	AK19	MEM_A_ODT<0>	
MCKE0A_1	AL26	MEM_A_CKE<1>	
MCKE0A_0	AN25	MEM_A_CKE<0>	

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MEMORY PARTITION 1

MEM_B_DQ<63>	AP1	MDQ1_63	
MEM_B_DQ<62>	AR3	MDQ1_62	
MEM_B_DQ<61>	AV4	MDQ1_61	
MEM_B_DQ<60>	AU4	MDQ1_60	
MEM_B_DQ<59>	AP3	MDQ1_59	
MEM_B_DQ<58>	AP2	MDQ1_58	
MEM_B_DQ<57>	AU3	MDQ1_57	
MEM_B_DQ<56>	AT4	MDQ1_56	
MEM_B_DQ<55>	AT5	MDQ1_55	
MEM_B_DQ<54>	AT7	MDQ1_54	
MEM_B_DQ<53>	AU8	MDQ1_53	
MEM_B_DQ<52>	AR10	MDQ1_52	
MEM_B_DQ<51>	AV5	MDQ1_51	
MEM_B_DQ<50>	AU5	MDQ1_50	
MEM_B_DQ<49>	AP10	MDQ1_49	
MEM_B_DQ<48>	AT8	MDQ1_48	
MEM_B_DQ<47>	AT10	MDQ1_47	
MEM_B_DQ<46>	AU10	MDQ1_46	
MEM_B_DQ<45>	AR13	MDQ1_45	
MEM_B_DQ<44>	AR14	MDQ1_44	
MEM_B_DQ<43>	AR11	MDQ1_43	
MEM_B_DQ<42>	AP11	MDQ1_42	
MEM_B_DQ<41>	AT11	MDQ1_41	
MEM_B_DQ<40>	AP13	MDQ1_40	
MEM_B_DQ<39>	AV14	MDQ1_39	
MEM_B_DQ<38>	AU14	MDQ1_38	
MEM_B_DQ<37>	AR17	MDQ1_37	
MEM_B_DQ<36>	AP17	MDQ1_36	
MEM_B_DQ<35>	AP14	MDQ1_35	
MEM_B_DQ<34>	AT13	MDQ1_34	
MEM_B_DQ<33>	AP16	MDQ1_33	
MEM_B_DQ<32>	AR16	MDQ1_32	
MEM_B_DQ<31>	AU26	MDQ1_31	
MEM_B_DQ<30>	AT26	MDQ1_30	
MEM_B_DQ<29>	AU29	MDQ1_29	
MEM_B_DQ<28>	AT29	MDQ1_28	
MEM_B_DQ<27>	AV25	MDQ1_27	
MEM_B_DQ<26>	AV26	MDQ1_26	
MEM_B_DQ<25>	AV28	MDQ1_25	
MEM_B_DQ<24>	AV29	MDQ1_24	
MEM_B_DQ<23>	AT31	MDQ1_23	
MEM_B_DQ<22>	AR32	MDQ1_22	
MEM_B_DQ<21>	AT34	MDQ1_21	
MEM_B_DQ<20>	AU34	MDQ1_20	
MEM_B_DQ<19>	AR29	MDQ1_19	
MEM_B_DQ<18>	AR31	MDQ1_18	
MEM_B_DQ<17>	AU32	MDQ1_17	
MEM_B_DQ<16>	AT32	MDQ1_16	
MEM_B_DQ<15>	AV35	MDQ1_15	
MEM_B_DQ<14>	AT35	MDQ1_14	
MEM_B_DQ<13>	AR37	MDQ1_13	
MEM_B_DQ<12>	AP38	MDQ1_12	
MEM_B_DQ<11>	AV34	MDQ1_11	
MEM_B_DQ<10>	AU35	MDQ1_10	
MEM_B_DQ<9>	AR36	MDQ1_9	
MEM_B_DQ<8>	AR38	MDQ1_8	
MEM_B_DQ<7>	AM36	MDQ1_7	
MEM_B_DQ<6>	AM37	MDQ1_6	
MEM_B_DQ<5>	AJ36	MDQ1_5	
MEM_B_DQ<4>	AL36	MDQ1_4	
MEM_B_DQ<3>	AP37	MDQ1_3	
MEM_B_DQ<2>	AP36	MDQ1_2	
MEM_B_DQ<1>	AJ38	MDQ1_1	
MEM_B_DQ<0>	AJ37	MDQ1_0	
MEM_B_DM<7>	AT2	MDQM1_7	
MEM_B_DM<6>	AU7	MDQM1_6	
MEM_B_DM<5>	AV10	MDQM1_5	
MEM_B_DM<4>	AT14	MDQM1_4	
MEM_B_DM<3>	AR28	MDQM1_3	
MEM_B_DM<2>	AV32	MDQM1_2	
MEM_B_DM<1>	AT37	MDQM1_1	
MEM_B_DM<0>	AM38	MDQM1_0	

MDQS1_7_P	AR2	MEM_B_DQS_P<7>	
MDQS1_7_N	AR1	MEM_B_DQS_N<7>	
MDQS1_6_P	AV7	MEM_B_DQS_P<6>	
MDQS1_6_N	AV8	MEM_B_DQS_N<6>	
MDQS1_5_P	AU11	MEM_B_DQS_P<5>	
MDQS1_5_N	AV11	MEM_B_DQS_N<5>	
MDQS1_4_P	AU13	MEM_B_DQS_P<4>	
MDQS1_4_N	AV13	MEM_B_DQS_N<4>	
MDQS1_3_P	AT28	MEM_B_DQS_P<3>	
MDQS1_3_N	AU28	MEM_B_DQS_N<3>	
MDQS1_2_P	AU31	MEM_B_DQS_P<2>	
MDQS1_2_N	AV31	MEM_B_DQS_N<2>	
MDQS1_1_P	AU36	MEM_B_DQS_P<1>	
MDQS1_1_N	AT36	MEM_B_DQS_N<1>	
MDQS1_0_P	AL38	MEM_B_DQS_P<0>	
MDQS1_0_N	AL37	MEM_B_DQS_N<0>	

MRAS1*	AR19	MEM_B_RAS_L	
MCAS1*	AU17	MEM_B_CAS_L	
MWE1*	AT17	MEM_B_WE_L	
MBA1_2	AR25	MEM_B_BA<2>	
MBA1_1	AT19	MEM_B_BA<1>	
MBA1_0	AR20	MEM_B_BA<0>	
MA1_15	AP26	MEM_B_A<15>	
MA1_14	AR26	MEM_B_A<14>	
MA1_13	AV16	MEM_B_A<13>	
MA1_12	AP25	MEM_B_A<12>	
MA1_11	AT23	MEM_B_A<11>	
MA1_10	AP20	MEM_B_A<10>	
MA1_9	AU23	MEM_B_A<9>	
MA1_8	AV22	MEM_B_A<8>	
MA1_7	AV23	MEM_B_A<7>	
MA1_6	AT22	MEM_B_A<6>	
MA1_5	AU22	MEM_B_A<5>	
MA1_4	AP23	MEM_B_A<4>	
MA1_3	AR23	MEM_B_A<3>	
MA1_2	AP22	MEM_B_A<2>	
MA1_1	AR22	MEM_B_A<1>	
MA1_0	AT20	MEM_B_A<0>	

=PP1V5R1V35_S3_MCP_MEM

R1520
1K
5%
1/16W
MF-LF
402

MRESET0*	AP4	MEM_RESET_L	
MCLK1A_1_P	AU20	MEM_B_CLK_P<1>	
MCLK1A_1_N	AV20	MEM_B_CLK_N<1>	
MCLK1A_0_P	AU19	MEM_B_CLK_P<0>	
MCLK1A_0_N	AV19	MEM_B_CLK_N<0>	
MCS1A_1*	AU16	MEM_B_CS_L<1>	
MCS1A_0*	AP19	MEM_B_CS_L<0>	
MODT1A_1	AT16	MEM_B_ODT<1>	
MODT1A_0	AV17	MEM_B_ODT<0>	
MCKE1A_1	AU25	MEM_B_CKE<1>	
MCKE1A_0	AT25	MEM_B_CKE<0>	

=PP1V5R1V35_SW_MCP_MEM

R1510
40.2
1%
1/16W
MF-LF
402

R1511
40.2
1%
1/16W
MF-LF
402

MCP_MEM_COMP_GND	AG23	MEM_COMP_GND
MCP_MEM_COMP_VDD	AG22	MEM_COMP_VDD

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=08/06/2009

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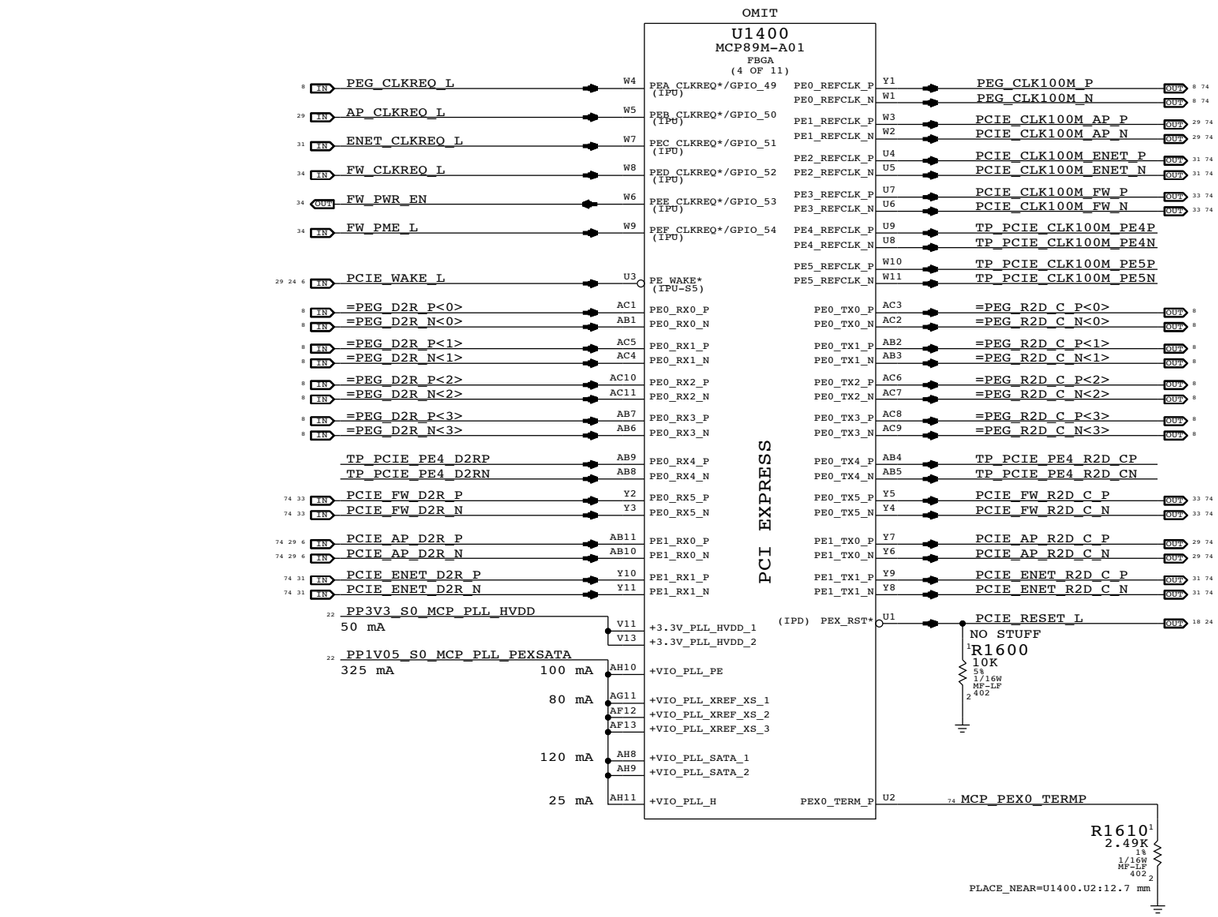

PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,
+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB SYNC DATE=11/05/2009

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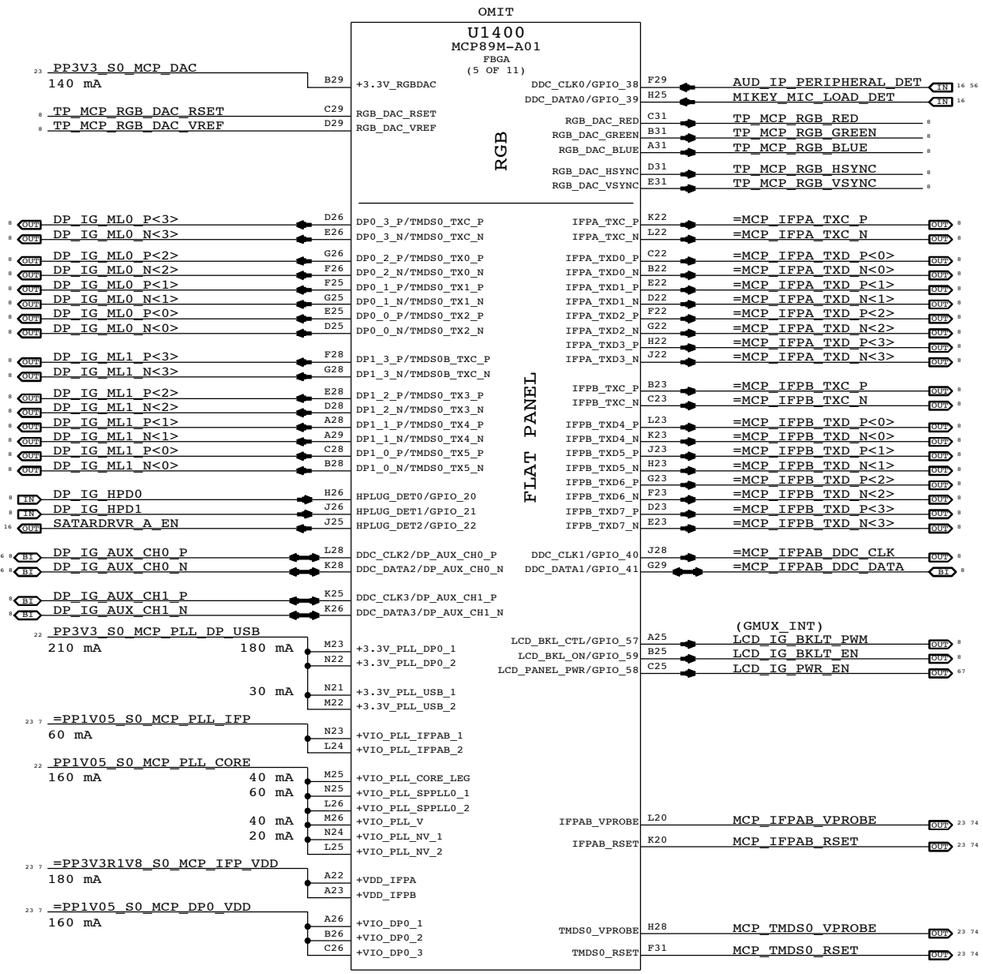

NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

	Interface Mode	
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

R1710 100K 5% 1/16W MF-LF 402 DP_IG_AUX_CH0_P
R1711 100K 5% 1/16W MF-LF 402 DP_IG_AUX_CH0_N

GPIO Pull-Ups

=PP3V3_S0_MCP_GPIO

R1780 10K 5% 1/16W MF-LF 402 SATARDRVR_A_EN
R1781 10K 5% 1/16W MF-LF 402 AUD_IP_PERIPHERAL_DET
R1782 10K 5% 1/16W MF-LF 402 MIKEY_MIC_LOAD_DET

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=11/05/2009

PAGE TITLE: MCP Graphics

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D
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BRANCH:
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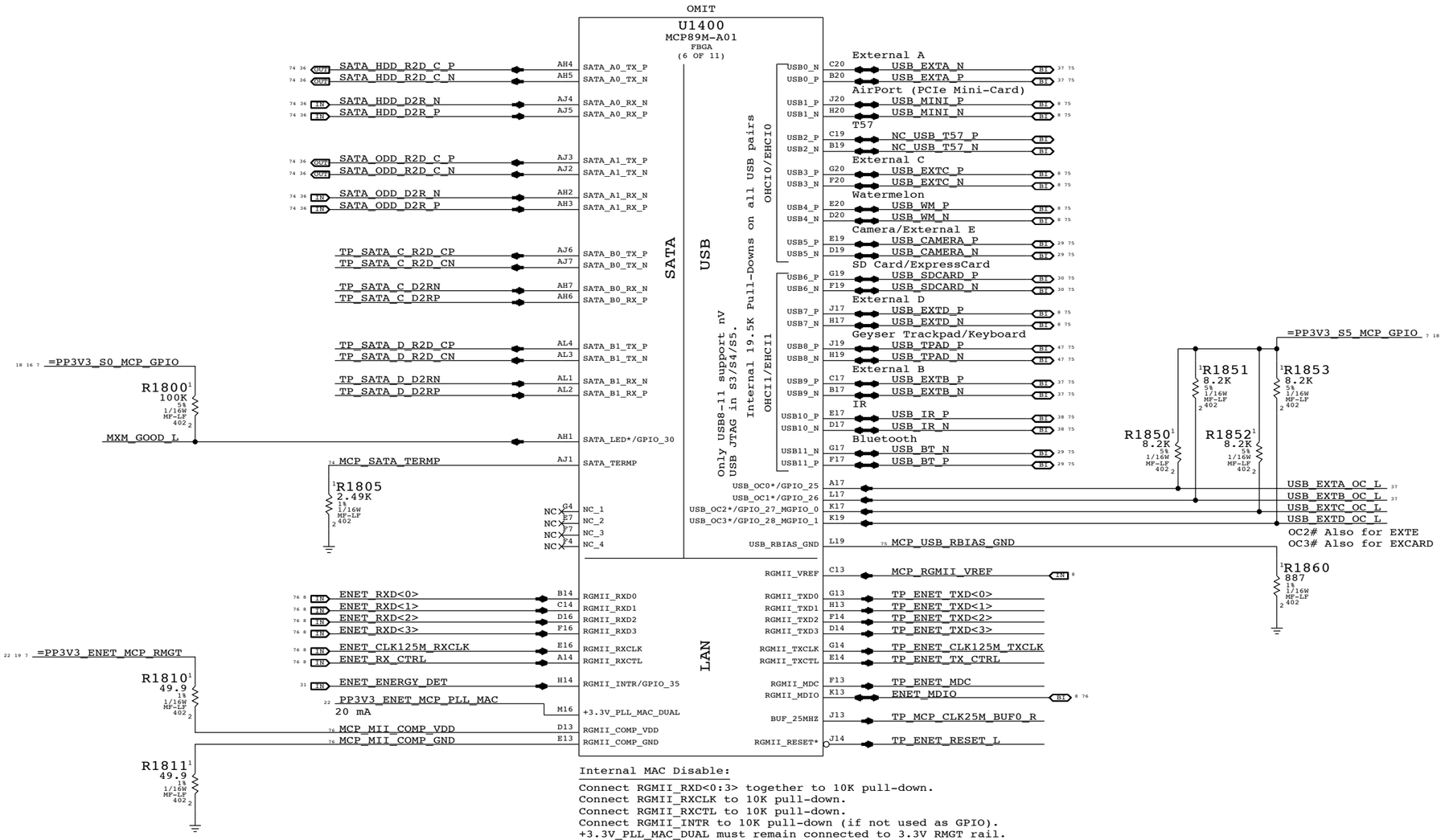

Internal MAC Disable:

Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB SYNC DATE=11/23/2009

PAGE TITLE
MCP SATA, USB & Ethernet

Apple Inc.

DRAWING NUMBER 051-8563
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REVISION A.13.0
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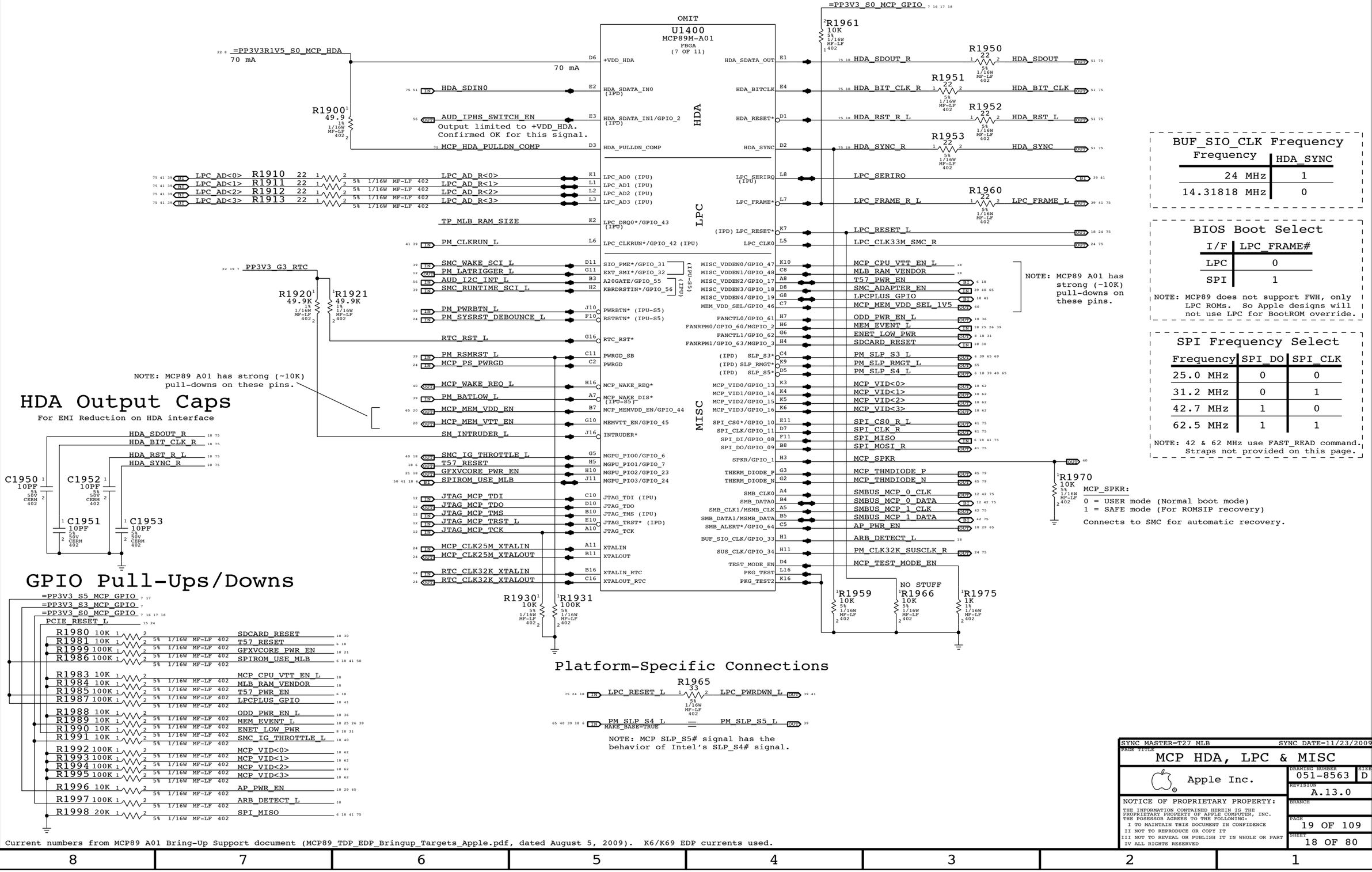

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB | SYNC DATE=11/23/2009

PAGE TITLE: MCP HDA, LPC & MISC

Apple Inc.

DRAWING NUMBER: 051-8563 | SIZE: D

REVISION: A.13.0

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NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.

OMIT

U1400
MCP89M-A01
FBGA
(8 OF 11)
POWER I

22 7 =PP1V05_SW_MCP_FSB
2000 mA

G32	+VTT_CPU_1	+VDD_MEM_1	AG14
K29	+VTT_CPU_2	+VDD_MEM_2	AL7
D32	+VTT_CPU_3	+VDD_MEM_3	AF18
L29	+VTT_CPU_4	+VDD_MEM_4	AF21
Y26	+VTT_CPU_5	+VDD_MEM_5	AM1
V26	+VTT_CPU_6	+VDD_MEM_6	AM4
P27	+VTT_CPU_7	+VDD_MEM_7	AK8
T27	+VTT_CPU_8	+VDD_MEM_8	AG13
J29	+VTT_CPU_9	+VDD_MEM_9	AF16
N27	+VTT_CPU_10	+VDD_MEM_10	AF22
P26	+VTT_CPU_11	+VDD_MEM_11	AG20
F32	+VTT_CPU_12	+VDD_MEM_12	AM5
A32	+VTT_CPU_13	+VDD_MEM_13	AG19
H29	+VTT_CPU_14	+VDD_MEM_14	AF23
W26	+VTT_CPU_15	+VDD_MEM_15	AJ9
U27	+VTT_CPU_16	+VDD_MEM_16	AF19
G31	+VTT_CPU_17	+VDD_MEM_17	AG17
C32	+VTT_CPU_18	+VDD_MEM_18	AL6
B32	+VTT_CPU_19	+VDD_MEM_19	AG16
M28	+VTT_CPU_20	+VDD_MEM_20	AH12
H30	+VTT_CPU_21	+VDD_MEM_21	AM2
U26	+VTT_CPU_22	+VDD_MEM_22	AF15
T26	+VTT_CPU_23	+VDD_MEM_23	AM3
H31	+VTT_CPU_24	+VDD_MEM_24	AL5
B32	+VTT_CPU_25	+VDD_MEM_25	AL8
R26	+VTT_CPU_26	+VDD_MEM_26	AF17
N26	+VTT_CPU_27	+VDD_MEM_27	AJ11
		+VDD_MEM_28	AJ8
		+VDD_MEM_29	AF14
		+VDD_MEM_30	AJ10
		+VDD_MEM_31	AF20

22 13 7 =PP1V05_S0_MCP_FSB
200 mA

W27	+VTT_CPU2_1		
W28	+VTT_CPU2_2		
Y27	+VTT_CPU2_3		
Y28	+VTT_CPU2_4		

=PP1V5R1V35_SW_MCP_MEM 14 20 22
4300 mA

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U1400
MCP89M-A01
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POWER II

22 7 =PPVCORE_S0_MCP
8450 mA (0.85V)

T3	+VDD_COREA_1	+VDD_COREB_1	M4
AB22	+VDD_COREA_2	+VDD_COREB_2	M2
AB20	+VDD_COREA_3	+VDD_COREB_3	P4
R13	+VDD_COREA_4	+VDD_COREB_4	N12
R7	+VDD_COREA_5	+VDD_COREB_5	N4
T6	+VDD_COREA_6	+VDD_COREB_6	N14
T13	+VDD_COREA_7	+VDD_COREB_7	V20
R11	+VDD_COREA_8	+VDD_COREB_8	N10
AB17	+VDD_COREA_9	+VDD_COREB_9	P3
R10	+VDD_COREA_10	+VDD_COREB_10	P1
AB18	+VDD_COREA_11	+VDD_COREB_11	N11
T1	+VDD_COREA_12	+VDD_COREB_12	N6
T2	+VDD_COREA_13	+VDD_COREB_13	P6
AB21	+VDD_COREA_14	+VDD_COREB_14	N2
R4	+VDD_COREA_15	+VDD_COREB_15	N9
AB19	+VDD_COREA_16	+VDD_COREB_16	N8
P13	+VDD_COREA_17	+VDD_COREB_17	M10
R2	+VDD_COREA_18	+VDD_COREB_18	N3
T8	+VDD_COREA_19	+VDD_COREB_19	N1
R8	+VDD_COREA_20	+VDD_COREB_20	M5
T4	+VDD_COREA_21	+VDD_COREB_21	M7
R5	+VDD_COREA_22	+VDD_COREB_22	P2
T7	+VDD_COREA_23	+VDD_COREB_23	M8
T5	+VDD_COREA_24	+VDD_COREB_24	M11
T9	+VDD_COREA_25	+VDD_COREB_25	V19
U22	+VDD_COREA_26	+VDD_COREB_26	N7
V22	+VDD_COREA_27	+VDD_COREB_27	N16
W22	+VDD_COREA_28	+VDD_COREB_28	P5
Y22	+VDD_COREA_29	+VDD_COREB_29	N5
AA22	+VDD_COREA_30	+VDD_COREB_30	N13
P12	+VDD_COREA_31	+VDD_COREB_31	N15
P10	+VDD_COREA_32	+VDD_COREB_32	P9
P11	+VDD_COREA_33	+VDD_COREB_33	V17
		+VDD_COREB_34	V18
		+VDD_COREB_35	M14
		+VDD_COREB_36	M13
		+VDD_COREB_37	Y19
		+VDD_COREB_38	Y20
		+VDD_COREB_39	Y17
		+VDD_COREB_40	Y18
		+VDD_COREB_41	P7
		+VDD_COREB_42	P8

=PPVCORE_SW_MCP_GFX 21 23
15350 mA (0.85V)

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators.
Instead connect regulator sense point as close to COREB FET as possible.

TP_MCP_VDDCOREA_SENSEP L10 +VDD_COREA_SENSE
TP_MCP_VDDCOREA_SENSEN L9 GND_COREA_SENSE

7 =PP1V05_S0_MCP_PE_DVDD0
200 mA (DVDD0 & DVDD1)
(PE0[3:0])

AF7	+VIO_PE_DVDD0_1	
AF8	+VIO_PE_DVDD0_2	
AE9	+VIO_PE_DVDD0_3	
AE10	+VIO_PE_DVDD0_4	

7 =PP1V05_S0_MCP_PE_DVDD1
200 mA (DVDD0 & DVDD1)
(PE0[5:4], PE1[1:0])

AE6	+VIO_PE_DVDD1_1	
AE7	+VIO_PE_DVDD1_2	
AE8	+VIO_PE_DVDD1_3	

7 =PP1V05_S0_MCP_PE_AVDD0
500 mA (AVDD0 & AVDD1)
(PE0[3:0])

AC13	+VIO_PE_AVDD0_1	
AB12	+VIO_PE_AVDD0_2	
AC12	+VIO_PE_AVDD0_3	
AD11	+VIO_PE_AVDD0_4	
AD13	+VIO_PE_AVDD0_5	
AB13	+VIO_PE_AVDD0_6	

7 =PP1V05_S0_MCP_PE_AVDD1
500 mA (AVDD0 & AVDD1)
(PE0[5:4], PE1[1:0])

Y12	+VIO_PE_AVDD1_1	
Y13	+VIO_PE_AVDD1_2	
AA13	+VIO_PE_AVDD1_3	
W12	+VIO_PE_AVDD1_4	
W13	+VIO_PE_AVDD1_5	

22 7 =PP3V3_S0_MCP_HVDD
30 mA

T11	+3.3V_HVDD_1	
T12	+3.3V_HVDD_2	
U13	+3.3V_HVDD_3	

22 7 =PP3V3_S0_MCP
250 mA

U11	+3.3V_1	
U12	+3.3V_2	
F5	+3.3V_3	
E29	+3.3V_4	
E5	+3.3V_5	

22 7 =PP0V9_S5_MCP_VDD_AUXC
150 mA

L11	+VDD_DUAL_AUXC_1	
M17	+VDD_DUAL_AUXC_2	
M20	+VDD_DUAL_AUXC_3	

22 18 7 PP3V3_G3_RTC
?? uA (G3)
5 mA (S0)

A16	+3.3V_VBAT	

U10	+VDD_COREB_SENSE	TP_MCP_VDDCOREB_SENSEP	
T10	GND_COREB_SENSE	TP_MCP_VDDCOREB_SENSEN	
AE1	+VIO_SATA_AVDD_1	PP1V05_S0_MCP_SATA_AVDD 22 300 mA	
AE2	+VIO_SATA_AVDD_2		
AE3	+VIO_SATA_AVDD_3		
AE4	+VIO_SATA_AVDD_4		
AE5	+VIO_SATA_AVDD_5		
AF1	+VIO_SATA_DVDD_1	=PP1V05_S0_MCP_SATA_DVDD 7 22 100 mA	
AF2	+VIO_SATA_DVDD_2		
AF3	+VIO_SATA_DVDD_3		
AF4	+VIO_SATA_DVDD_4		
AF5	+VIO_SATA_DVDD_5		
AF6	+VIO_SATA_DVDD_6		
AF9	+VIO_SATA_DVDD_7		
AF10	+VIO_SATA_DVDD_8		
AF11	+VIO_SATA_DVDD_9		
AE11	+VIO_SATA_DVDD_10		
AE12	+VIO_SATA_DVDD_11		
AE13	+VIO_SATA_DVDD_12		
L12	+VDD_DUAL_RMGT_1	=PP0V9_ENET_MCP_RMGT 7 22 140 mA	
L13	+VDD_DUAL_RMGT_2		
A13	+3.3V_DUAL_RMGT_1	=PP3V3_ENET_MCP_RMGT 7 17 22 300 mA	
B13	+3.3V_DUAL_RMGT_2		
A20	+3.3V_DUAL_USB_1	=PP3V3_S5_MCP 7 22 240 mA	
A19	+3.3V_DUAL_USB_2		
F8	+3.3V_DUAL_1	40 mA	
E8	+3.3V_DUAL_2		

OMIT

U1400
MCP89M-A01
FBGA
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GND

AP21	GND_1	GND_68	AD7
M37	GND_2	GND_69	B12
AM21	GND_3	GND_70	D12
AU37	GND_4	GND_71	E12
AC27	GND_5	GND_72	G12
D18	GND_6	GND_73	A2
B1	GND_7	GND_74	AL12
AD5	GND_8	GND_75	AM6
J2	GND_9	GND_76	AD37
AT1	GND_10	GND_77	AG32
AM30	GND_11	GND_78	H12
C1	GND_12	GND_79	AR35
AT3	GND_13	GND_80	H9
AP24	GND_14	GND_81	G24
AM33	GND_15	GND_82	V10
AE27	GND_16	GND_83	V5
AJ24	GND_17	GND_84	AL30
AH18	GND_18	GND_85	G7
AA8	GND_19	GND_86	V29
AM18	GND_20	GND_87	AP15
B6	GND_21	GND_88	AN2
J32	GND_22	GND_89	AJ12
AJ21	GND_23	GND_90	AR15
AK35	GND_24	GND_91	N20
H15	GND_25	GND_92	D21
D33	GND_26	GND_93	E21
B18	GND_27	GND_94	G21
M32	GND_28	GND_95	H21
B2	GND_29	GND_96	AR27
E6	GND_30	GND_97	AM27
J5	GND_31	GND_98	AP27
K18	GND_32	GND_99	AM15
AN34	GND_33	GND_100	AA31
AD10	GND_34	GND_101	AM9
F34	GND_35	GND_102	AH24
V8	GND_36	GND_103	K12
R35	GND_37	GND_104	J31
AR9	GND_38	GND_105	E30
AA2	GND_39	GND_106	AK7
AA10	GND_40	GND_107	V7
R32	GND_41	GND_108	M31
AG29	GND_42	GND_109	AU12
H8	GND_43	GND_110	AP6
AP12	GND_44	GND_111	B37
AM12	GND_45	GND_112	A36
AH21	GND_46	GND_113	F35
V32	GND_47	GND_114	L27
AR33	GND_48	GND_115	D35
J7	GND_49	GND_116	AL24
AA32	GND_50	GND_117	AP30
AG34	GND_51	GND_118	AH15
AK37	GND_52	GND_119	B21
K24	GND_53	GND_120	AV3
K21	GND_54	GND_121	AT38
J8	GND_55	GND_122	B38
AG8	GND_56	GND_123	AA21
AN5	GND_57	GND_124	AD4
V2	GND_58	GND_125	A37
AD32	GND_59	GND_126	AP18
AD2	GND_60	GND_127	AN4
D15	GND_61	GND_128	B24
AG2	GND_62	GND_129	D30
L15	GND_63	GND_130	V4
AK32	GND_64	GND_131	AA7
AR12	GND_65	GND_132	AD34
AN35	GND_66	GND_133	AK4
AN37	GND_67	GND_134	R37

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U1400
MCP89M-A01
FBGA
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GND

AU24	GND_135	GND_200	E33
AU15	GND_136	GND_201	M35
AG5	GND_137	GND_202	AV2
AD35	GND_138	GND_203	AK2
AJ18	GND_139	GND_204	AU6
AL18	GND_140	GND_205	F37
AR24	GND_141	GND_206	C3
AA5	GND_142	GND_207	J37
G18	GND_143	GND_208	V35
B9	GND_144	GND_209	G27
AU9	GND_145	GND_210	AA35
AM24	GND_146	GND_211	AU18
H24	GND_147	GND_212	AR6
B30	GND_148	GND_213	AV36
AR21	GND_149	GND_214	B33
D24	GND_150	GND_215	AJ27
AU30	GND_151	GND_216	G9
AK5	GND_152	GND_217	AG35
N18	GND_153	GND_218	AG7
E24	GND_154	GND_219	AD8
K15	GND_155	GND_220	AU2
M19	GND_156	GND_221	AP9
AH27	GND_157	GND_222	AD31
E18	GND_158	GND_223	V37
AA34	GND_159	GND_224	AA37
AK31	GND_160	GND_225	AG37
K11	GND_161	GND_226	AL15
AU21	GND_162	GND_227	AR18
V34	GND_163	GND_228	L14
AL21	GND_164	GND_229	K14
AA11	GND_165	GND_230	F2
M34	GND_166	GND_231	K27
B27	GND_167	GND_232	AL9
V28	GND_168	GND_233	AB26
C38	GND_169	GND_234	M29
D27	GND_170	GND_235	G30
R34	GND_171	GND_236	R28
J35	GND_172	GND_237	R29
AK34	GND_173	GND_238	R31
E15	GND_174	GND_239	U17
AR30	GND_175	GND_240	K8
AU33	GND_176	GND_241	Y21
J34	GND_177	GND_242	V31
AH30	GND_178	GND_243	U18
J4	GND_179	GND_244	W21
AU27	GND_180	GND_245	U19
AU1	GND_181	GND_246	W18
AG10	GND_182	GND_247	U20
E9	GND_183	GND_248	W17
E27	GND_184	GND_249	V21
L21	GND_185	GND_250	AA28
AU38	GND_186	GND_251	AA29
H18	GND_187	GND_252	N17
B15	GND_188	GND_253	AD28
AA4	GND_189	GND_254	AD29
AJ15	GND_190	GND_255	AG4
L18	GND_191	GND_256	W19
A3	GND_192	GND_257	W20
G15	GND_193	GND_258	AA26
AL27	GND_194	GND_259	AB27
AV37	GND_195	GND_260	AA17
D9	GND_196	GND_261	AA18
L4	GND_197	GND_262	AA19
N19	GND_198	GND_263	AA20
H27	GND_199	GND_264	U21

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB SYNC DATE=08/06/2009

PAGE TITLE
MCP Power & Ground

Apple Inc.

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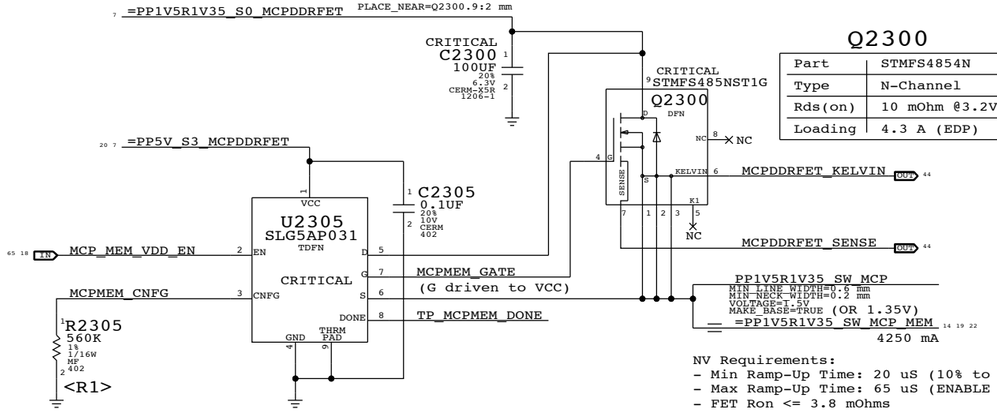
C2300 helps reduce input rail
droop during Q2300 turn-on.



Q2300

Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)

Approx. Ramp Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1(Kohms)

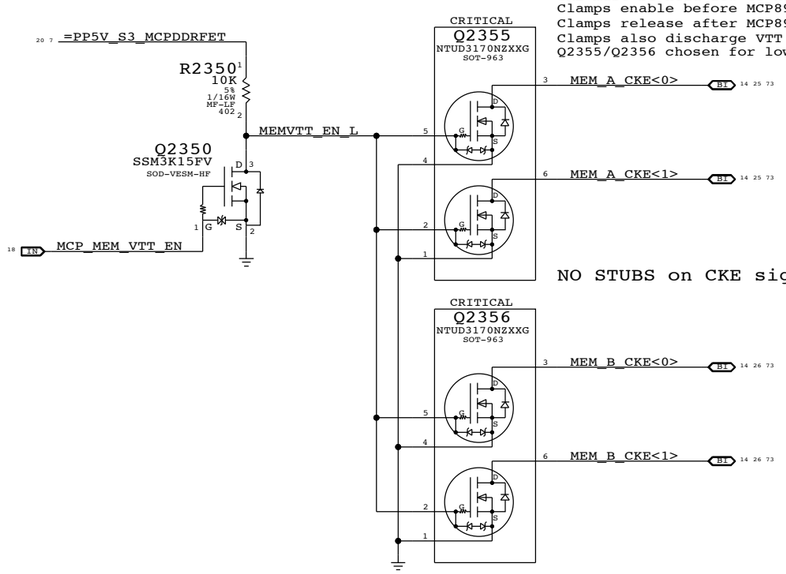
NV Requirements:
- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.



SYNC MASTER=T27 MLB SYNC DATE=11/23/2009

PAGE TITLE
MCP89 Memory Rail Gating

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D
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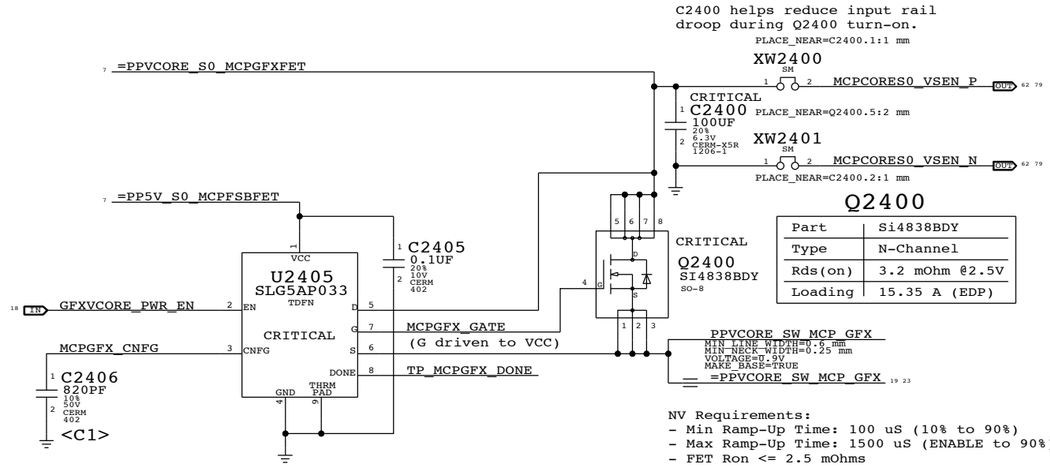

C2400 helps reduce input rail droop during Q2400 turn-on.

PLACE_NEAR=C2400.1:1 mm

Q2400

Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

SYNC_MASTER=T27_MLB SYNC_DATE=11/23/2009

PAGE TITLE
MCP89 GFX Core Rail Gating

Apple Inc.

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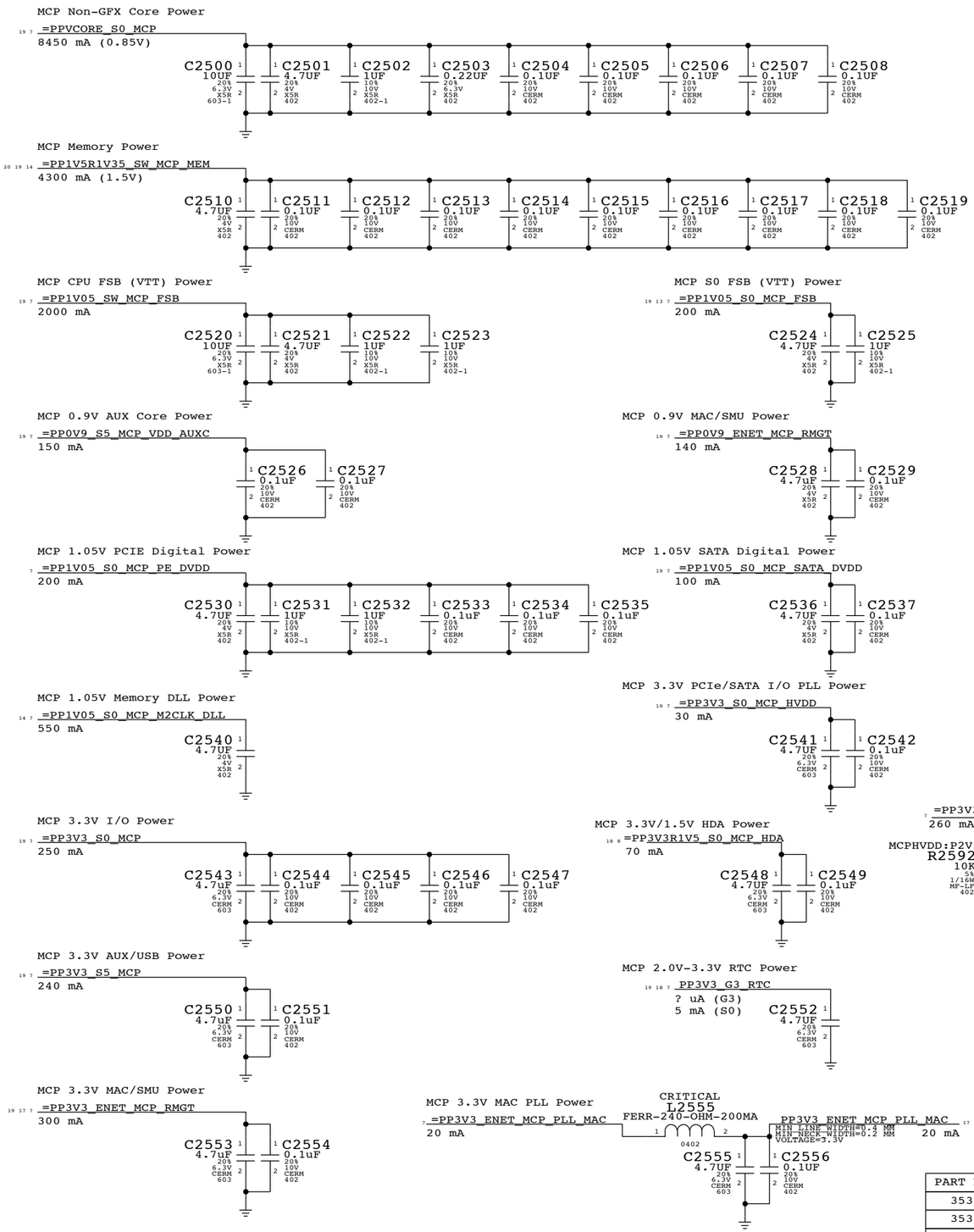

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2971	1	IC,LDO,MIC5365,2.5V,150MA,2%,SC70-5,HFLF	U2592	CRITICAL	LDO:FIXED
353S2979	1	IC,LDO,TPS717,ADJ,150MA,3%,SC70,HFLF	U2592	CRITICAL	LDO:ADJ
116S0004	1	RES,0402,0,5%,1/16W	R2596	CRITICAL	HTOL_SENSE:NO

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=08/15/2009

PAGE TITLE
MCP Standard Decoupling

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D
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MCP GFX Core Power

=PPVCORE_SW_MCP_GFX
15350 mA (0.85V)

C2600 10UF 20% 6.3V X5R 603-1
C2601 4.7UF 20% 4V X5R 402
C2602 1UF 10% 10V X5R 402-1
C2603 1UF 10% 10V X5R 402-1
C2604 0.22UF 20% 6.3V X5R 402
C2605 0.22UF 20% 6.3V X5R 402
C2606 0.1UF 20% 10V CERM 402
C2607 0.1UF 20% 10V CERM 402
C2608 0.1UF 20% 10V CERM 402
C2609 0.1UF 20% 10V CERM 402
C2610 0.1UF 20% 10V CERM 402
C2611 0.1UF 20% 10V CERM 402
C2612 0.1UF 20% 10V CERM 402

MCP 3.3V RGBDAC Power

GND_MCP_DAC_P3V3 = PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
MAKE_BASE=TRUE
140 mA

R2670 0 5% 1/16W MF-LF 402

If RGBDAC is used, requires ferrite (155S0382) plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.

If RGBDAC is not used, tie to GND.

MCP 3.3V/1.8V IFP Interface Power

=PP3V3R1V8_S0_MCP_IFP_VDD
180 mA (1.8V LVDS)

C2620 4.7uF 20% 6.3V CERM 603
C2621 0.1uF 20% 10V CERM 402

MCP 1.05V IFP PLL Power

=PP1V05_S0_MCP_PLL_IFP
60 mA

C2630 4.7uF 20% 4V X5R 402
C2631 0.1uF 20% 10V CERM 402

MCP 1.05V DisplayPort Power

=PP1V05_S0_MCP_DP0_VDD
160 mA

C2640 4.7UF 20% 4V X5R 402
C2641 0.1uF 20% 10V CERM 402

MCP_TMDS0_RSET
MCP_TMDS0_VPROBE

NO STUFF
C2650 0.1UF 20% 10V CERM 402
R2650 1K 1% 1/16W MF-LF 402

MCP_IFPAB_RSET
MCP_IFPAB_VPROBE

NO STUFF
C2655 0.1UF 20% 10V CERM 402
NO STUFF
R2655 1K 1% 1/16W MF-LF 402

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB SYNC DATE=08/06/2009

PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D
REVISION: A.13.0
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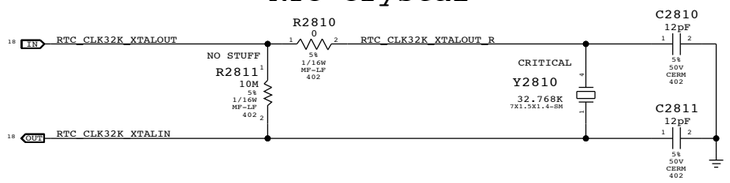
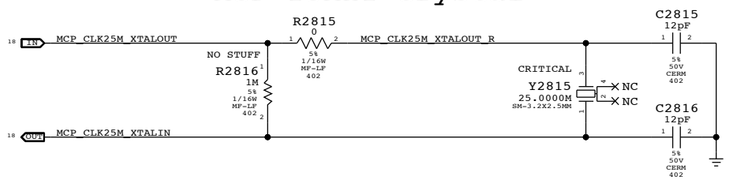
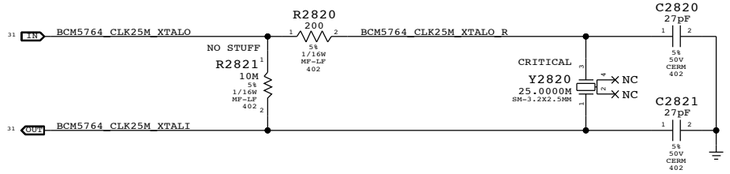
RTC Crystal



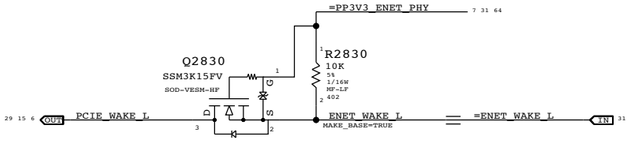
MCP 25MHz Crystal



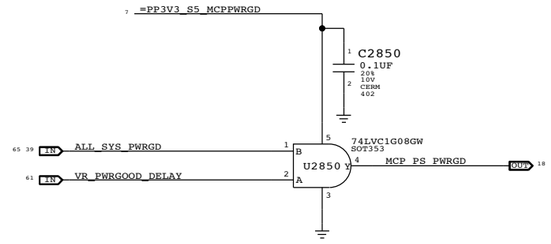
Caesar II (ENET) 25MHz Crystal



Ethernet WAKE# Isolation

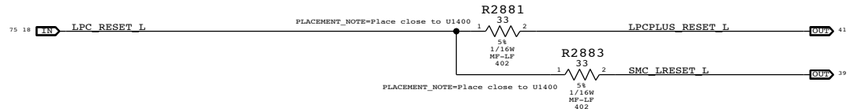


MCP S0 PWRGD & CPU_VLD

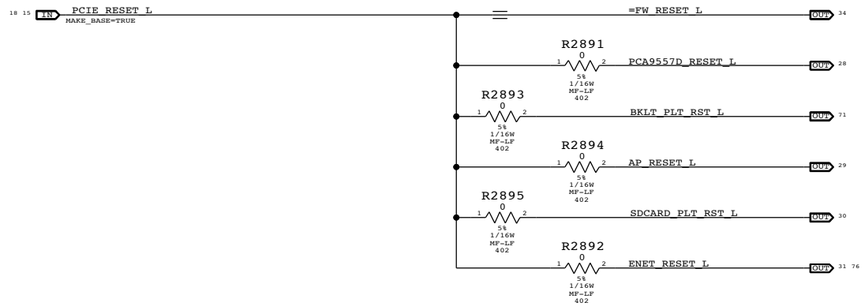


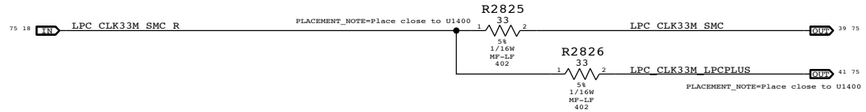
Platform Reset Connections

LPC Reset (Unbuffered)

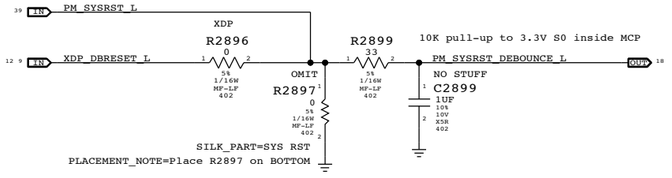


PCIE Reset (Unbuffered)





System Reset Circuit



SYNC MASTER=T27 MLB
SYNC DATE=07/28/2009

PAGE TITLE

SB Misc

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPLVDDR_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 Plane Stitching Caps (Space evenly across plane split)

=PPLVDDR_S3_MEM_A

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603
C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A

PPVREF_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

PPVREF_S3_MEM_VREFCA_A

C2936 0.1UF 20% 10V CERM 402
C2935 2.2UF 20% 6.3V CERM 402-LF

=PPSPD_S0_MEM_A

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

SPD Addr: 0xA0(Wr)/0xA1(Rd)

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

KEY

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD1	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

NCX: 77, 125
NC: 122

MEM_A_CKE<0>	MEM_A_CKE<1>	
MEM_A_BA<2>	MEM_A_A<15>	
MEM_A_A<12>	MEM_A_A<14>	
MEM_A_A<9>	MEM_A_A<11>	
MEM_A_A<8>	MEM_A_A<7>	
MEM_A_A<5>	MEM_A_A<6>	
MEM_A_A<3>	MEM_A_A<4>	
MEM_A_A<1>	MEM_A_A<2>	
MEM_A_CLK_P<0>	MEM_A_A<0>	
MEM_A_CLK_N<0>	MEM_A_CLK_P<1>	
MEM_A_A<10>	MEM_A_CLK_N<1>	
MEM_A_BA<0>	MEM_A_BA<1>	
MEM_A_WE_L	MEM_A_RAS_L	
MEM_A_CAS_L	MEM_A_CS_L<0>	
MEM_A_A<13>	MEM_A_ODT<0>	
MEM_A_CS_L<1>	MEM_A_ODT<1>	
MEM_A_SA<0>	MEM_EVENT_L	MDP
MEM_A_SA<1>	=I2C_SODIMMA_SDA	B1
	=I2C_SODIMMA_SCL	IN

=MEM_A_DQ<32>	=MEM_A_DQ<36>	
=MEM_A_DQ<33>	=MEM_A_DQ<37>	
=MEM_A_DQS_N<4>	=MEM_A_DM<4>	IN
=MEM_A_DQS_P<4>	=MEM_A_DQ<38>	
=MEM_A_DQ<34>	=MEM_A_DQ<39>	
=MEM_A_DQ<35>	=MEM_A_DQ<44>	
=MEM_A_DQ<40>	=MEM_A_DQ<45>	
=MEM_A_DQ<41>	=MEM_A_DQS_N<5>	
=MEM_A_DM<5>	=MEM_A_DQS_P<5>	
=MEM_A_DQ<42>	=MEM_A_DQ<46>	
=MEM_A_DQ<43>	=MEM_A_DQ<47>	
=MEM_A_DQ<48>	=MEM_A_DQ<52>	
=MEM_A_DQ<49>	=MEM_A_DQ<53>	
=MEM_A_DQS_N<6>	=MEM_A_DM<6>	IN
=MEM_A_DQS_P<6>	=MEM_A_DQ<54>	
=MEM_A_DQ<50>	=MEM_A_DQ<55>	
=MEM_A_DQ<51>	=MEM_A_DQ<60>	
=MEM_A_DQ<56>	=MEM_A_DQ<61>	
=MEM_A_DQ<57>	=MEM_A_DQS_N<7>	
=MEM_A_DM<7>	=MEM_A_DQS_P<7>	
=MEM_A_DQ<58>	=MEM_A_DQ<62>	
=MEM_A_DQ<59>	=MEM_A_DQ<63>	

516-0201

"Factory" (top) slot

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)

KEY

	VREFDQ	VSS	
	VSS	DQ4	=MEM_A_DQ<4>
=MEM_A_DQ<0>	DQ0	DQ5	=MEM_A_DQ<5>
=MEM_A_DQ<1>	DQ1	VSS	
	VSS	DQS0*	=MEM_A_DQS_N<0>
=MEM_A_DM<0>	DM0	DQS0	=MEM_A_DQS_P<0>
	VSS	VSS	
=MEM_A_DQ<2>	DQ2	DQ6	=MEM_A_DQ<6>
=MEM_A_DQ<3>	DQ3	DQ7	=MEM_A_DQ<7>
	VSS	VSS	
=MEM_A_DQ<8>	DQ8	DQ12	=MEM_A_DQ<12>
=MEM_A_DQ<9>	DQ9	DQ13	=MEM_A_DQ<13>
	VSS	VSS	
=MEM_A_DQS_N<1>	DQS1*	DM1	=MEM_A_DM<1>
=MEM_A_DQS_P<1>	DQS1	RESET*	MEM_RESET_L
	VSS	VSS	
=MEM_A_DQ<10>	DQ10	DQ14	=MEM_A_DQ<14>
=MEM_A_DQ<11>	DQ11	DQ15	=MEM_A_DQ<15>
	VSS	VSS	
=MEM_A_DQ<16>	DQ16	DQ20	=MEM_A_DQ<20>
=MEM_A_DQ<17>	DQ17	DQ21	=MEM_A_DQ<21>
	VSS	VSS	
=MEM_A_DQS_N<2>	DQS2*	DM2	=MEM_A_DM<2>
=MEM_A_DQS_P<2>	DQS2	VSS	
	VSS	DQ22	=MEM_A_DQ<22>
=MEM_A_DQ<18>	DQ18	DQ23	=MEM_A_DQ<23>
=MEM_A_DQ<19>	DQ19	VSS	
	VSS	DQ28	=MEM_A_DQ<28>
=MEM_A_DQ<24>	DQ24	DQ29	=MEM_A_DQ<29>
=MEM_A_DQ<25>	DQ25	VSS	
	VSS	DQS3*	=MEM_A_DQS_N<3>
=MEM_A_DM<3>	DM3	DQS3	=MEM_A_DQS_P<3>
	VSS	VSS	
=MEM_A_DQ<26>	DQ26	DQ30	=MEM_A_DQ<30>
=MEM_A_DQ<27>	DQ27	DQ31	=MEM_A_DQ<31>
	VSS	VSS	

516-0201

SYNC MASTER=T27 MLB	SYNC DATE=07/28/2009
PAGE TITLE: DDR3 SO-DIMM Connector A	
Apple Inc.	DRAWING NUMBER 051-8563 SIZE D
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	BRANCH
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Page Notes

Power aliases required by this page:
- =PPLVDDR_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 Plane Stitching Caps (Space evenly across plane split)

=PPLVDDR_S3_MEM_B

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_B

PPVREF_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

PPVREF_S3_MEM_VREFCA_B

C3136 0.1UF 20% 10V CERM 402
C3135 2.2UF 20% 6.3V CERM 402-LF

"Expansion" (bottom) slot

DDR3-SODIMM (2 OF 2)

MEM_B_CKE<0>	CKE0	CKE1	MEM_B_CKE<1>
NCX	NC	VDD	
MEM_B_BA<2>	BA2	A15	MEM_B_A<15>
	VDD	A14	MEM_B_A<14>
MEM_B_A<12>	A12/BC*	VDD	
MEM_B_A<9>	A9	A11	MEM_B_A<11>
	VDD	A7	MEM_B_A<7>
MEM_B_A<8>	A8	VDD	
MEM_B_A<5>	A5	A6	MEM_B_A<6>
	VDD	A4	MEM_B_A<4>
MEM_B_A<3>	A3	VDD	
MEM_B_A<1>	A1	A2	MEM_B_A<2>
	VDD	A0	MEM_B_A<0>
MEM_B_CLK_P<0>	CK0	VDD	
MEM_B_CLK_N<0>	CK0*	CK1	MEM_B_CLK_P<1>
	VDD	CK1*	MEM_B_CLK_N<1>
MEM_B_A<10>	A10/AP	VDD	
MEM_B_BA<0>	BA0	BA1	MEM_B_BA<1>
	VDD	RAS*	MEM_B_RAS_L
MEM_B_WE_L	WE*	VDD	
MEM_B_CAS_L	CAS*	S0*	MEM_B_CS_L<0>
	VDD	ODT0	MEM_B_ODT<0>
MEM_B_A<13>	A13	VDD	
MEM_B_CS_L<1>	S1*	ODT1	MEM_B_ODT<1>
	VDD	NC	NC
NCX	TEST	VDD	
	VSS	VREFCA	PPVREF_S3_MEM_VREFCA_B
MEM_B_DQ<32>	DQ32	VSS	
MEM_B_DQ<33>	DQ33	DQ36	MEM_B_DQ<36>
	VSS	DQ37	MEM_B_DQ<37>
MEM_B_DQS_N<4>	DQS4*	VSS	
MEM_B_DQS_P<4>	DQS4	DM4	MEM_B_DM<4>
	VSS	VSS	
MEM_B_DQ<34>	DQ34	DQ38	MEM_B_DQ<38>
MEM_B_DQ<35>	DQ35	DQ39	MEM_B_DQ<39>
	VSS	VSS	
MEM_B_DQ<40>	DQ40	DQ44	MEM_B_DQ<44>
MEM_B_DQ<41>	DQ41	DQ45	MEM_B_DQ<45>
	VSS	VSS	
MEM_B_DM<5>	DM5	DQS5*	MEM_B_DQS_N<5>
	VSS	DQS5	MEM_B_DQS_P<5>
MEM_B_DQ<42>	DQ42	VSS	
MEM_B_DQ<43>	DQ43	DQ46	MEM_B_DQ<46>
	VSS	DQ47	MEM_B_DQ<47>
MEM_B_DQ<48>	DQ48	VSS	
MEM_B_DQ<49>	DQ49	DQ52	MEM_B_DQ<52>
	VSS	DQ53	MEM_B_DQ<53>
MEM_B_DQS_N<6>	DQS6*	VSS	
MEM_B_DQS_P<6>	DQS6	DM6	MEM_B_DM<6>
	VSS	VSS	
MEM_B_DQ<50>	DQ50	DQ54	MEM_B_DQ<54>
MEM_B_DQ<51>	DQ51	DQ55	MEM_B_DQ<55>
	VSS	VSS	
MEM_B_DQ<56>	DQ56	DQ60	MEM_B_DQ<60>
MEM_B_DQ<57>	DQ57	DQ61	MEM_B_DQ<61>
	VSS	VSS	
MEM_B_DM<7>	DM7	DQS7*	MEM_B_DQS_N<7>
	VSS	DQS7	MEM_B_DQS_P<7>
MEM_B_DQ<58>	DQ58	VSS	
MEM_B_DQ<59>	DQ59	DQ62	MEM_B_DQ<62>
	VSS	DQ63	MEM_B_DQ<63>
MEM_B_SA<0>	SA0	VSS	
	VDDSPD	EVENT*	MEM_EVENT_L
MEM_B_SA<1>	SA1	SDA	=I2C_SODIMMB_SDA
	VTT	SCL	=I2C_SODIMMB_SCL
		VTT	
	MTG PIN	MTG PIN	
	MTG PIN	MTG PIN	
	MTG PIN	MTG PIN	
	MTG PIN	MTG PIN	

516s0706

=PPSPD_S0_MEM_B

R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402
C3140 2.2UF 20% 6.3V CERM 402-LF

SPD Addr: 0xA2(Wr)/0xA3(Rd)

DDR3-SODIMM (1 OF 2)

	VREFDQ	VSS	
MEM_B_DQ<0>	DQ0	DQ4	MEM_B_DQ<4>
MEM_B_DQ<1>	DQ1	DQ5	MEM_B_DQ<5>
	VSS	VSS	
MEM_B_DM<0>	DM0	DQS0*	MEM_B_DQS_N<0>
	VSS	DQS0	MEM_B_DQS_P<0>
MEM_B_DQ<2>	DQ2	VSS	
MEM_B_DQ<3>	DQ3	DQ6	MEM_B_DQ<6>
	VSS	DQ7	MEM_B_DQ<7>
MEM_B_DQ<8>	DQ8	VSS	
MEM_B_DQ<9>	DQ9	DQ12	MEM_B_DQ<12>
	VSS	DQ13	MEM_B_DQ<13>
MEM_B_DQS_N<1>	DQS1*	VSS	
MEM_B_DQS_P<1>	DQS1	DM1	MEM_B_DM<1>
	VSS	RESET*	MEM_RESET_L
MEM_B_DQ<10>	DQ10	VSS	
MEM_B_DQ<11>	DQ11	DQ14	MEM_B_DQ<14>
	VSS	DQ15	MEM_B_DQ<15>
MEM_B_DQ<16>	DQ16	VSS	
MEM_B_DQ<17>	DQ17	DQ20	MEM_B_DQ<20>
	VSS	DQ21	MEM_B_DQ<21>
MEM_B_DQS_N<2>	DQS2*	VSS	
MEM_B_DQS_P<2>	DQS2	DM2	MEM_B_DM<2>
	VSS	VSS	
MEM_B_DQ<18>	DQ18	DQ22	MEM_B_DQ<22>
MEM_B_DQ<19>	DQ19	DQ23	MEM_B_DQ<23>
	VSS	VSS	
MEM_B_DQ<24>	DQ24	DQ28	MEM_B_DQ<28>
MEM_B_DQ<25>	DQ25	DQ29	MEM_B_DQ<29>
	VSS	VSS	
MEM_B_DM<3>	DM3	DQS3*	MEM_B_DQS_N<3>
	VSS	DQS3	MEM_B_DQS_P<3>
MEM_B_DQ<26>	DQ26	VSS	
MEM_B_DQ<27>	DQ27	DQ30	MEM_B_DQ<30>
	VSS	DQ31	MEM_B_DQ<31>
		VSS	

516s0706

SYNC MASTER=T27 MLB	SYNC DATE=07/28/2009
PAGE TITLE	DDR3 SO-DIMM Connector B
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MCP CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQ<0>	MAKE_BASE=TRUE	=	=MEM_A_DQ<7>
MEM_A_DQ<1>	MAKE_BASE=TRUE	=	=MEM_A_DQ<2>
MEM_A_DQ<2>	MAKE_BASE=TRUE	=	=MEM_A_DQ<3>
MEM_A_DQ<3>	MAKE_BASE=TRUE	=	=MEM_A_DQ<5>
MEM_A_DQ<4>	MAKE_BASE=TRUE	=	=MEM_A_DQ<1>
MEM_A_DQ<5>	MAKE_BASE=TRUE	=	=MEM_A_DQ<0>
MEM_A_DQ<6>	MAKE_BASE=TRUE	=	=MEM_A_DQ<6>
MEM_A_DQ<7>	MAKE_BASE=TRUE	=	=MEM_A_DQ<4>
MEM_A_DM<0>	MAKE_BASE=TRUE	=	=MEM_A_DM<0>
MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<0>

MCP CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQ<8>	MAKE_BASE=TRUE	=	=MEM_A_DQ<8>
MEM_A_DQ<9>	MAKE_BASE=TRUE	=	=MEM_A_DQ<9>
MEM_A_DQ<10>	MAKE_BASE=TRUE	=	=MEM_A_DQ<14>
MEM_A_DQ<11>	MAKE_BASE=TRUE	=	=MEM_A_DQ<10>
MEM_A_DQ<12>	MAKE_BASE=TRUE	=	=MEM_A_DQ<13>
MEM_A_DQ<13>	MAKE_BASE=TRUE	=	=MEM_A_DQ<12>
MEM_A_DQ<14>	MAKE_BASE=TRUE	=	=MEM_A_DQ<15>
MEM_A_DQ<15>	MAKE_BASE=TRUE	=	=MEM_A_DQ<11>
MEM_A_DM<1>	MAKE_BASE=TRUE	=	=MEM_A_DM<1>
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<1>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<1>

MCP CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQ<16>	MAKE_BASE=TRUE	=	=MEM_A_DQ<17>
MEM_A_DQ<17>	MAKE_BASE=TRUE	=	=MEM_A_DQ<20>
MEM_A_DQ<18>	MAKE_BASE=TRUE	=	=MEM_A_DQ<18>
MEM_A_DQ<19>	MAKE_BASE=TRUE	=	=MEM_A_DQ<19>
MEM_A_DQ<20>	MAKE_BASE=TRUE	=	=MEM_A_DQ<21>
MEM_A_DQ<21>	MAKE_BASE=TRUE	=	=MEM_A_DQ<16>
MEM_A_DQ<22>	MAKE_BASE=TRUE	=	=MEM_A_DQ<23>
MEM_A_DQ<23>	MAKE_BASE=TRUE	=	=MEM_A_DQ<22>
MEM_A_DM<2>	MAKE_BASE=TRUE	=	=MEM_A_DM<2>
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<2>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<2>

MCP CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQ<24>	MAKE_BASE=TRUE	=	=MEM_A_DQ<29>
MEM_A_DQ<25>	MAKE_BASE=TRUE	=	=MEM_A_DQ<26>
MEM_A_DQ<26>	MAKE_BASE=TRUE	=	=MEM_A_DQ<31>
MEM_A_DQ<27>	MAKE_BASE=TRUE	=	=MEM_A_DQ<27>
MEM_A_DQ<28>	MAKE_BASE=TRUE	=	=MEM_A_DQ<28>
MEM_A_DQ<29>	MAKE_BASE=TRUE	=	=MEM_A_DQ<25>
MEM_A_DQ<30>	MAKE_BASE=TRUE	=	=MEM_A_DQ<24>
MEM_A_DQ<31>	MAKE_BASE=TRUE	=	=MEM_A_DQ<30>
MEM_A_DM<3>	MAKE_BASE=TRUE	=	=MEM_A_DM<3>
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<3>

MCP CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQ<32>	MAKE_BASE=TRUE	=	=MEM_A_DQ<38>
MEM_A_DQ<33>	MAKE_BASE=TRUE	=	=MEM_A_DQ<39>
MEM_A_DQ<34>	MAKE_BASE=TRUE	=	=MEM_A_DQ<35>
MEM_A_DQ<35>	MAKE_BASE=TRUE	=	=MEM_A_DQ<32>
MEM_A_DQ<36>	MAKE_BASE=TRUE	=	=MEM_A_DQ<36>
MEM_A_DQ<37>	MAKE_BASE=TRUE	=	=MEM_A_DQ<34>
MEM_A_DQ<38>	MAKE_BASE=TRUE	=	=MEM_A_DQ<33>
MEM_A_DQ<39>	MAKE_BASE=TRUE	=	=MEM_A_DQ<37>
MEM_A_DM<4>	MAKE_BASE=TRUE	=	=MEM_A_DM<4>
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<4>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<4>

MCP CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQ<40>	MAKE_BASE=TRUE	=	=MEM_A_DQ<44>
MEM_A_DQ<41>	MAKE_BASE=TRUE	=	=MEM_A_DQ<45>
MEM_A_DQ<42>	MAKE_BASE=TRUE	=	=MEM_A_DQ<47>
MEM_A_DQ<43>	MAKE_BASE=TRUE	=	=MEM_A_DQ<43>
MEM_A_DQ<44>	MAKE_BASE=TRUE	=	=MEM_A_DQ<42>
MEM_A_DQ<45>	MAKE_BASE=TRUE	=	=MEM_A_DQ<40>
MEM_A_DQ<46>	MAKE_BASE=TRUE	=	=MEM_A_DQ<41>
MEM_A_DQ<47>	MAKE_BASE=TRUE	=	=MEM_A_DQ<46>
MEM_A_DM<5>	MAKE_BASE=TRUE	=	=MEM_A_DM<5>
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<5>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<5>

MCP CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQ<48>	MAKE_BASE=TRUE	=	=MEM_A_DQ<51>
MEM_A_DQ<49>	MAKE_BASE=TRUE	=	=MEM_A_DQ<53>
MEM_A_DQ<50>	MAKE_BASE=TRUE	=	=MEM_A_DQ<50>
MEM_A_DQ<51>	MAKE_BASE=TRUE	=	=MEM_A_DQ<54>
MEM_A_DQ<52>	MAKE_BASE=TRUE	=	=MEM_A_DQ<48>
MEM_A_DQ<53>	MAKE_BASE=TRUE	=	=MEM_A_DQ<49>
MEM_A_DQ<54>	MAKE_BASE=TRUE	=	=MEM_A_DQ<55>
MEM_A_DQ<55>	MAKE_BASE=TRUE	=	=MEM_A_DQ<52>
MEM_A_DM<6>	MAKE_BASE=TRUE	=	=MEM_A_DM<6>
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<6>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<6>

MCP CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQ<56>	MAKE_BASE=TRUE	=	=MEM_A_DQ<56>
MEM_A_DQ<57>	MAKE_BASE=TRUE	=	=MEM_A_DQ<61>
MEM_A_DQ<58>	MAKE_BASE=TRUE	=	=MEM_A_DQ<62>
MEM_A_DQ<59>	MAKE_BASE=TRUE	=	=MEM_A_DQ<59>
MEM_A_DQ<60>	MAKE_BASE=TRUE	=	=MEM_A_DQ<57>
MEM_A_DQ<61>	MAKE_BASE=TRUE	=	=MEM_A_DQ<60>
MEM_A_DQ<62>	MAKE_BASE=TRUE	=	=MEM_A_DQ<63>
MEM_A_DQ<63>	MAKE_BASE=TRUE	=	=MEM_A_DQ<58>
MEM_A_DM<7>	MAKE_BASE=TRUE	=	=MEM_A_DM<7>
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<7>

MCP CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQ<0>	MAKE_BASE=TRUE	=	=MEM_B_DQ<5>
MEM_B_DQ<1>	MAKE_BASE=TRUE	=	=MEM_B_DQ<4>
MEM_B_DQ<2>	MAKE_BASE=TRUE	=	=MEM_B_DQ<3>
MEM_B_DQ<3>	MAKE_BASE=TRUE	=	=MEM_B_DQ<7>
MEM_B_DQ<4>	MAKE_BASE=TRUE	=	=MEM_B_DQ<1>
MEM_B_DQ<5>	MAKE_BASE=TRUE	=	=MEM_B_DQ<0>
MEM_B_DQ<6>	MAKE_BASE=TRUE	=	=MEM_B_DQ<6>
MEM_B_DQ<7>	MAKE_BASE=TRUE	=	=MEM_B_DQ<2>
MEM_B_DM<0>	MAKE_BASE=TRUE	=	=MEM_B_DM<0>
MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<0>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<0>

MCP CHANNEL B DQS 1 -> DIMM B DQS 2

MEM_B_DQ<8>	MAKE_BASE=TRUE	=	=MEM_B_DQ<21>
MEM_B_DQ<9>	MAKE_BASE=TRUE	=	=MEM_B_DQ<20>
MEM_B_DQ<10>	MAKE_BASE=TRUE	=	=MEM_B_DQ<18>
MEM_B_DQ<11>	MAKE_BASE=TRUE	=	=MEM_B_DQ<19>
MEM_B_DQ<12>	MAKE_BASE=TRUE	=	=MEM_B_DQ<16>
MEM_B_DQ<13>	MAKE_BASE=TRUE	=	=MEM_B_DQ<17>
MEM_B_DQ<14>	MAKE_BASE=TRUE	=	=MEM_B_DQ<22>
MEM_B_DQ<15>	MAKE_BASE=TRUE	=	=MEM_B_DQ<23>
MEM_B_DM<1>	MAKE_BASE=TRUE	=	=MEM_B_DM<2>
MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<2>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<2>

MCP CHANNEL B DQS 2 -> DIMM B DQS 1

MEM_B_DQ<16>	MAKE_BASE=TRUE	=	=MEM_B_DQ<14>
MEM_B_DQ<17>	MAKE_BASE=TRUE	=	=MEM_B_DQ<11>
MEM_B_DQ<18>	MAKE_BASE=TRUE	=	=MEM_B_DQ<12>
MEM_B_DQ<19>	MAKE_BASE=TRUE	=	=MEM_B_DQ<8>
MEM_B_DQ<20>	MAKE_BASE=TRUE	=	=MEM_B_DQ<10>
MEM_B_DQ<21>	MAKE_BASE=TRUE	=	=MEM_B_DQ<15>
MEM_B_DQ<22>	MAKE_BASE=TRUE	=	=MEM_B_DQ<13>
MEM_B_DQ<23>	MAKE_BASE=TRUE	=	=MEM_B_DQ<9>
MEM_B_DM<2>	MAKE_BASE=TRUE	=	=MEM_B_DM<1>
MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<1>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<1>

MCP CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQ<24>	MAKE_BASE=TRUE	=	=MEM_B_DQ<28>
MEM_B_DQ<25>	MAKE_BASE=TRUE	=	=MEM_B_DQ<24>
MEM_B_DQ<26>	MAKE_BASE=TRUE	=	=MEM_B_DQ<26>
MEM_B_DQ<27>	MAKE_BASE=TRUE	=	=MEM_B_DQ<30>
MEM_B_DQ<28>	MAKE_BASE=TRUE	=	=MEM_B_DQ<25>
MEM_B_DQ<29>	MAKE_BASE=TRUE	=	=MEM_B_DQ<29>
MEM_B_DQ<30>	MAKE_BASE=TRUE	=	=MEM_B_DQ<31>
MEM_B_DQ<31>	MAKE_BASE=TRUE	=	=MEM_B_DQ<27>
MEM_B_DM<3>	MAKE_BASE=TRUE	=	=MEM_B_DM<3>
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<3>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<3>

MCP CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQ<32>	MAKE_BASE=TRUE	=	=MEM_B_DQ<32>
MEM_B_DQ<33>	MAKE_BASE=TRUE	=	=MEM_B_DQ<37>
MEM_B_DQ<34>	MAKE_BASE=TRUE	=	=MEM_B_DQ<34>
MEM_B_DQ<35>	MAKE_BASE=TRUE	=	=MEM_B_DQ<35>
MEM_B_DQ<36>	MAKE_BASE=TRUE	=	=MEM_B_DQ<36>
MEM_B_DQ<37>	MAKE_BASE=TRUE	=	=MEM_B_DQ<33>
MEM_B_DQ<38>	MAKE_BASE=TRUE	=	=MEM_B_DQ<39>
MEM_B_DQ<39>	MAKE_BASE=TRUE	=	=MEM_B_DQ<38>
MEM_B_DM<4>	MAKE_BASE=TRUE	=	=MEM_B_DM<4>
MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<4>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<4>

MCP CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQ<40>	MAKE_BASE=TRUE	=	=MEM_B_DQ<42>
MEM_B_DQ<41>	MAKE_BASE=TRUE	=	=MEM_B_DQ<44>
MEM_B_DQ<42>	MAKE_BASE=TRUE	=	=MEM_B_DQ<41>
MEM_B_DQ<43>	MAKE_BASE=TRUE	=	=MEM_B_DQ<40>
MEM_B_DQ<44>	MAKE_BASE=TRUE	=	=MEM_B_DQ<47>
MEM_B_DQ<45>	MAKE_BASE=TRUE	=	=MEM_B_DQ<45>
MEM_B_DQ<46>	MAKE_BASE=TRUE	=	=MEM_B_DQ<46>
MEM_B_DQ<47>	MAKE_BASE=TRUE	=	=MEM_B_DQ<43>
MEM_B_DM<5>	MAKE_BASE=TRUE	=	=MEM_B_DM<5>
MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<5>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<5>

MCP CHANNEL B DQS 6 -> DIMM B DQS 6

MEM_B_DQ<48>	MAKE_BASE=TRUE	=	=MEM_B_DQ<49>
MEM_B_DQ<49>	MAKE_BASE=TRUE	=	=MEM_B_DQ<53>
MEM_B_DQ<50>	MAKE_BASE=TRUE	=	=MEM_B_DQ<50>
MEM_B_DQ<51>	MAKE_BASE=TRUE	=	=MEM_B_DQ<51>
MEM_B_DQ<52>	MAKE_BASE=TRUE	=	=MEM_B_DQ<52>
MEM_B_DQ<53>	MAKE_BASE=TRUE	=	=MEM_B_DQ<48>
MEM_B_DQ<54>	MAKE_BASE=TRUE	=	=MEM_B_DQ<55>
MEM_B_DQ<55>	MAKE_BASE=TRUE	=	=MEM_B_DQ<54>
MEM_B_DM<6>	MAKE_BASE=TRUE	=	=MEM_B_DM<6>
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<6>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<6>

MCP CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQ<56>	MAKE_BASE=TRUE	=	=MEM_B_DQ<62>
MEM_B_DQ<57>	MAKE_BASE=TRUE	=	=MEM_B_DQ<63>
MEM_B_DQ<58>	MAKE_BASE=TRUE	=	=MEM_B_DQ<56>
MEM_B_DQ<59>	MAKE_BASE=TRUE	=	=MEM_B_DQ<60>
MEM_B_DQ<60>	MAKE_BASE=TRUE	=	=MEM_B_DQ<59>
MEM_B_DQ<61>	MAKE_BASE=TRUE	=	=MEM_B_DQ<58>
MEM_B_DQ<62>	MAKE_BASE=TRUE	=	=MEM_B_DQ<57>
MEM_B_DQ<63>	MAKE_BASE=TRUE	=	=MEM_B_DQ<61>
MEM_B_DM<7>	MAKE_BASE=TRUE	=	=MEM_B_DM<7>
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<7>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<7>

SYNC MASTER=K18 MLB SYNC DATE=06/19/2009

PAGE TITLE

DDR3 BYTE/BIT SWAPS-K6

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

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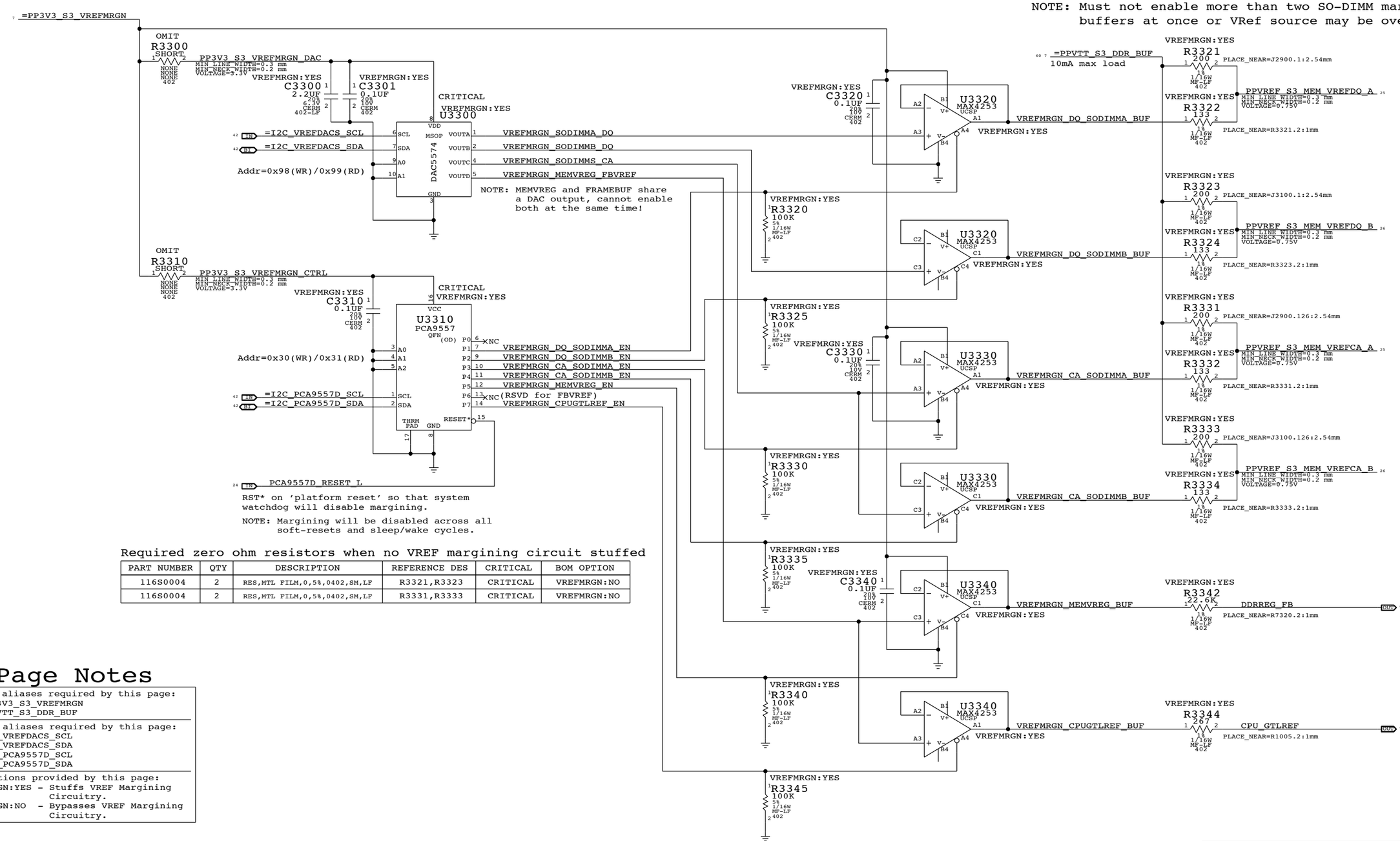

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3321,R3323	CRITICAL	VREFMRGN:NO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3331,R3333	CRITICAL	VREFMRGN:NO

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	7
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	9.24mV / step @ output

SYNC_MASTER=T27_MLB SYNC_DATE=09/29/2009

PAGE TITLE: FSB/DDR3 Vref Margining

Apple Inc.

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5V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

PCIE_AP_D2R_P
PCIE_AP_D2R_N
74 6 PCIE_AP_R2D_P
74 6 PCIE_AP_R2D_N
79 6 PCIE_CLK100M_AP_CONN_P
79 6 PCIE_CLK100M_AP_CONN_N
(AP_CLKREQ_Q_L)
PCIE_WAKE_L
(AP_RESET_CONN_L)
NC
NC

PLACEMENT_NOTE=Place close to J3401.

C3431 0.1uF 10% 16V X5R 402
C3430 0.1uF 10% 16V X5R 402

PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N

CRITICAL
L3401
90-OHM-100MA
DLP11S

PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N

AIRPORT

1000 mA peak
750 mA nominal max
6 PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

L3404
FERR-120-OHM-1.5A
0402-LF

C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 20% 10V CERM 402
C3420 10UF 20% 10V X5R 805

29 PP5V_WLAN_F
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

PLACEMENT_NOTE=Place close to J3401.
PLACEMENT_NOTE=Place close to Q3450.
PLACEMENT_NOTE=Place close to Q3450.

CRITICAL
Q3450
TPCP8102
23V1K-SM

C3450 0.1UF 10% 16V X5R 402
P5VWLAN_SS
C3451 0.033UF 10% 16V X5R 402
R3450 33K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402

=PP5V_S3_WLAN 7
PM_WLAN_EN_L IN 65

6 PP5V_S3_BTCAMERA_F
I2C_ALS_SDA BI 42
I2C_ALS_SCL IN 42
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

ALS

275 mA peak
206 mA nominal max

L3405
FERR-120-OHM-1.5A
0402-LF

C3452 0.1uF 20% 10V CERM 402

=PP5V_S3_BTCAMERA 7

CAMERA

79 6 USB_CAMERA_CONN_P
79 6 USB_CAMERA_CONN_N

CRITICAL
L3402
90-OHM
DLP0NS

USB_CAMERA_P OUT 17 75
USB_CAMERA_N OUT 17 75

PLACEMENT_NOTE=Place close to J3401.

BLUETOOTH

79 6 USB_BT_CONN_P
79 6 USB_BT_CONN_N

CRITICAL
L3403
90-OHM
DLP0NS

USB_BT_P BI 17 75
USB_BT_N BI 17 75

PLACEMENT_NOTE=Place close to J3401.

Supervisor & CLKREQ# Isolation

PP5V_WLAN_F 29
=PP3V3_S3_WLAN 7

R3440 100K 5% 1/16W MF-LF 402
R3453 392K 1% 1/16W MF-LF 402
R3454 97.6K 1% 1/16W MF-LF 402

WF: Need pull-up?
P3V3WLAN_VMON

CRITICAL
U3440
SLG4AP016V
TDFN
VDD
SENSE
0.7V
DLY
RESET*
MR*
EN
OUT
(OD)
IN
THRM PAD
GND

C3440 0.1uF 20% 10V CERM 402

DLY = 60 ms +/- 20%

6 AP_RESET_CONN_L
AP_RESET_L IN 24
AP_PWR_EN IN 18 65
6 AP_CLKREQ_Q_L
AP_CLKREQ_L OUT 15

SYNC MASTER=T27 MLB
SYNC DATE=07/28/2009
PAGE TITLE
RIGHT CLUTCH CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8563
SIZE D
REVISION A.13.0
BRANCH
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SHEET 29 OF 80

Caesar IV Support

=PP3V3_S3_CARDREADER
GL137 R3511 0 5% 1/16W MF-LF 402

PP3V3_S3_CARDREADER_DVDD
MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V
BYPASS=U3500.15:16:5 mm BYPASS=U3500.26:27:5 mm BYPASS=U3500.35:34:5 mm
GL137 L3500 0.22UH 0805-1
GL137 C3500 10UF 20% 6.3V X5R 603
GL137 C3501 0.1UF 20% 10V CERM 402
GL137 C3502 0.1UF 20% 10V CERM 402
GL137 C3503 0.1UF 20% 10V CERM 402

PP3V3_S3_CARDREADER_AVDD
MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V
BYPASS=U3500.6:5:5 mm BYPASS=U3500.11:12:5 mm
GL137 C3514 10UF 20% 6.3V X5R 603
GL137 C3504 0.1UF 20% 10V CERM 402
GL137 C3508 0.1UF 20% 10V CERM 402

PP1V8_S3_CARDREADER
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM VOLTAGE=1.8V
BYPASS=U3500.4:5:5 mm
GL137 C3506 0.1UF 20% 10V CERM 402

GL137 R3507 10K 5% 1/16W MF-LF 402 — NO STUFF R3508 10K 5% 1/16W MF-LF 402
NO STUFF R3509 10K 5% 1/16W MF-LF 402 — GL137 R3510 10K 5% 1/16W MF-LF 402

NO STUFF R3503 1M 5% 1/16W MF-LF 402
CRITICAL GL137 Y3500 12.000M-100PPM 8X4.5X1.4-SM
GL137 C3511 33PF 5% 50V CERM 402
GL137 C3512 33PF 5% 50V CERM 402

GL137 R3506 715 1% 1/16W MF-LF 402
GL137 R3502 0 5% 1/16W MF-LF 402
NO STUFF C3513 0.1UF 20% 10V CERM 402

GL137 Q3500 SSM6N15FEAPE SOT563
SDCARD_RESET
SDCARD_PLT_RST
GL137 Q3500 SSM6N15FEAPE SOT563
SDCARD_PLT_RST_L

U3500 GL137A LQFP CRITICAL GL137

VDD18	4	
AVDD	6	
DVDD	11	
VDD5V	15	
PMOS	26	
NC	35	
	25	
	36	
USB_SDCARD_N	7	DM
USB_SDCARD_P	8	DP
GL137_GPIO1	48	GPIO1
GL137_GPIO2	47	GPIO2
	46	GPIO3
NC	19	SK
NC	20	CS
NC	21	DO
NC	22	DI (IPD)
GL137_CLK12M_X1	13	X1
GL137_CLK12M_X2	14	X2
GL137_RREF	10	RREF
GL137_TESTMOD	17	TESTMOD (IPD)
GL137_RESET_L	18	EXTRSTZ* (IPU)
GND	5, 9, 12, 16, 27, 34	

D0	40	
D1	43	
D2	37	
D3	29	
D4	28	
D5	30	
D6	32	
D7	38	
CLK	39	SD_CLK_R
(IPD) SD_WP	3	
(IPD) SD_CMD	41	
(IPU) PDMOD	2	GL137_PDMOD
(IPU) SD_CDZ	23	
(IPU) XD_CDZ	1	NC
XD_CE	31	NC
(IPD) XD_WEZ	42	NC
(IPD) XD_RBZ	44	NC
(IPD) XD_WPZ	45	NC
(IPU) MS_INS	24	NC
(IPD) MS_BS	33	NC

PDMOD: POWER DOWN MODES
NC = DISABLE (DEFAULT)
10K LOW = POWER SAVING MODE ENABLE
10K HIGH = REMOTE WAKE UP ENABLE

SDCONN_DATA<0> — BCM57765 R3550 0 5% 1/16W MF-LF 402 — SD_D<0>
SDCONN_DATA<1> — BCM57765 R3551 0 5% 1/16W MF-LF 402 — SD_D<1>
SDCONN_DATA<2> — BCM57765 R3552 0 5% 1/16W MF-LF 402 — SD_D<2>
SDCONN_DATA<3> — BCM57765 R3553 0 5% 1/16W MF-LF 402 — SD_D<3>
SDCONN_DATA<4..7> — SD_D<4..7> MAKE_BASE=TRUE
SDCONN_CLK — BCM57765 R3554 0 5% 1/16W MF-LF 402 — SD_CLK
SDCONN_CMD — BCM57765 R3556 0 5% 1/16W MF-LF 402 — SD_CMD MAKE_BASE=TRUE
SDCONN_WP — SD_WP MAKE_BASE=TRUE
SDCONN_CD — SD_CD_L MAKE_BASE=TRUE

=PP3V3_S0_SDCONN
BCM57765 R3555 0 5% 1/10W MF-LF 603

Keep this net short!
PP3V3_SW_SD_PWR
MIN_LINE_WIDTH=0.50 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V MAKE_BASE=TRUE
MAX CURRENT = 800 MA

GL137 R3512 10K 5% 1/16W MF-LF 402
C3507 2.2UF 20% 6.3V CERM1 603
C3505 0.1UF 20% 10V CERM 402
R3505 39K 5% 1/16W MF-LF 402

NO STUFF R3513 10K 5% 1/16W MF-LF 402
GL137 R3504 0 5% 1/16W MF-LF 402
NO STUFF C3515 10PF 5% 50V CERM 402-1

CRITICAL J3500 SD-CARD-K19-K24 F-RT-TH

3	VSS
6	VSS
5	CLK
2	CMD
7	DAT0
8	DAT1
9	DAT2
1	CD/DAT3
10	DAT4
11	DAT5
12	DAT6
13	DAT7
14	CARD_DETECT_SW
15	CARD_DETECT_GND
16	WRITE_PROTECT_SW
4	VDD
17	SHLD_PIN
18	SHLD_PIN
19	SHLD_PIN
20	SHLD_PIN

SD_CLK
SD_CMD
SD_D<0>
SD_D<1>
SD_D<2>
SD_D<3>
SD_D<4>
SD_D<5>
SD_D<6>
SD_D<7>
SD_WP
SD_CD_L

516-0225

ADDED SERIES RESISTOR TO SD_CMD, MAX CURRENT NUMBER CHANGED TO 800MA

SYNC MASTER=T27 MLB — SYNC DATE=09/30/2009
PAGE TITLE: SecureDigital Card Reader
Apple Inc.
DRAWING NUMBER: 051-8563 — SIZE: D
REVISION: A.13.0
BRANCH:
PAGE: 35 OF 109
SHEET: 30 OF 80

BCM57765 SR pins are internal 1.2V switching regulator.
If unused: Okay to float all 4 pins. (Broadcom not so sure now)
If used: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor, VFB to =PP1V2_ENET_PHY

=PP3V3_ENET_PHY
86mA (1000base-T, Caesar II)

BCM57765 R3915 0 5% 1/16W MF-LF 402

CRITICAL L3900 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

BCM57765 R3900 0 5% 1/16W MF-LF 402
BCM57765_XTALVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

BCM57765 R3940 4.7K 5% 1/16W MF-LF 402
BCM57765 R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

=PP3V3_S0_ENETPHY
BCM57765 R3942 1K 5% 1/16W MF-LF 402

TP_BCM57765_SR_VDDP
BCM57765_SR_VDD
BCM57765_VDDO_PIN20
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

BCM57765_SR_LX
BCM57765_SR_VFB

CRITICAL L3920 FERR-600-OHM-0.5A =PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

AVDDH BIASVDDH VDDC VDDIO XTALVDDH VDDIO VDDC VDDIO REGCTL12 VDDIO WAKE* AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC VDDC

CRITICAL OMIT U3900 BCM5764M QFN-8X8 VERSION 2

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

BCM57765 R3943 0 5% 1/16W MF-LF 402
=ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM5764_SCLK
BCM5764_MISO
BCM5764_MOSI
BCM5764_CS_L
TP_BCM5764_SPD100LED_L
TP_BCM5764_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM5764_RDAC

SMB_DATA (IPD)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
LINKLED* (OD)
LOW_PWR (IPD)
VDDC
UART_MODE (IPD-BCM5764M)
SCLK
SI
SO
CS*
(IPU)
SPD100LED*
TRAFFICLED*
XTALI
XTALO
RDAC

R3965 1.24K 1% 1/16W MF-LF 402

THRM_PAD 69

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
TRD0_P TRD0_N TRD1_P TRD1_N TRD2_P TRD2_N TRD3_P TRD3_N

CR_BUS_PWR is not for SD Card power, just decoupling for BCM57765 CR I/Os.
BCM57765 C3970 4.7UF 10% 6.3V X5R-CERM 603
BCM57765 C3971 0.1UF 10% 16V X7R-CERM 402
BCM57765 C3972 0.1UF 10% 16V X7R-CERM 402

PP3V3R1V8_SW_SD_VIO
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

(IPD) GPIO_0/SERIAL_DO NC
GPIO_1/SERIAL_DI
GPIO_2 BCM57765_MEDIA_SENSE R3972 0 5% 1/16W MF-LF 402 ENET_ENERGY_DET (OUT)
NC BCM57765_SD_DETECT R3973 0 5% 1/16W MF-LF 402 SDCONN_CD (IN)
PCIE_VDDL BCM57765_CR_CMD R3974 0 5% 1/16W MF-LF 402 SDCONN_CMD (IN)
PLACE_NEAR=L3999.1:1 mm
DC0 SDCONN_CLK (OUT)
DC4 SDCONN_DATA<0>
DC3 SDCONN_DATA<1>
DC2 SDCONN_DATA<2>
DC1 SDCONN_DATA<3>
NC BCM57765_CR_DATA<4> R3975 0 5% 1/16W MF-LF 402 SDCONN_DATA<4>
VMAIN_PRSNT BCM57765_CR_DATA<5> R3976 0 5% 1/16W MF-LF 402 SDCONN_DATA<5>
VAUX_PRSNT BCM57765_CR_DATA<6> R3977 0 5% 1/16W MF-LF 402 SDCONN_DATA<6>
VDDC BCM57765_CR_DATA<7> R3978 0 5% 1/16W MF-LF 402 SDCONN_DATA<7>
SMB_CLK BCM57765_CE_L_MS_INS_L
ENERGY_DET BCM57765_CR_LED
DC5 SDCONN_WP (IN)
SPD1000LED* TP_BCM57765_XD_DET

BCM57765: All resistors above BOMOPTIONed BCM57765
BCM57765 supports both active-levels for WP.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

=PP3V3_ENET_PHY
U3990 AT45DB011D SOIC-8S1 OMIT
VCC SCK CS* WP* RESET* SI SO GND
C3990 0.1UF 10% 16V X7R-CERM 402
BCM57765 R3990 4.7K 5% 1/16W MF-LF 402
BCM5764M R3997 4.7K 5% 1/16W MF-LF 402
BCM5764_SCLK BCM5764_CS_L BCM5764_MOSI BCM5764_MISO

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M pin-function

60-ENERGY_DET	BCM57765_CR_LED	R3980	0		ENET_ENERGY_DET
13-WAKE*	BCM57765_SR_VFB	R3981	0		=ENET_WAKE_L (See note)
53-VMAIN_PRSNT	BCM57765_CR_DATA<5>	R3982	1K		=PP3V3_S0_ENETPHY
59-SMB_CLK	BCM57765_CE_L_MS_INS_L	R3983	4.7K		=PP3V3_ENET_PHY
58-SMB_DATA	BCM57765_VMAIN_PRSNT	R3984	4.7K		
54-VAUX_PRSNT	BCM57765_CR_DATA<6>	R3985	1K		
16-VDDIO	BCM57765_SR_LX	R3986	0		
20-XTALVDDH	BCM57765_VDDO_PIN20	R3987	0		PP3V3_ENET_PHY_XTALVDDH
55-VDDC	BCM57765_CR_DATA<7>	R3988	0		=PP1V2_ENET_PHY
17-VDDC	BCM57765_XTALVDDH	R3989	0		
14-VDDC	BCM57765_SR_VDD	R3998	0		
06-VDDC	BCM57765_SMB_CLK	R3999	0		

All resistors 5% 1/16W MF-LF 402

26-PCIE_VDDL BCM57765_CR_CMD PLACE_NEAR=U3900.26:2 mm
L3999 FERR-600-OHM-0.5A SM CRITICAL
Keep net short, with no stubs.
BCM5764M C3999 0.1UF 10% 16V X7R-CERM 402 PLACE_NEAR=U3900.26:1 mm
BCM5764M C3998 4.7UF 10% 6.3V X5R-CERM 603 PLACE_NEAR=L3999.1:1 mm

SYNC_MASTER=T27_MLB SYNC_DATE=08/20/2009
PAGE TITLE: Ethernet PHY (Caesar II/IV)
Apple Inc.
DRAWING NUMBER 051-8563 SIZE D
REVISION A.13.0
BRANCH
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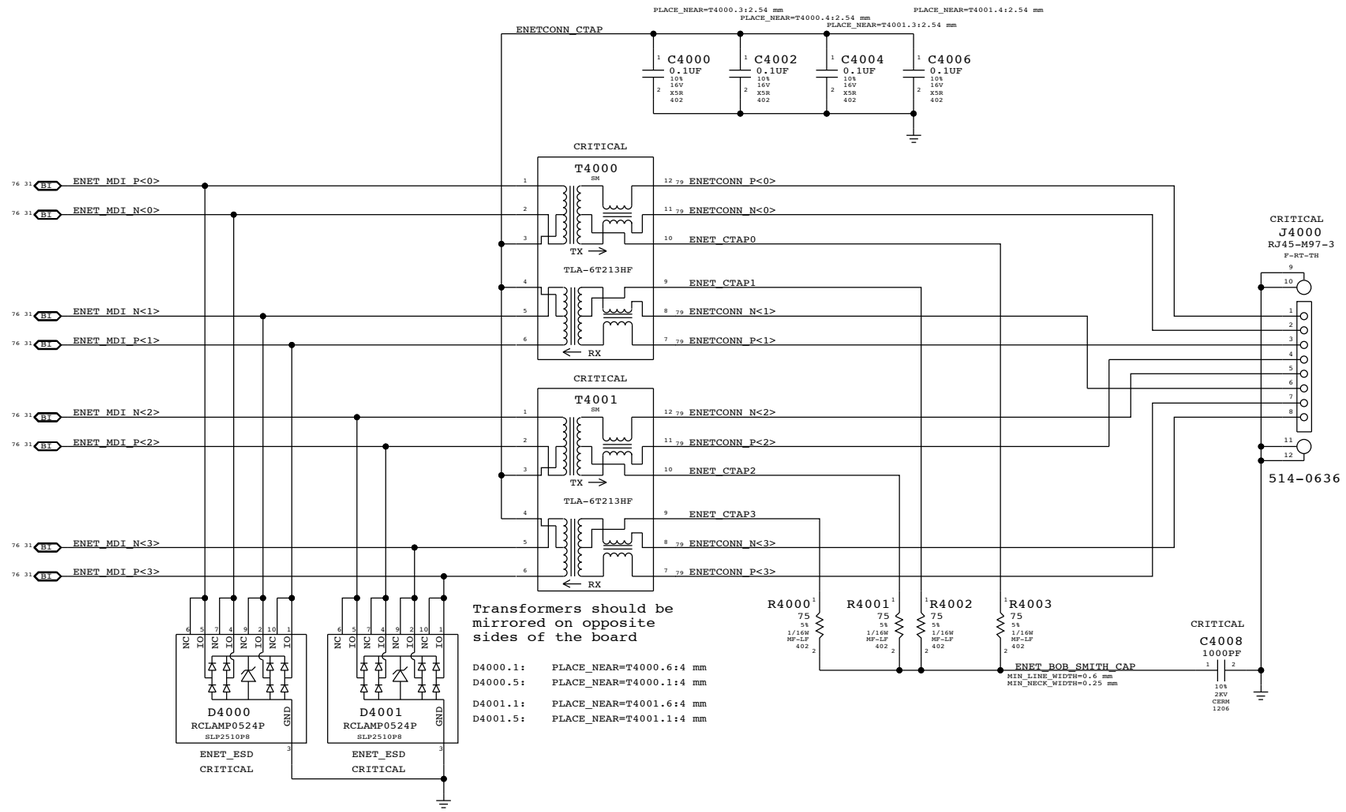
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=T27 MLB — SYNC DATE=07/28/2009

PAGE TITLE

Ethernet Connector

Apple Inc.

DRAWING NUMBER 051-8563 — SIZE D

REVISION A.13.0

BRANCH

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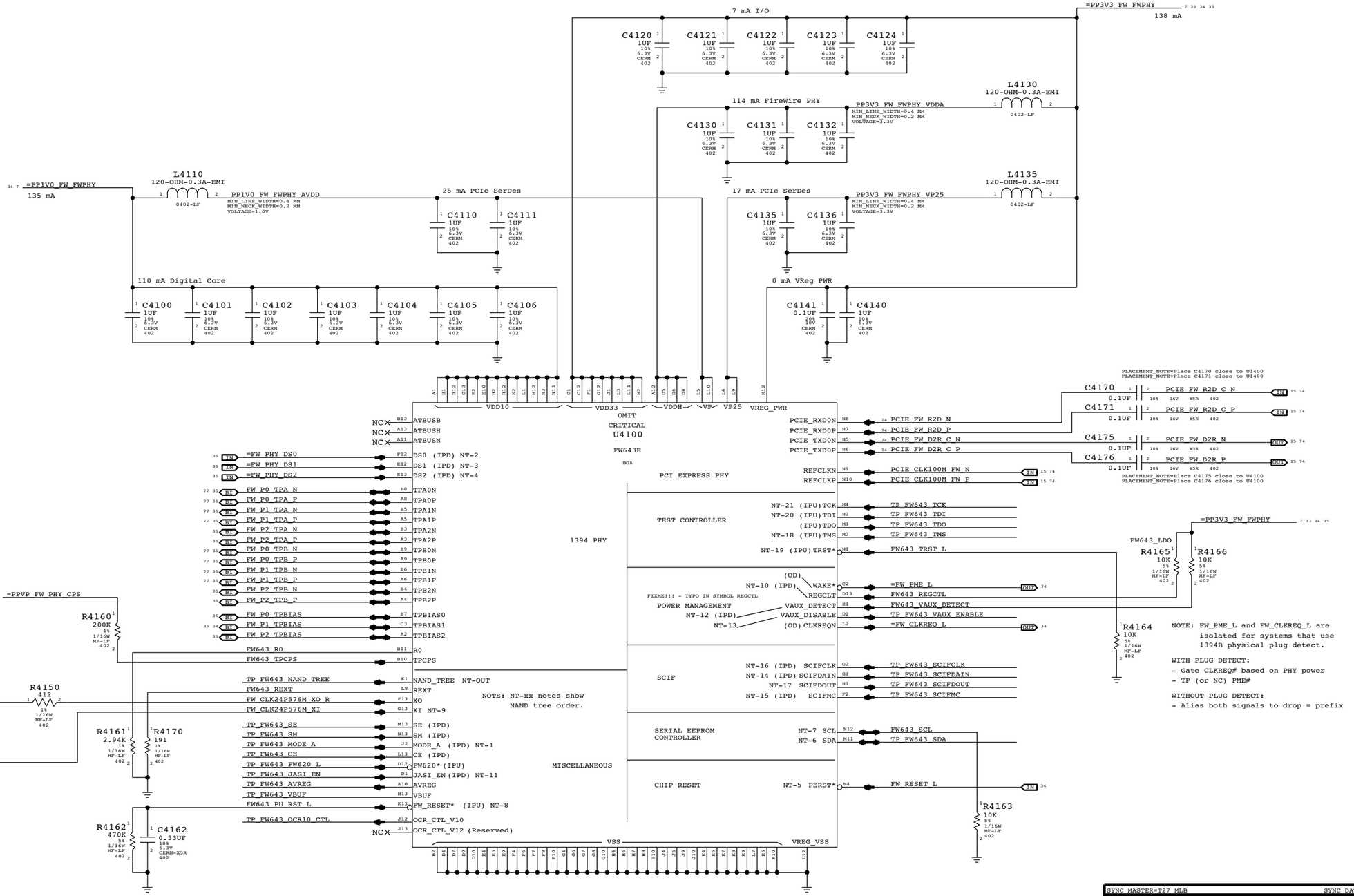

SYNC MASTER=T27 MLB | SYNC DATE=07/20/2005

PAGE TITLE

FireWire LLC/PHY (FW643E)

Apple Inc.

DRAWING NUMBER 051-8563 | SIZE D

REVISION A.13.0

BRANCH

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SHEET 33 OF 80

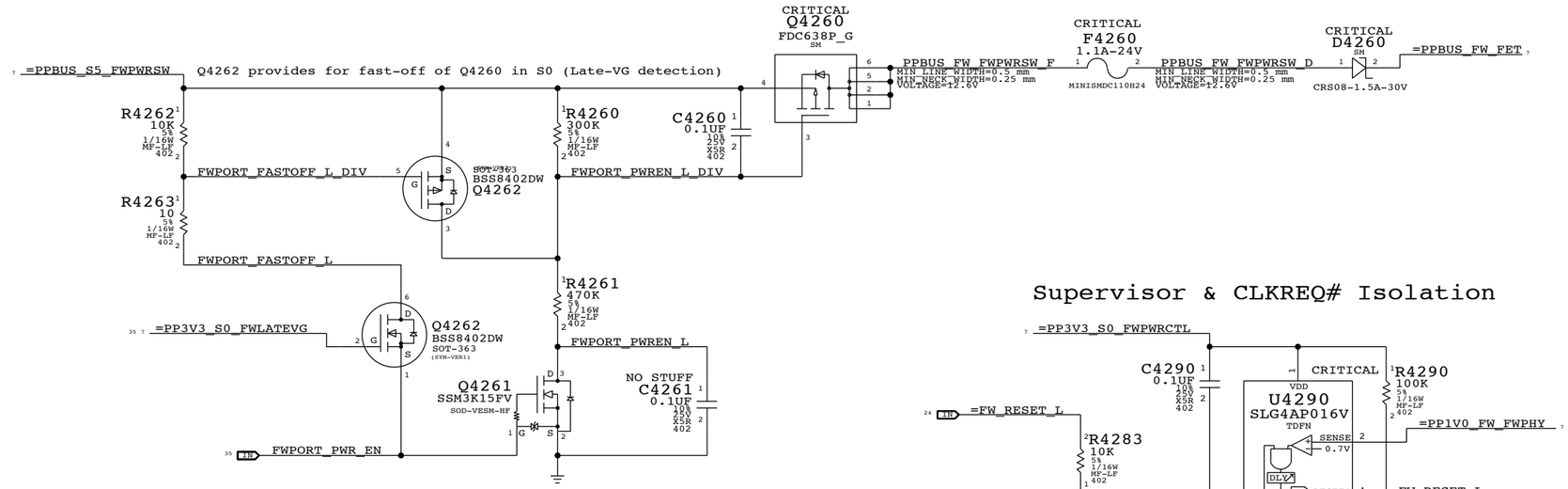
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

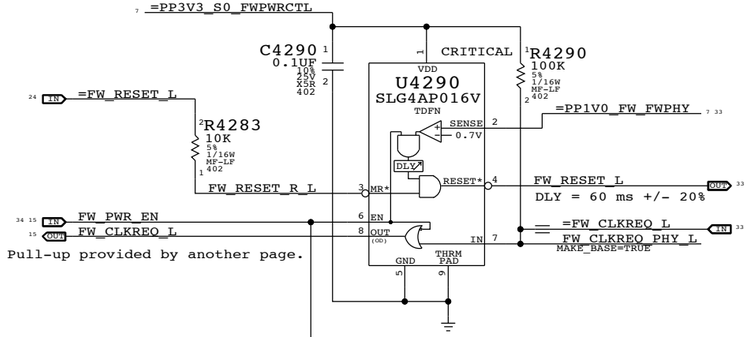
Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

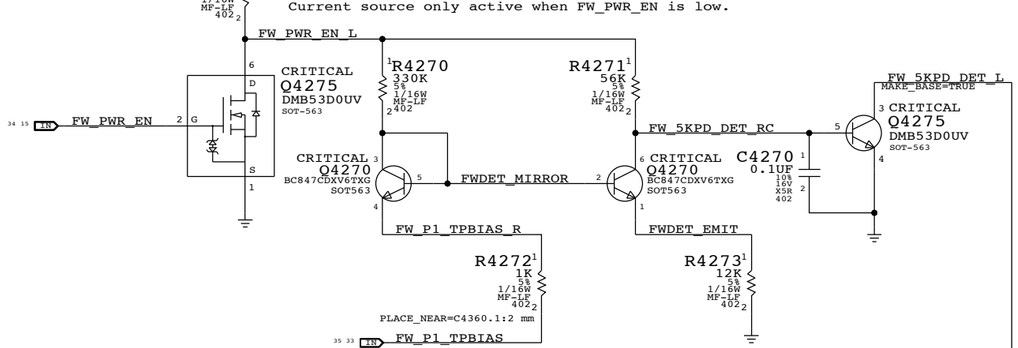


Supervisor & CLKREQ# Isolation



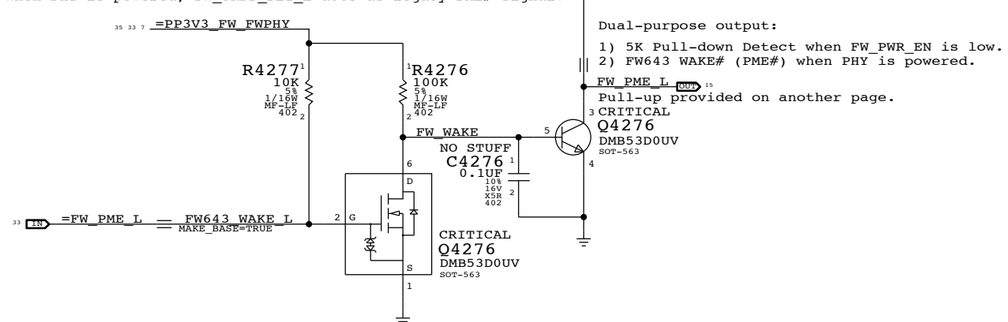
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

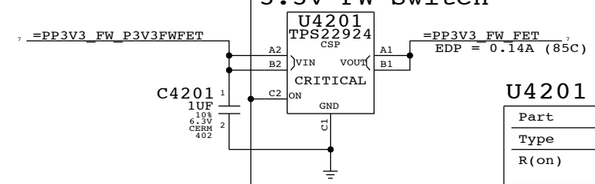


Dual-purpose output:

1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

3.3V FW Switch

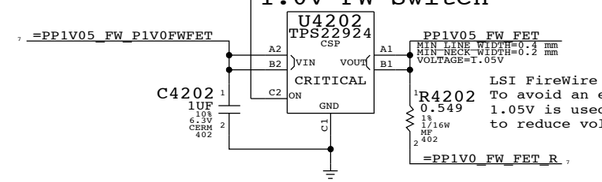


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC_MASTER=T27_MLB SYNC_DATE=12/15/2009

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D
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PAGE 42 OF 109
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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.

=PPVP_FW_PHY_CPS_FET
From Port
R4311 470K 5% 1/16W MF-LF 402
CPS_EN_L_DIV
R4312 330K 5% 1/16W MF-LF 402
CPS_EN_L
=PP3V3_FW_FWPHY
Q4300 BSS8402DW SOT-363 (SYM-VER1)
PPVP_FW_CPS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVP_FW_PHY_CPS
To FW643

Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)

FW_P0_TPBIAS	NC_FW0_TPBIAS	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P0_TPA_P	NC_FW0_TPAP	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P0_TPA_N	NC_FW0_TPAN	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P0_TPB_P	NC_FW0_TPBP	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P0_TPB_N	NC_FW0_TPBN	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P2_TPBIAS	NC_FW2_TPBIAS	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P2_TPA_P	NC_FW2_TPAP	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P2_TPA_N	NC_FW2_TPAN	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P2_TPB_P	NC_FW2_TPBP	MAKE_BASE=TRUE, NO_TEST=TRUE
FW_P2_TPB_N	NC_FW2_TPBN	MAKE_BASE=TRUE, NO_TEST=TRUE

FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

=PP3V3_FW_FWPHY
R4382 10K 1% 1/16W MF-LF 402
R4380 10K 1% 1/16W MF-LF 402
R4381 10K 1% 1/16W MF-LF 402
FWPHY_DS0 = =FW_PHY_DS0 (OUT)
FWPHY_DS1 = =FW_PHY_DS1 (OUT)
FWPHY_DS2 = =FW_PHY_DS2 (OUT)

Termination

Place close to FireWire PHY

FW_P1_TPBIAS
C4360 0.33UF 10% 6.3V CERM-X5R 402
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402
FW_P1_TPA_P
FW_P1_TPA_N
FW_P1_TPB_P
FW_P1_TPB_N
FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402
FW_PORT1_TPB_C
C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

"Snapback" & "Late VG" Protection

=PP3V3_S0_FWLATEVG
PLACE_NEAR=U4350.1:2 mm
C4350 0.1UF 10% 16V X5R 402
U4350 TPD4S1394 LLP
TP_FWLATEVG_VCLMP
FWPORT_PWR_EN
R4350 100K 5% 1/16W MF-LF 402
(PINS 5/6 AND 7/8 ARE SWAPPED FOR BETTER ROUTING)
(FW_PORT1_TPA_P)
(FW_PORT1_TPA_N)
(FW_PORT1_TPB_P)
(FW_PORT1_TPB_N)

Cable Power

=PPVP_FW_PORT1
CRITICAL
L4310 FERR-250-OHM SM
PPVP_FW_PORT1_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V
C4314 0.01UF 10% 50V X7R 402
C4319 0.1uF 10% 50V X7R 603-1
PLACE_NOTE=J4310.5:2 mm
R4319 1M 5% 1/16W MF-LF 402

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PORT 1

BILINGUAL
CRITICAL
J4310 1394B-M97 F-RT-TH

(FW_PORT1_TPB_N)
(FW_PORT1_BREF)
(FW_PORT1_TPB_P)
(GND)
(FW_PORT1_TPA_N)
FW_PORT1_AREF
(FW_PORT1_TPA_P)
TPB- TPB(R) TPB+ VP NC SC/NC TPA- VG TPA+ TPA(R) — OUTPUT
CHASSIS GND
514S0605

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC MASTER=T27 MLB
SYNC DATE=07/28/2009
PAGE TITLE: FireWire Connector
Apple Inc.
DRAWING NUMBER: 051-8563
SIZE: D
REVISION: A.13.0
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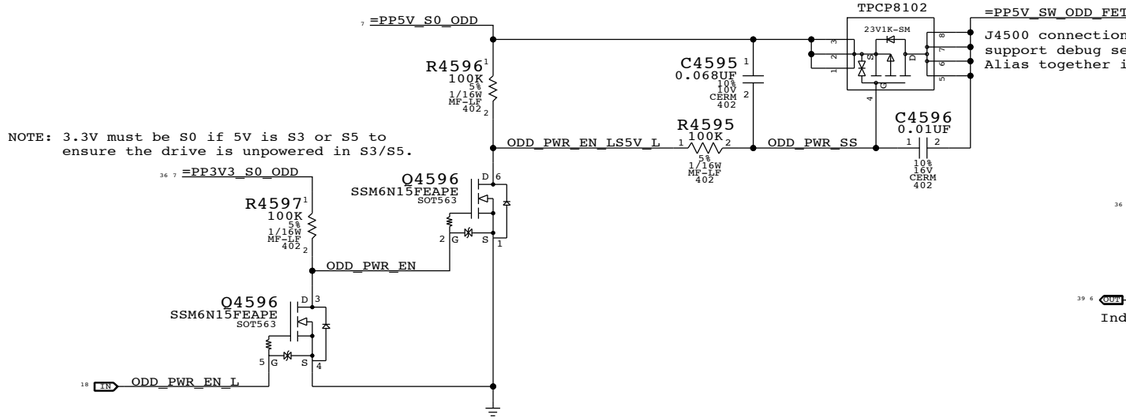
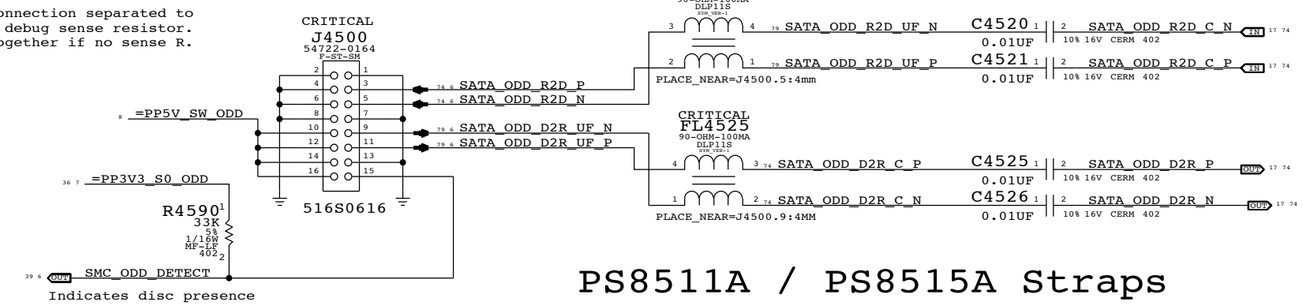
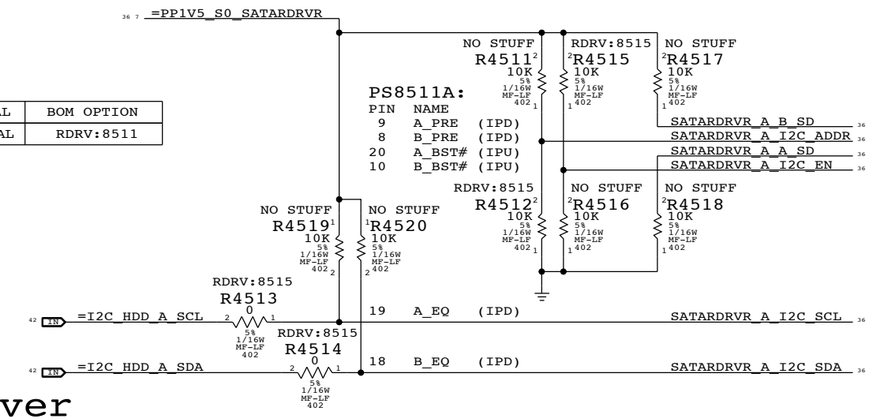
ODD Power Control



SATA ODD Port



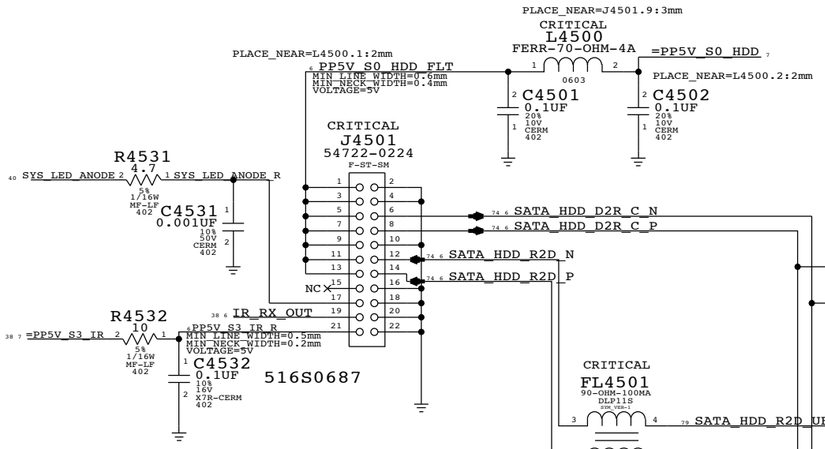
PS8511A / PS8515A Straps



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8511

BOMOPTIONs:
- RDRV:8511 stuffs PS8511A & associated parts (STRAPS TBD!!!)
- RDRV:8515 stuffs PS8515A & associated parts
- RDRV:NO stuffs bypass path (neither IC or associated parts stuffed)

SATA HDD Port



SATA Redriver

U4510 ADD NO STUFF IN PRODUCTION!!!!

J5401 PINOUTS ARE DIFFERENT FOR K6, DO NOT SYNC THIS PAGE FROM T27 DIRECTLY

SYNC MASTER=T27 MLB SYNC DATE=08/06/2009

PAGE TITLE: SATA Connectors

Apple Inc.

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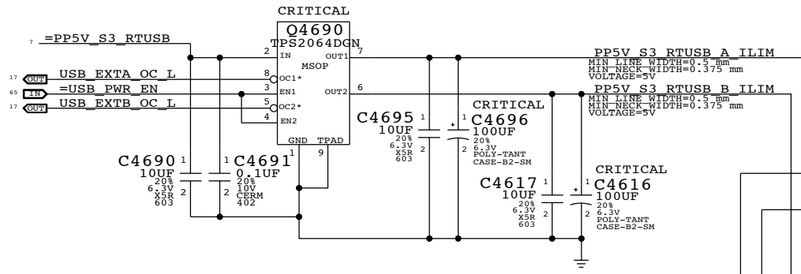
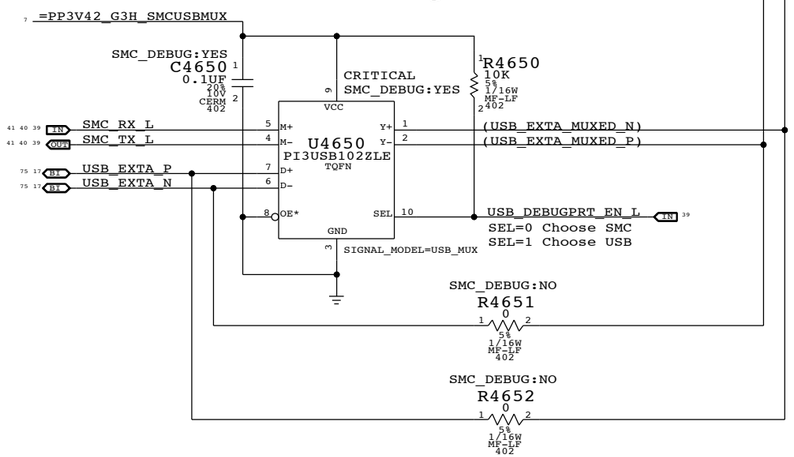
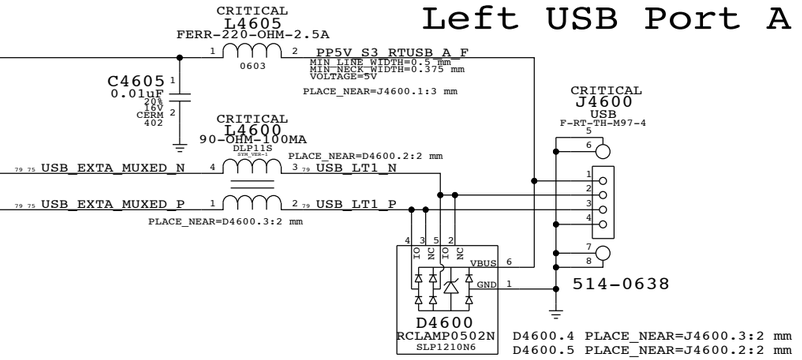
Port Power Switch



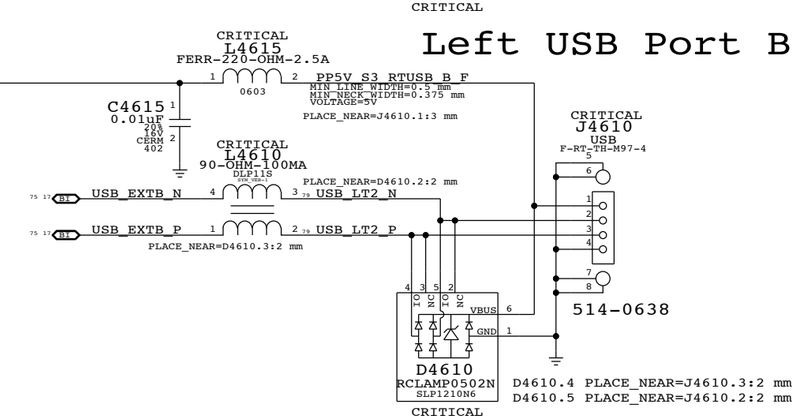
USB/SMC Debug Mux



Left USB Port A



Left USB Port B



SYNC_MASTER=T27_MLB SYNC_DATE=08/27/2009

PAGE TITLE
External USB Connectors

Apple Inc.

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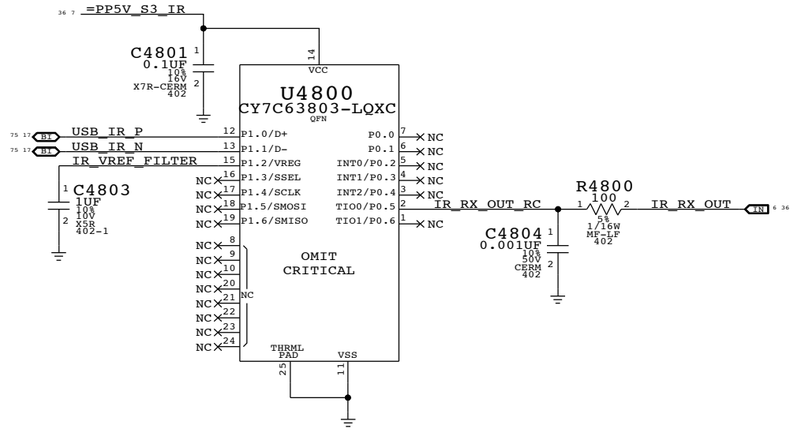
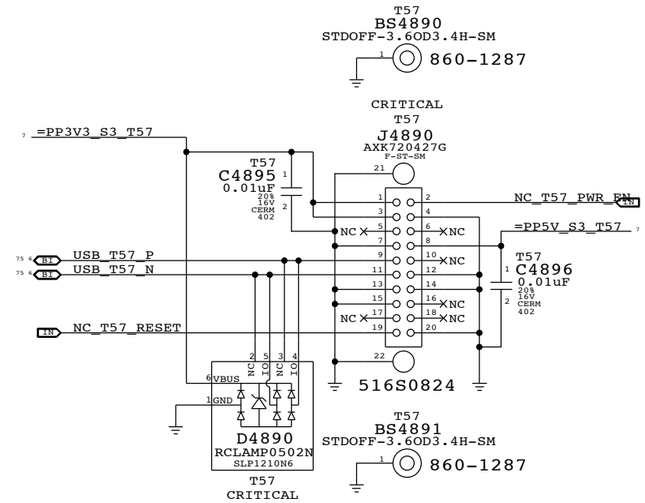
IR Support



T57 Connector



K6 NOTES : D4890 CONNECTION IS DIFFERENT,CANNOT DIRECTLY SYNC FROM T27

SYNC MASTER=T27 MLB | SYNC DATE=08/27/2009

PAGE TITLE: Internal USB Support

Apple Inc.

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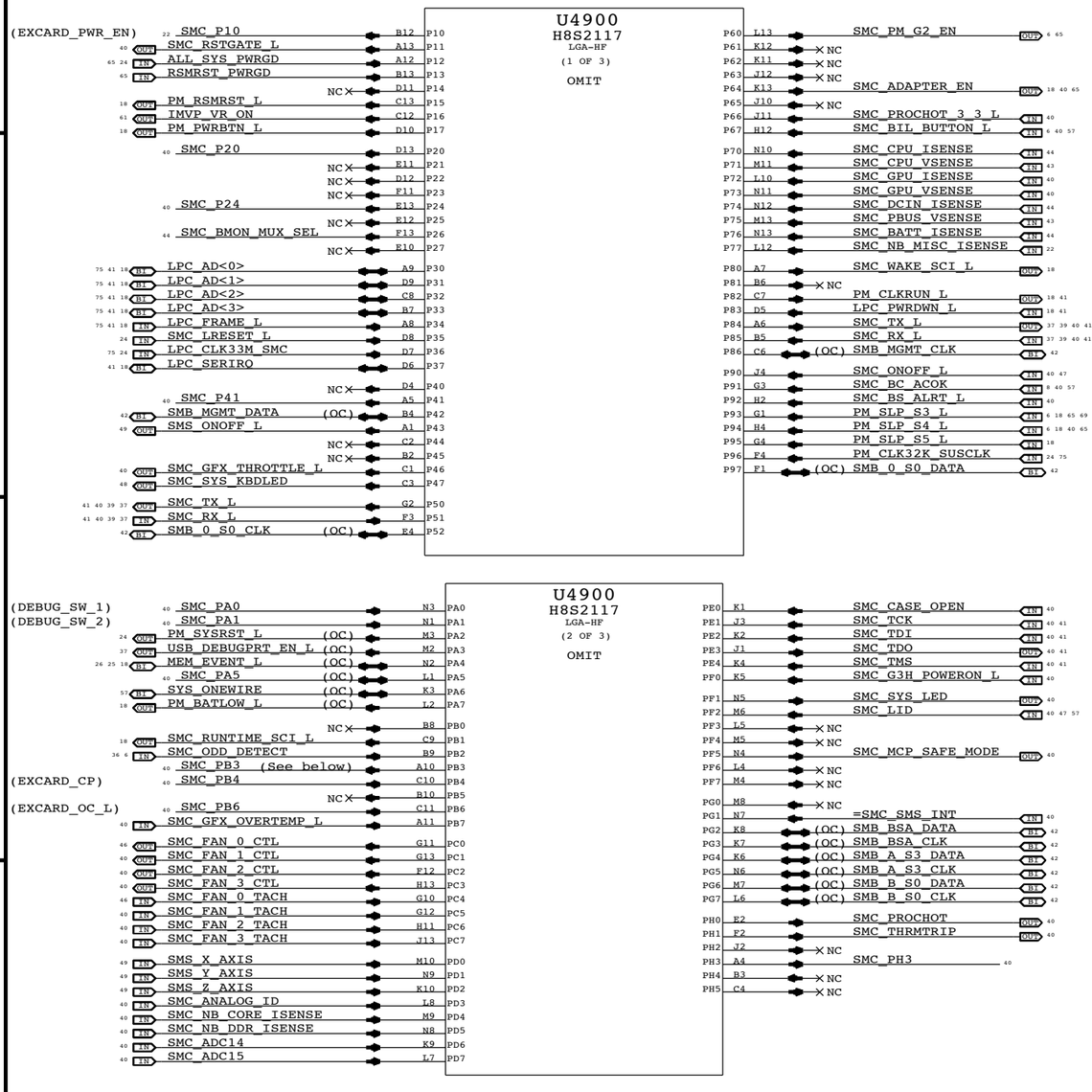
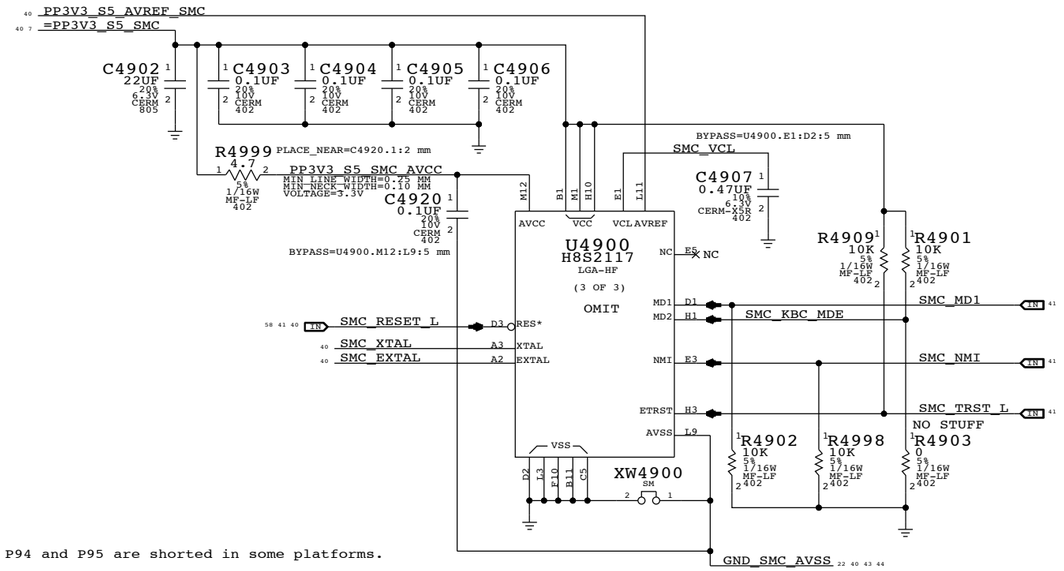
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay.



NOTE: P94 and P95 are shorted in some platforms.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC_MASTER=T27_MLB SYNC_DATE=09/02/2009

PAGE TITLE: SMC

Apple Inc.

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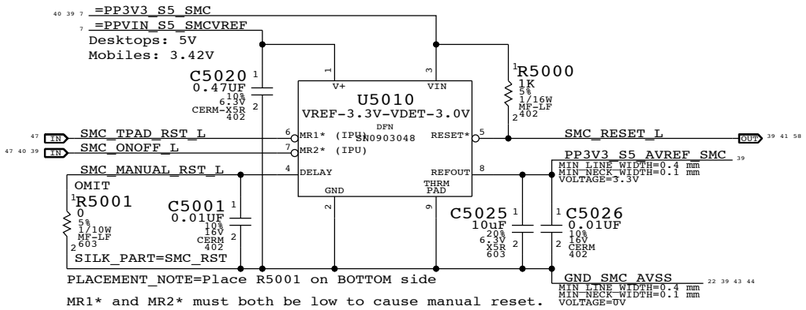
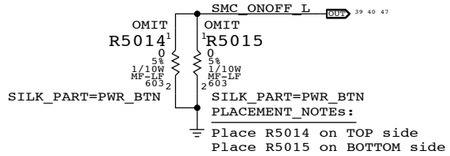
SMC Reset "Button", Supervisor & AVREF Supply



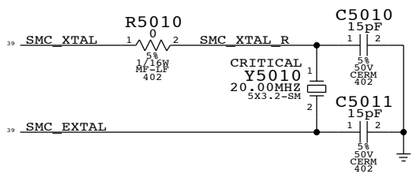
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

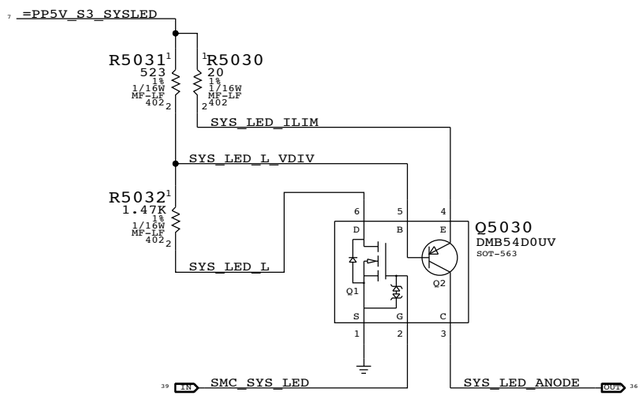
Debug Power "Buttons"



SMC Crystal Circuit



System (Sleep) LED Circuit



SMC Aliases

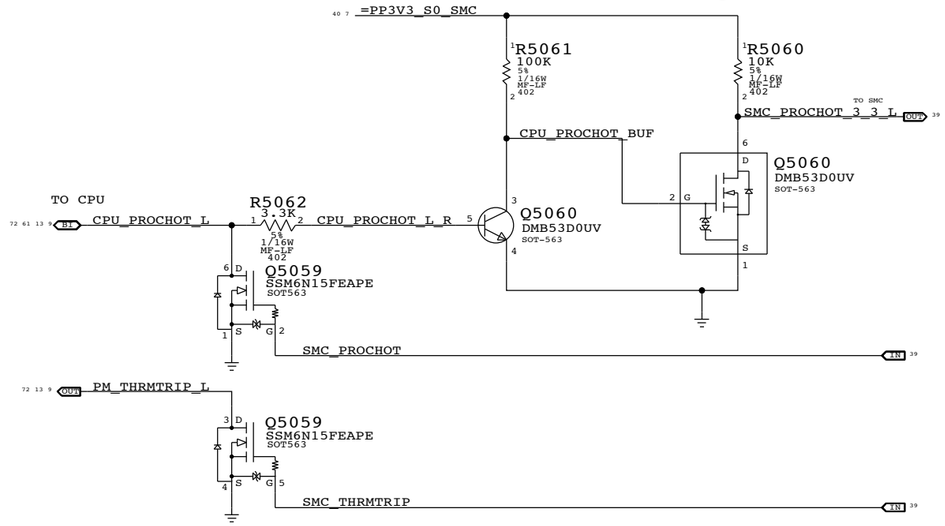
SMC_MCP_VSENSE (MAKE_BASE=TRUE)	=	SMC_ADC14
SMC_CPU_FSB_ISENSE (MAKE_BASE=TRUE)	=	SMC_ADC15
SMC_MCP_CORE_ISENSE (MAKE_BASE=TRUE)	=	SMC_NB_CORE_ISENSE
SMC_MCP_DDR_ISENSE (MAKE_BASE=TRUE)	=	SMC_NB_DDR_ISENSE
TP_SMC_GPU_1V8_ISENSE (MAKE_BASE=TRUE)	=	SMC_ANALOG_ID
TP_SMC_GPU_ISENSE (MAKE_BASE=TRUE)	=	SMC_GPU_ISENSE
TP_SMC_GPU_VSENSE (MAKE_BASE=TRUE)	=	SMC_GPU_VSENSE
SMC_GFX_THROTTLE_L	=	SMC_IG_THROTTLE_L (MAKE_BASE=TRUE)
SMS_INT_L (MAKE_BASE=TRUE)	=	=SMC_SMS_INT
MCP_WAKE_REQ_L	=	SMC_G3H_POWERON_L (MAKE_BASE=TRUE)

R5096 0 5% 1/16W MF-LF 402
SMC_MCP_SAFE_MODE — MCP_SPKR

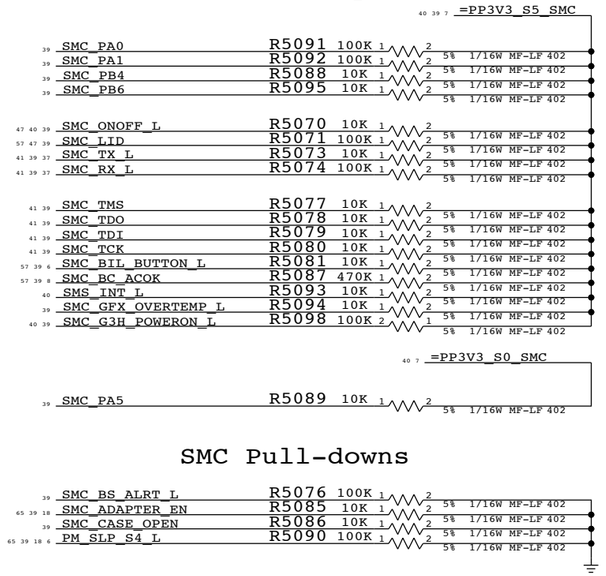
Unused Pins

SMC_FAN_1_CTL	=	TP_SMC_FAN_1_CTL (MAKE_BASE=TRUE)
TP_SMC_FAN_1_TACH (MAKE_BASE=TRUE)	=	SMC_FAN_1_TACH
SMC_FAN_2_CTL	=	NC_SMC_FAN_2_CTL (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_FAN_2_TACH (MAKE_BASE=TRUE, NO_TEST=TRUE)	=	SMC_FAN_2_TACH
SMC_FAN_3_CTL	=	NC_SMC_FAN_3_CTL (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_FAN_3_TACH (MAKE_BASE=TRUE, NO_TEST=TRUE)	=	SMC_FAN_3_TACH
SMC_RSTGATE_L	=	TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)
SMC_P20	=	TP_SMC_P20 (MAKE_BASE=TRUE)
SMC_P24	=	TP_SMC_P24 (MAKE_BASE=TRUE)
SMC_P41	=	TP_SMC_P41 (MAKE_BASE=TRUE)
SMC_PB3	=	TP_SMC_PB3 (MAKE_BASE=TRUE)
SMC_PH3	=	TP_SMC_PH3 (MAKE_BASE=TRUE)

SMC FSB to 3.3V Level Shifting



SMC Pull-ups



SMC Pull-downs

SYNC_MASTER=T27_MLB SYNC_DATE=09/02/2009

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Apple Inc.

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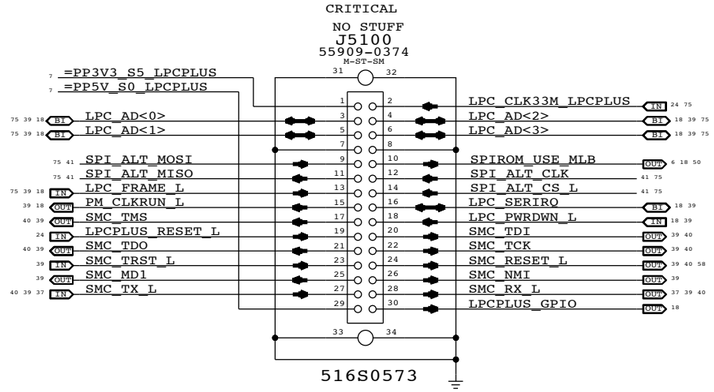
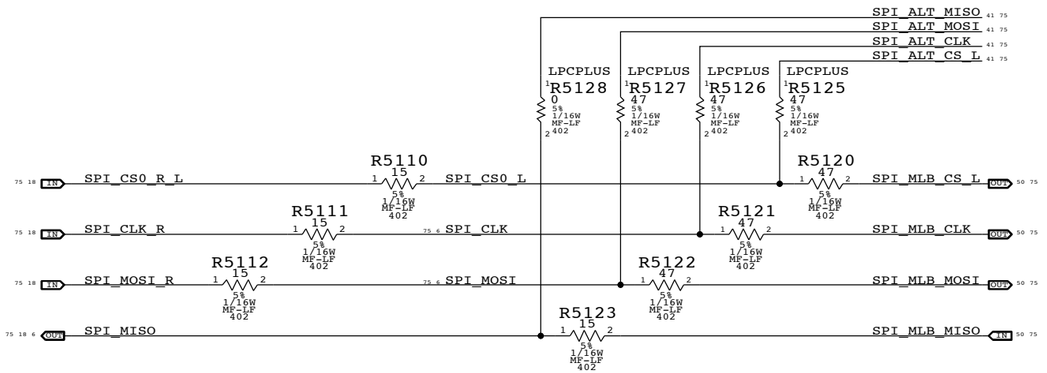
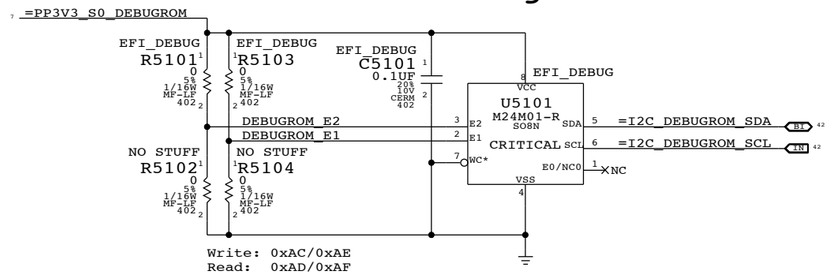
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC MASTER=T27 MLB SYNC DATE=08/27/2009

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

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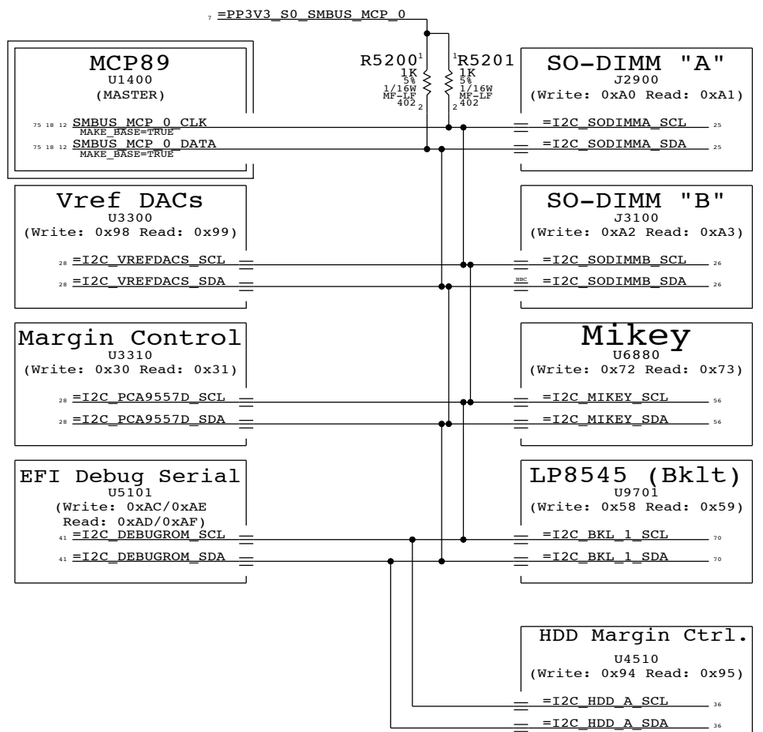
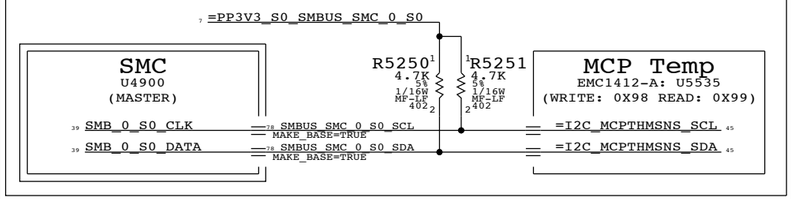
MCP89 SMBus "0" Connections

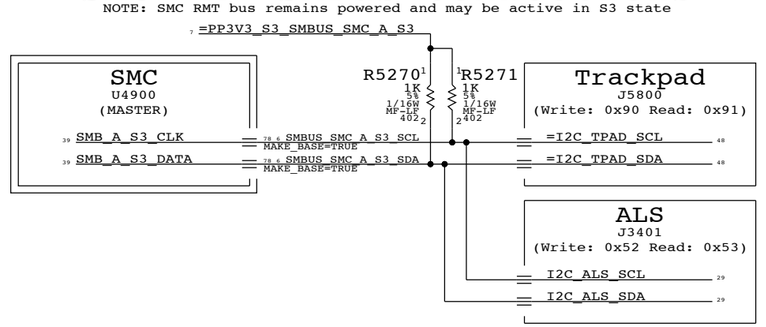


SMC "0" SMBus Connections

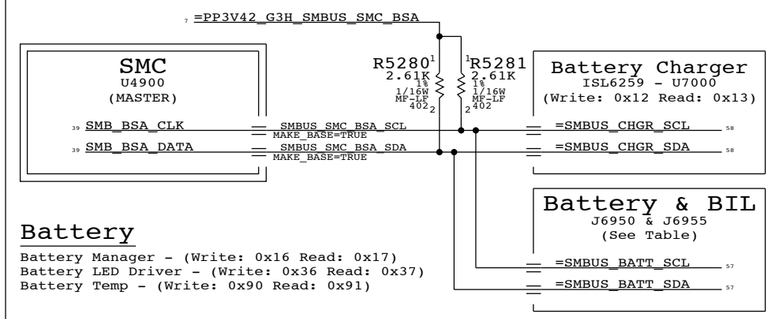


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "Battery A" SMBus Connections

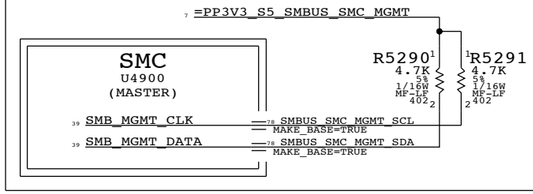


Battery

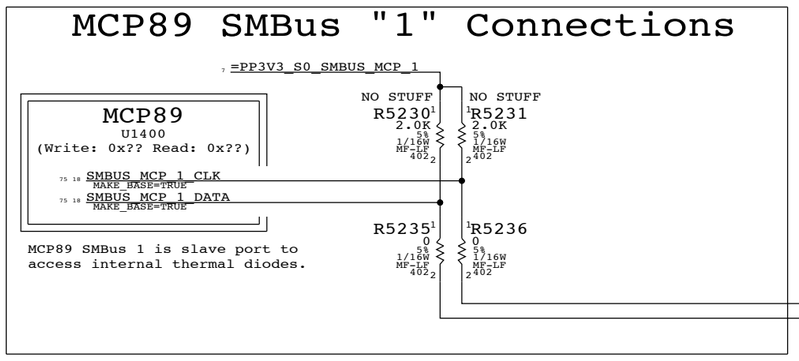
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

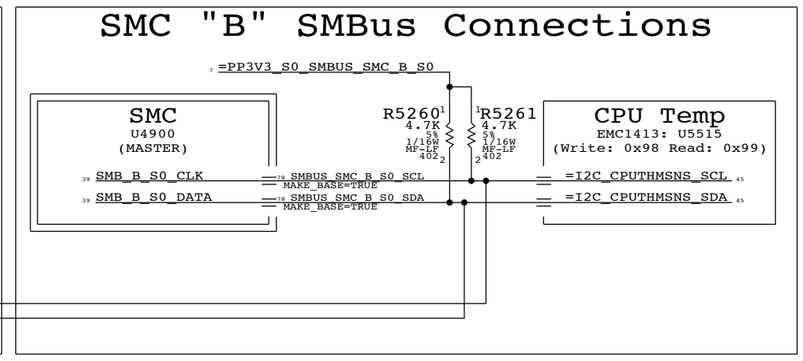


MCP89 SMBus "1" Connections



MCP89 SMBus 1 is slave port to access internal thermal diodes.

SMC "B" SMBus Connections



NOTE:

R5280/81 WAS 2K ON K24, VALUE NEEDS TO BE CHECKED
R5290/91 (VREF DAC, MARGIN CONTROL)WAS 4.7K ON K24, VALUE NEEDS TO BE CHECKED

SYNC MASTER=T27 MLB SYNC DATE=08/21/2009

PAGE TITLE
K6 SMBUS CONNECTIONS

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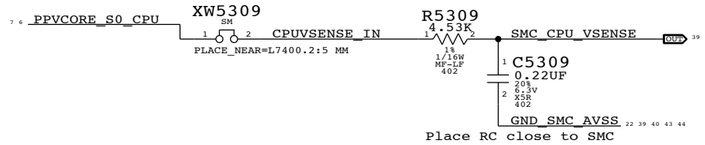
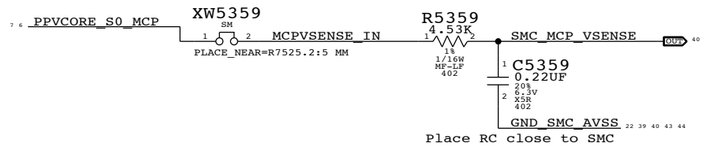
CPU Voltage Sense / Filter



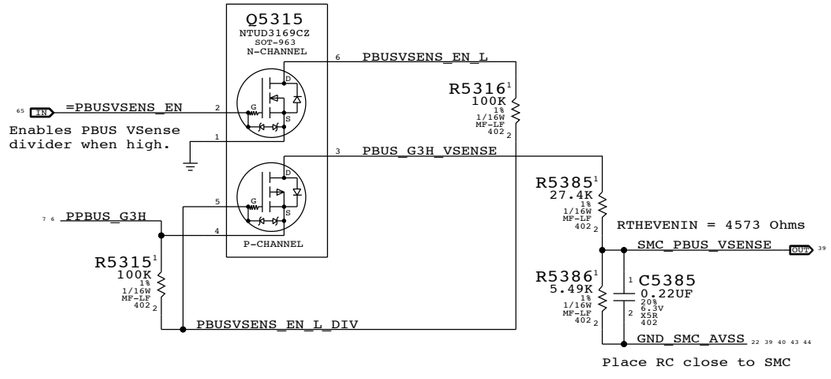
Place RC close to SMC

MCP Voltage Sense / Filter



Place RC close to SMC

PBUS Voltage Sense Enable & Filter



Place RC close to SMC

SYNC MASTER=T27 MLB SYNC DATE=08/27/2009

PAGE TITLE

Voltage Sensing

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

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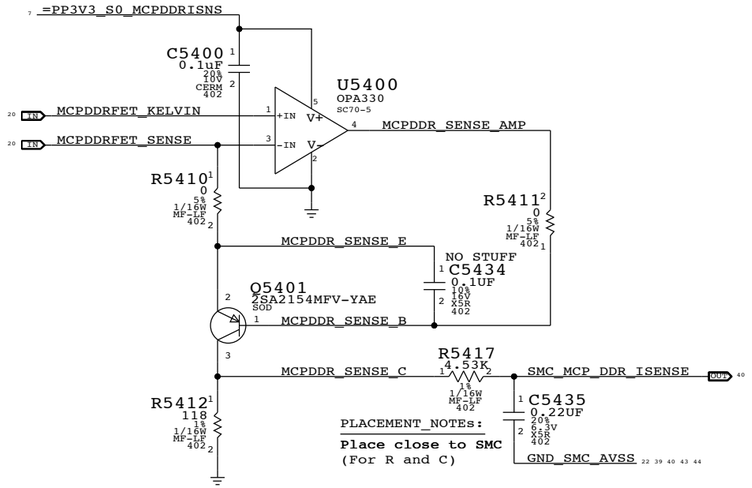
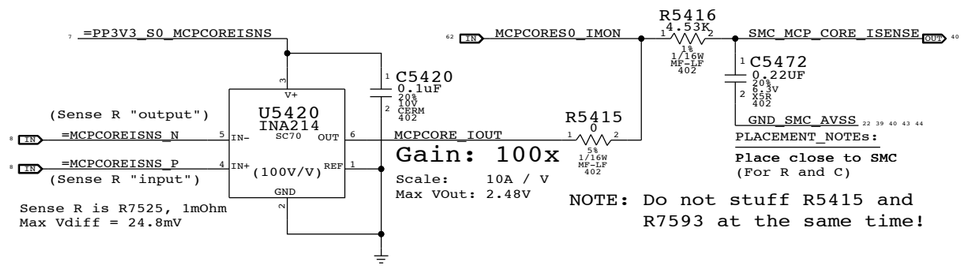
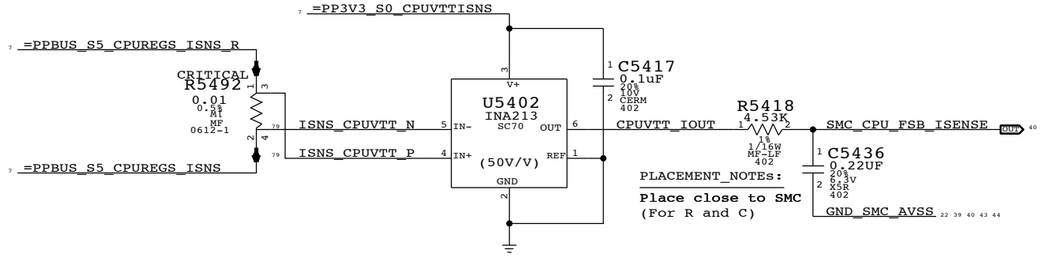
MCP MEM VDD Current Sense / Filter



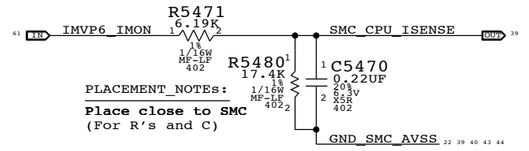
MCP VCore Current Sense Filter



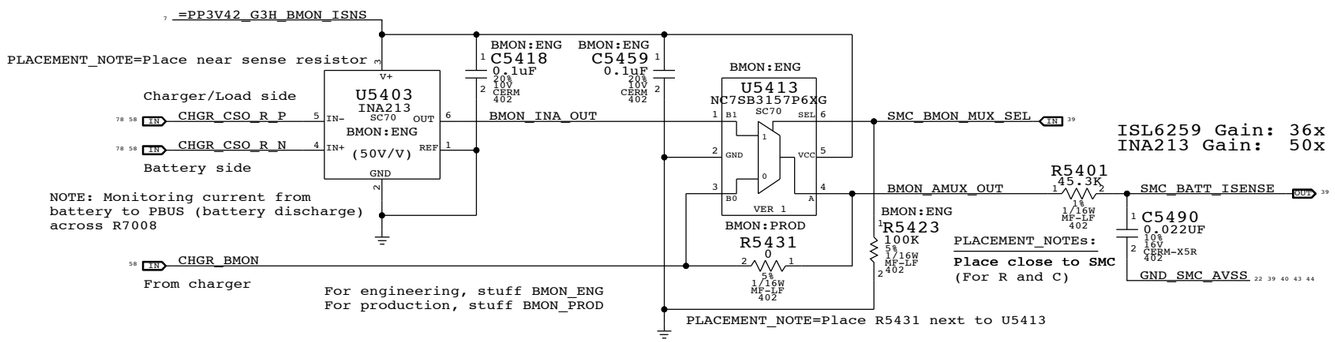
MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter



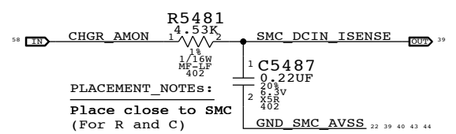
CPU VCore Load Side Current Sense / Filter



Battery (BMON) Current Sense, MUX & Filter



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=T27_MLB SYNC_DATE=09/30/2009

PAGE TITLE: Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

REVISION: A.13.0

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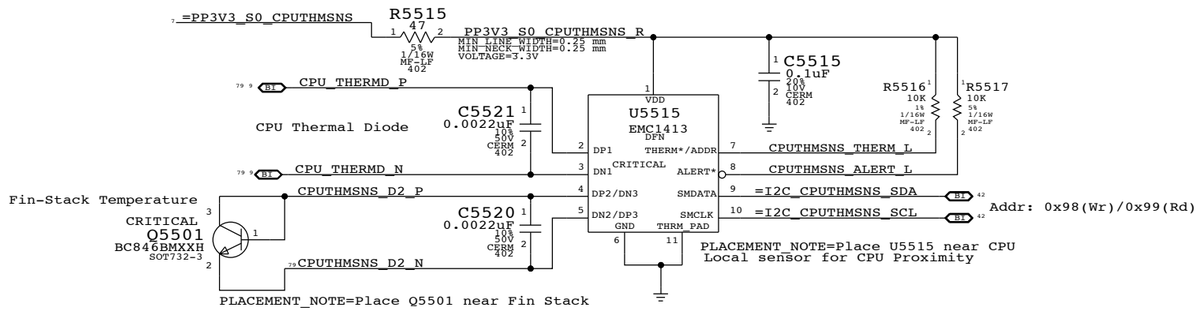
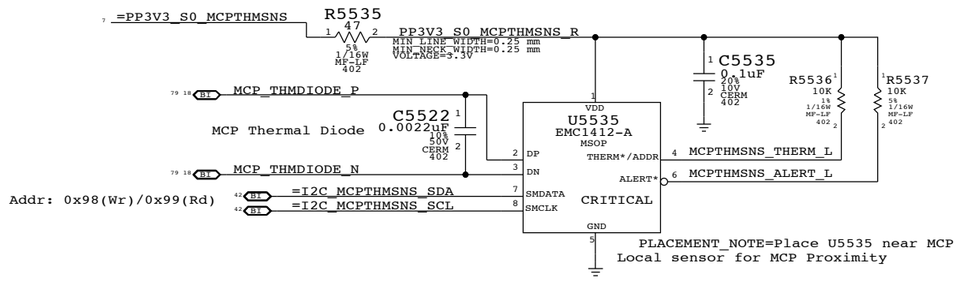
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



SYNC MASTER=T27 MLB SYNC DATE=08/27/2009

PAGE TITLE

Thermal Sensors

Apple Inc.

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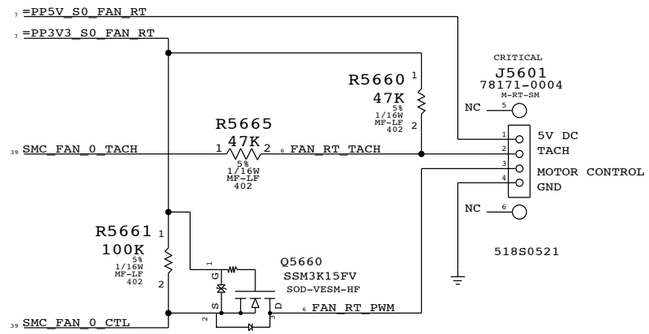

SYNC MASTER=K24 MLB SYNC DATE=07/20/2009

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

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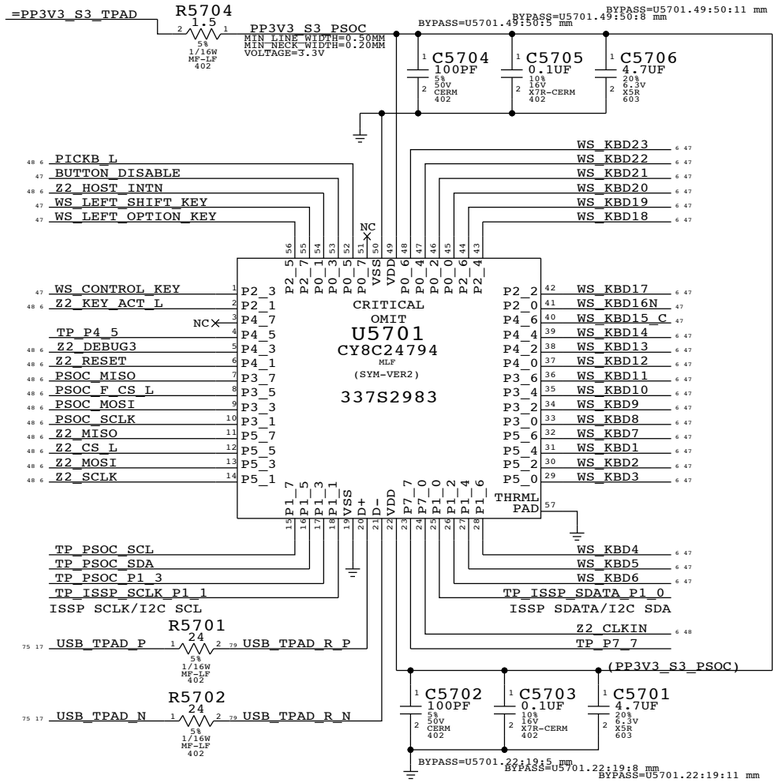
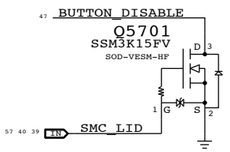
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

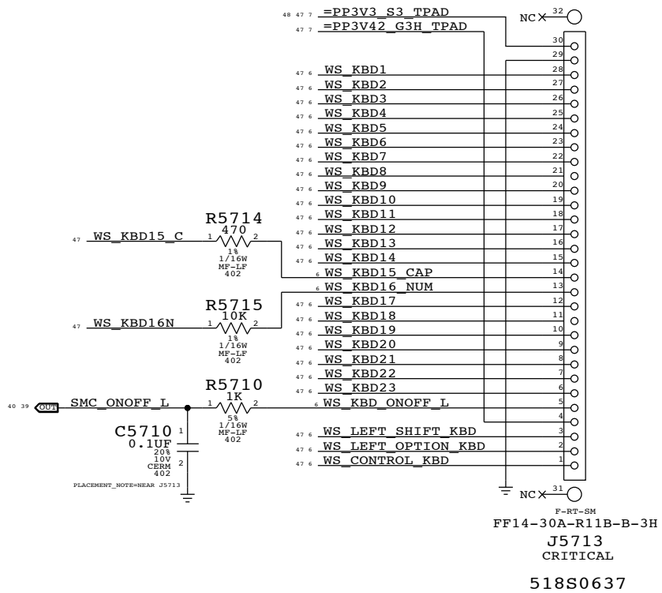


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

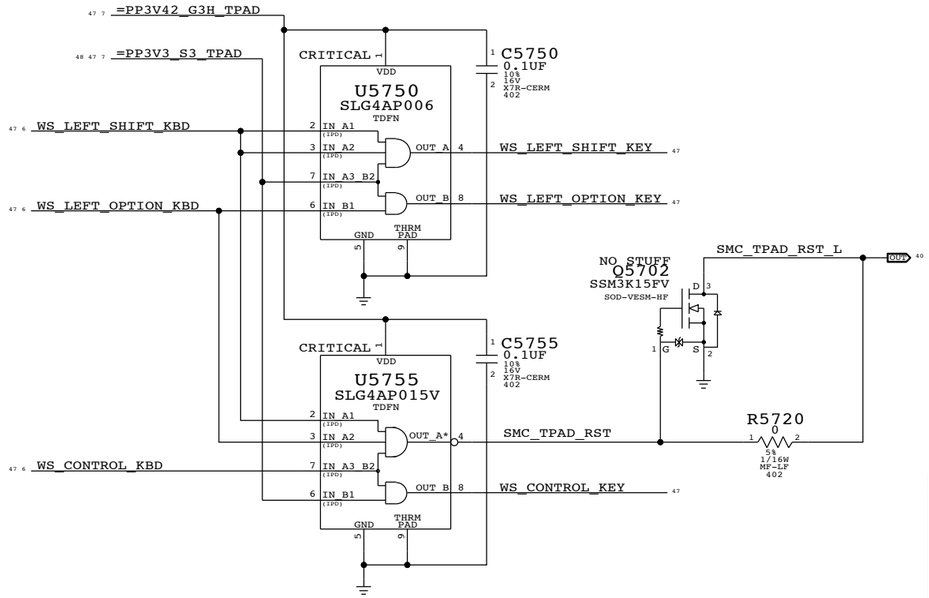
Keyboard Connector



518S0637

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



SYNC MASTER=T27 MLB	SYNC DATE=08/15/2009
PAGE TITLE: WELLSPRING 1	
Apple Inc.	DRAWING NUMBER: 051-8563 SIZE: D
	REVISION: A.13.0
	BRANCH:
	PAGE: 57 OF 109
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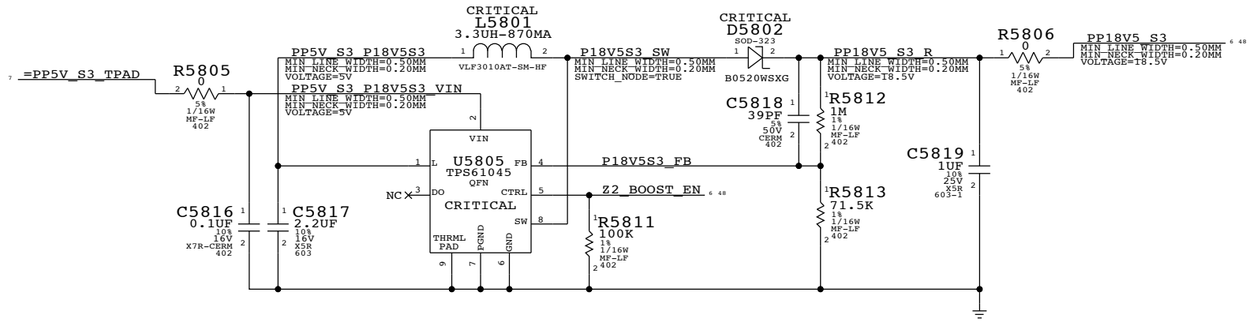
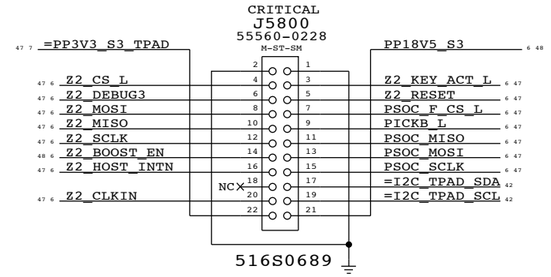
BOOSTER +18.5VDC FOR SENSORS

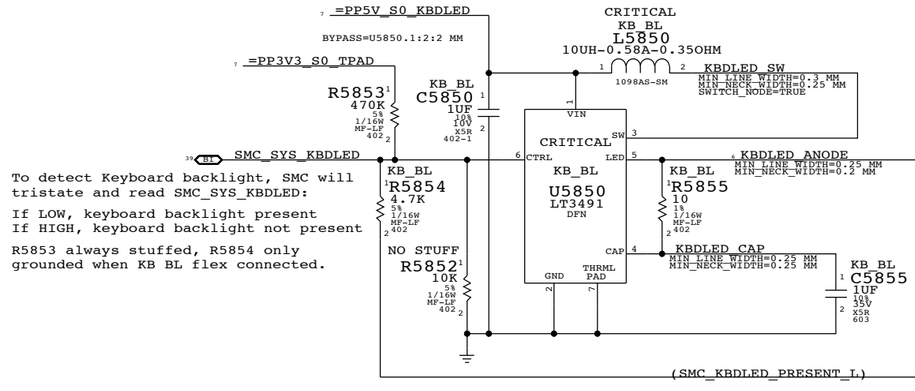
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

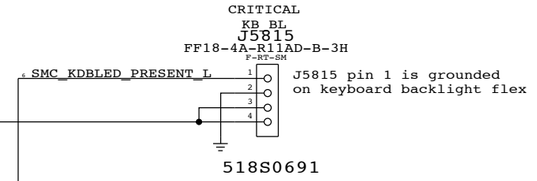


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



K6 NOTES : C5850 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=T27 MLB
SYNC DATE=08/03/2009

PAGE TITLE
WELLSPRING 2

Apple Inc.

DRAWING NUMBER 051-8563
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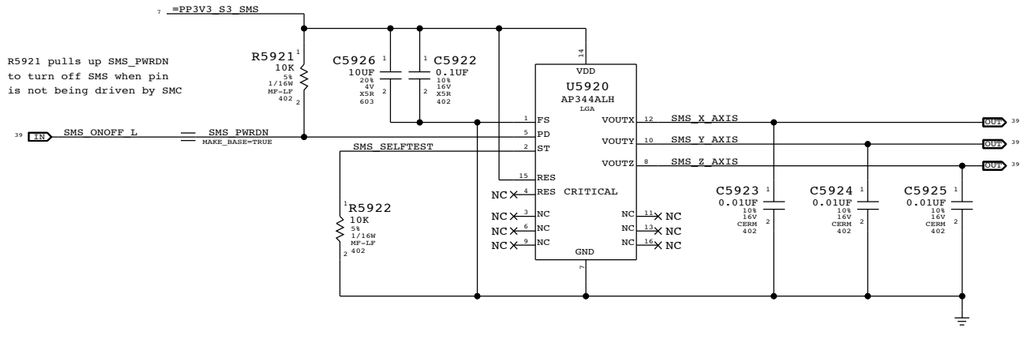
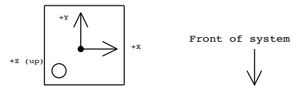
Analog SMS



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC MASTER=T27 MLB SYNC DATE=07/20/2009

PAGE TITLE

Sudden Motion Sensor (SMS)

Apple Inc.

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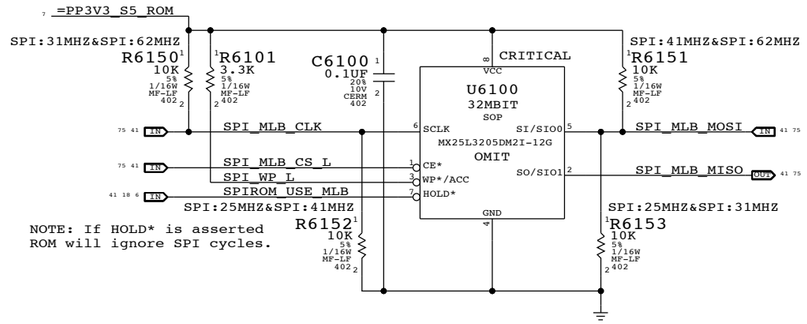

MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC MASTER=T27 MLB SYNC DATE=10/21/2009

PAGE TITLE

SPI ROM

Apple Inc.

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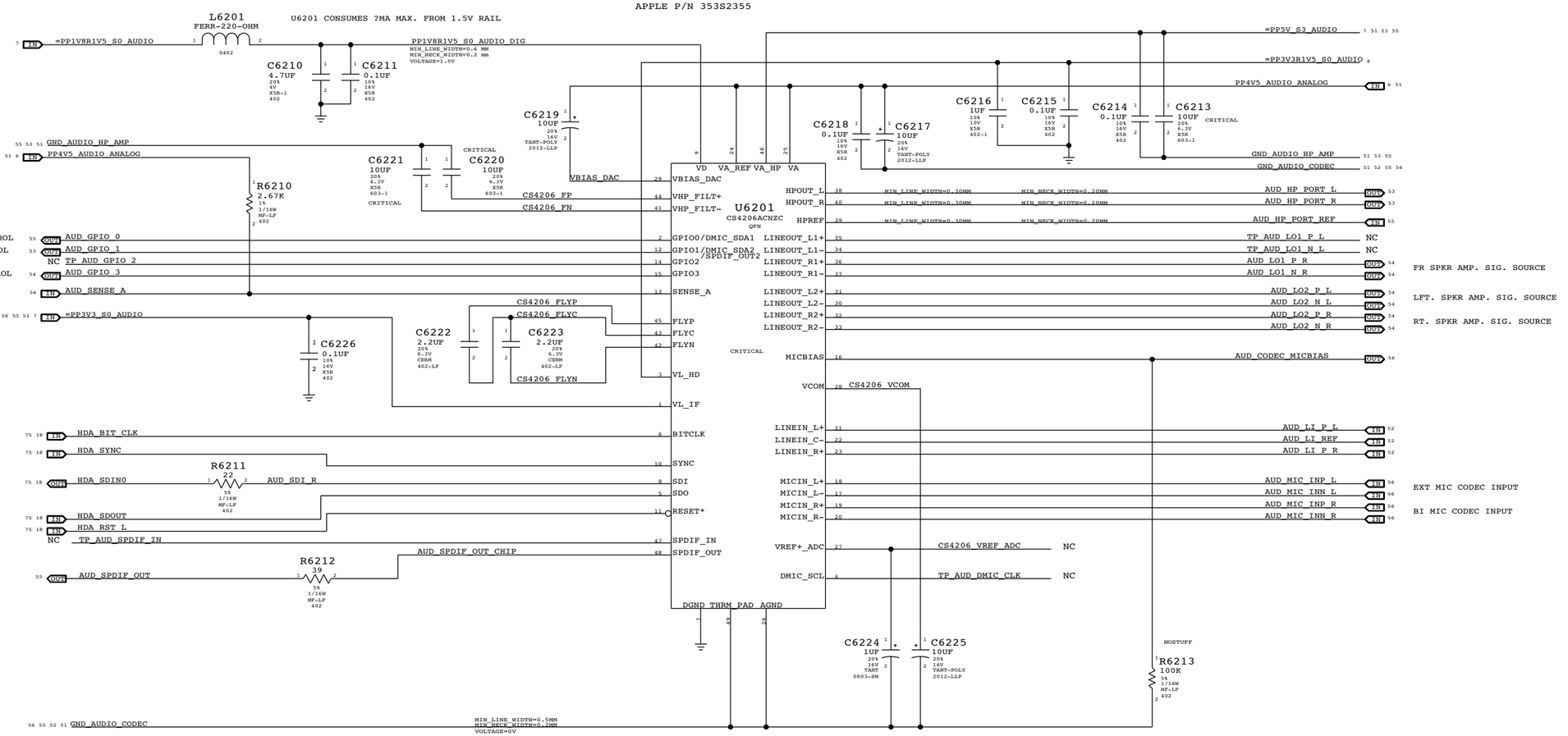
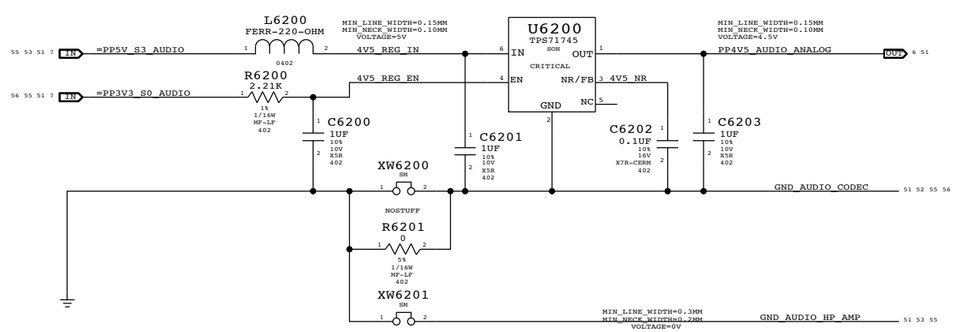
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=AUDIO
SYNC DATE=08/31/2005
PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-8563
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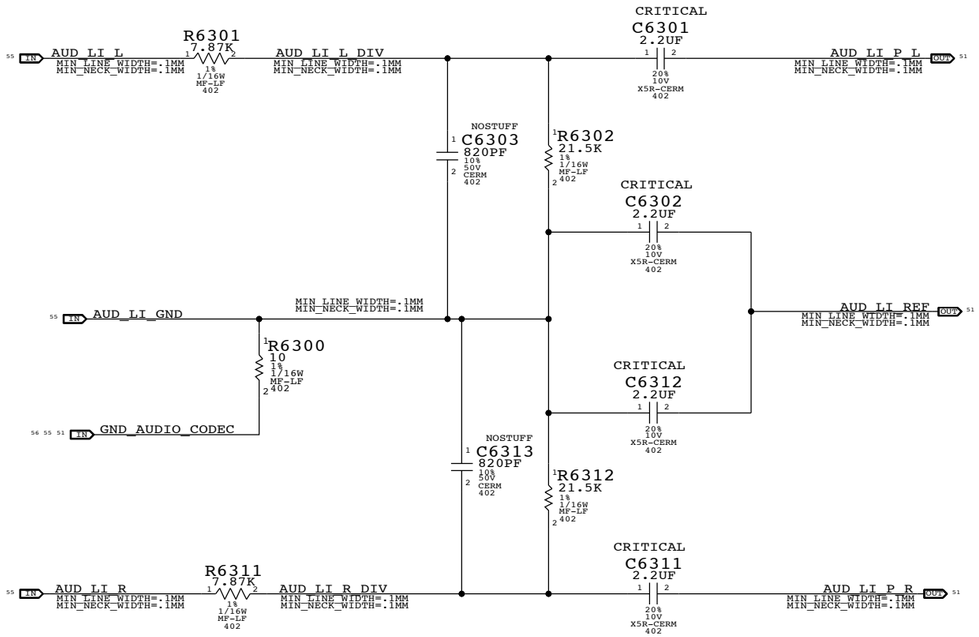
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER 051-8563 | SIZE D
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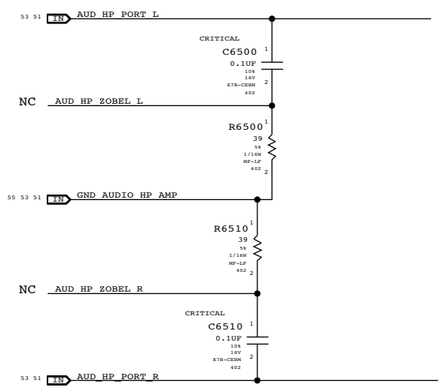
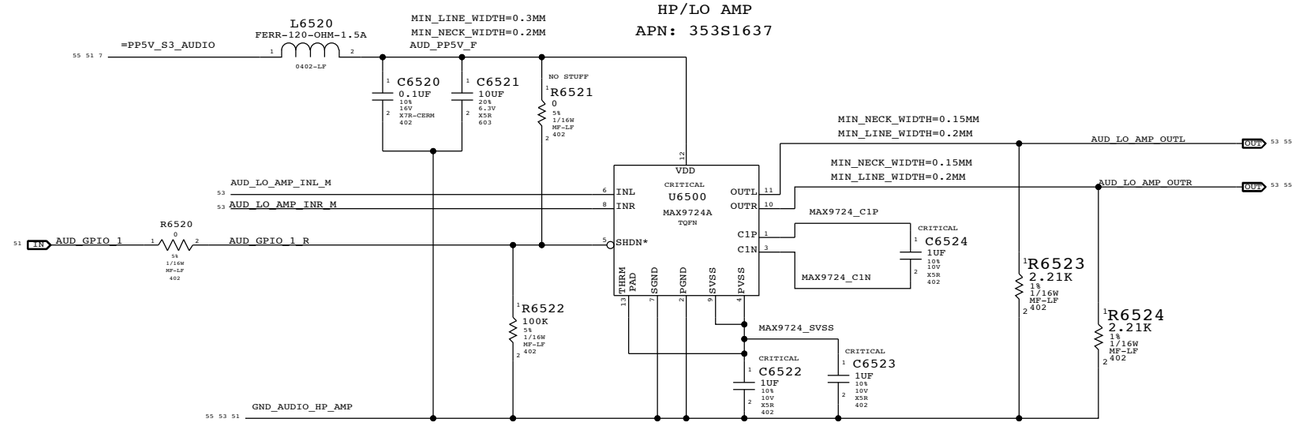
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



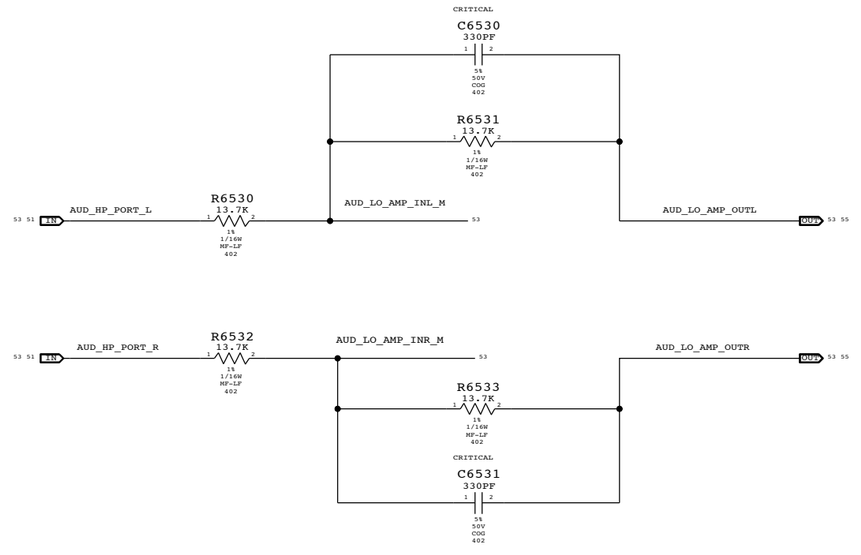
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC MASTER=AUDIO SYNC DATE=07/17/2009

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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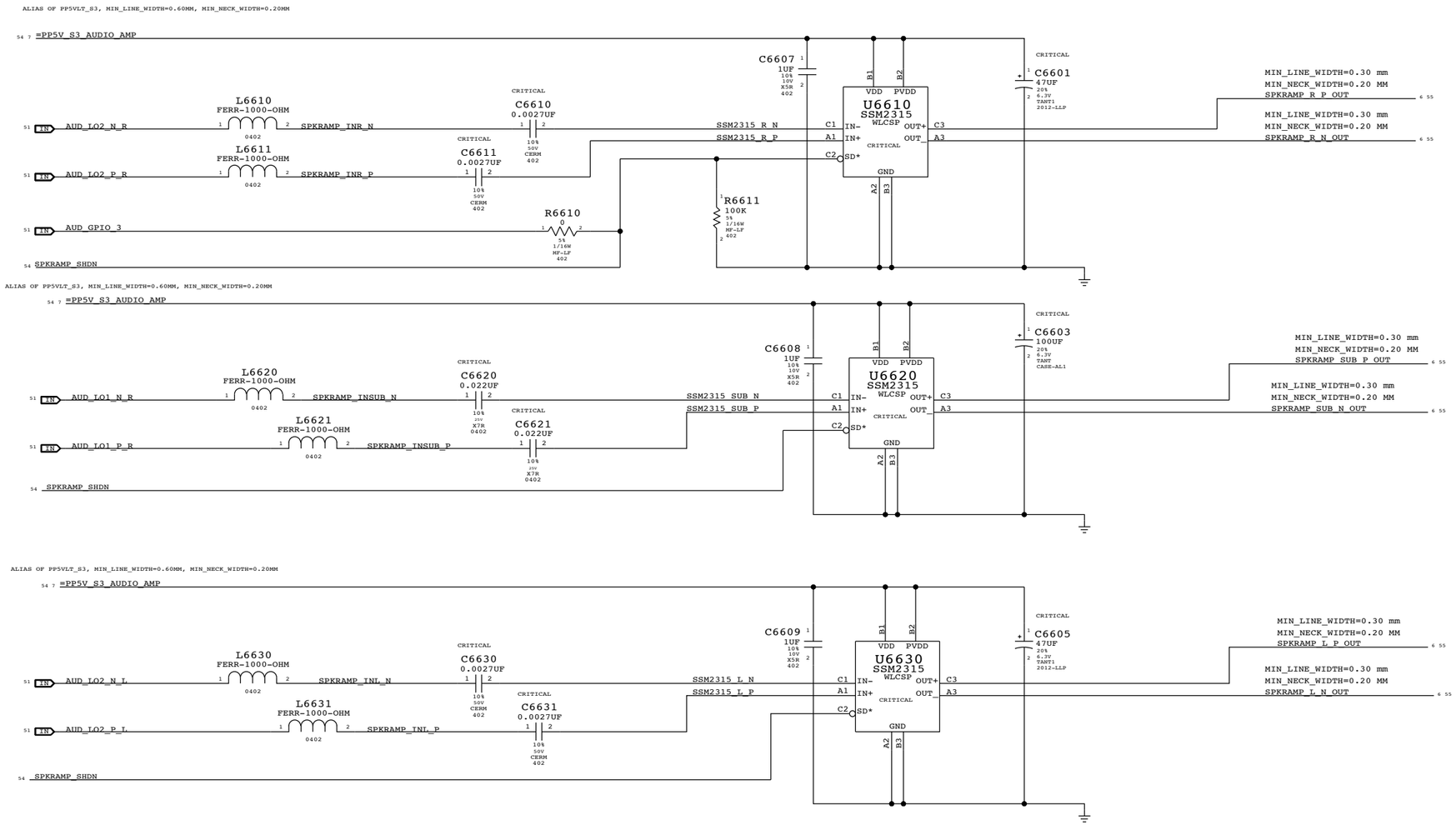
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2524

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC MASTER=AUDIO SYNC DATE=07/17/2009

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

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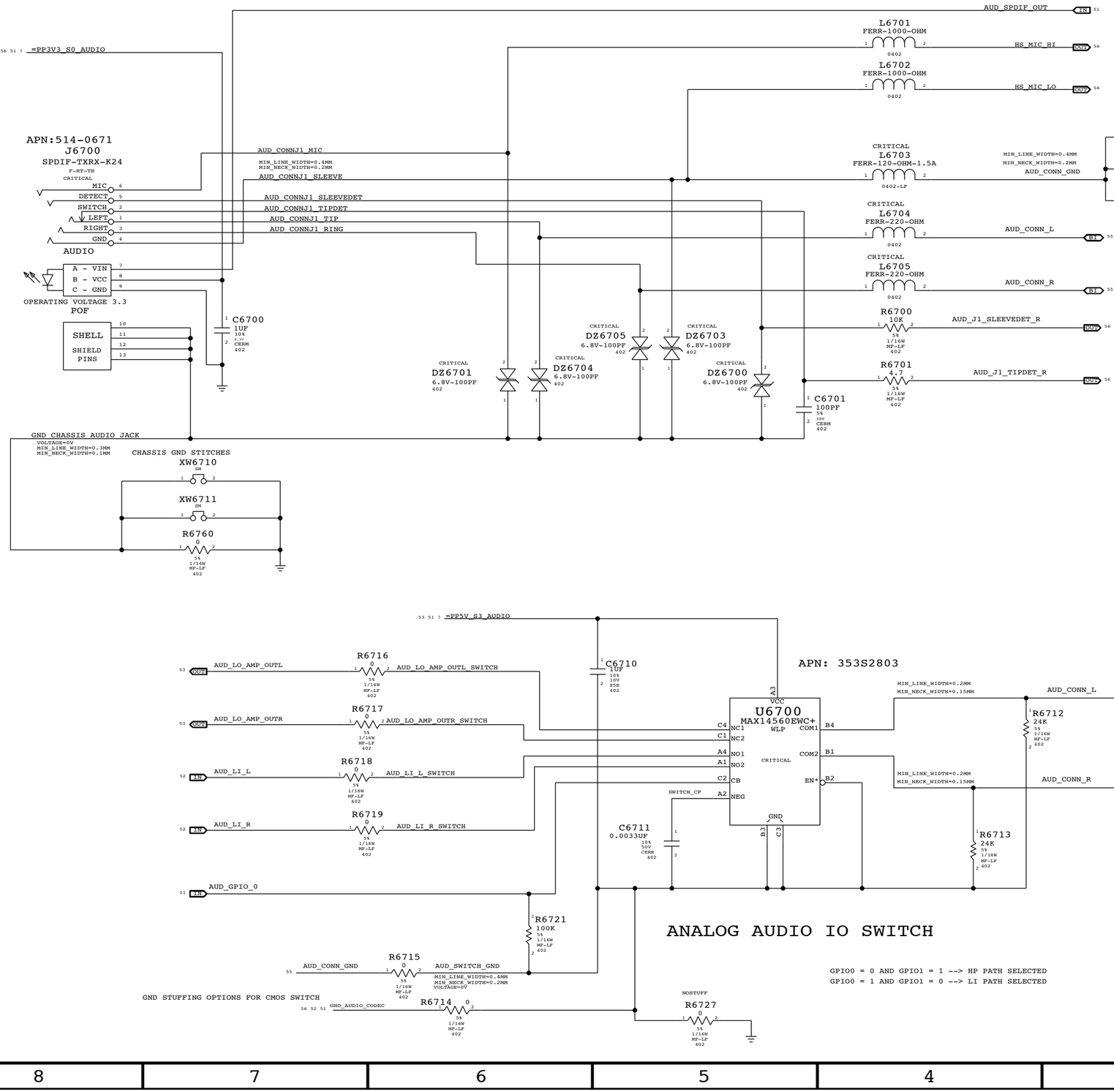
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



SYNC MASTER=AUDIO	SYNC DATE=08/25/2009
PAGE TITLE	AUDIO: JACK
Apple Inc.	DRAWING NUMBER 051-8563 · SIZE D
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CODEC OUTPUT SIGNAL PATHS

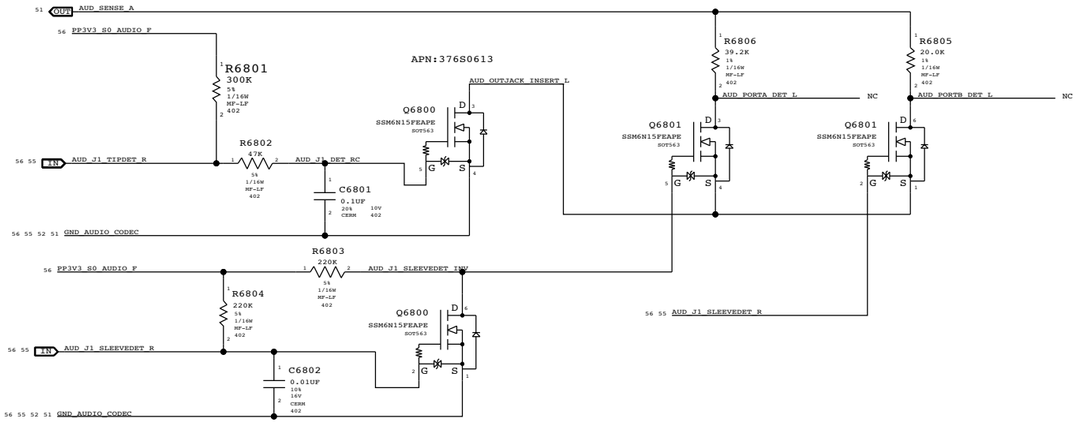
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

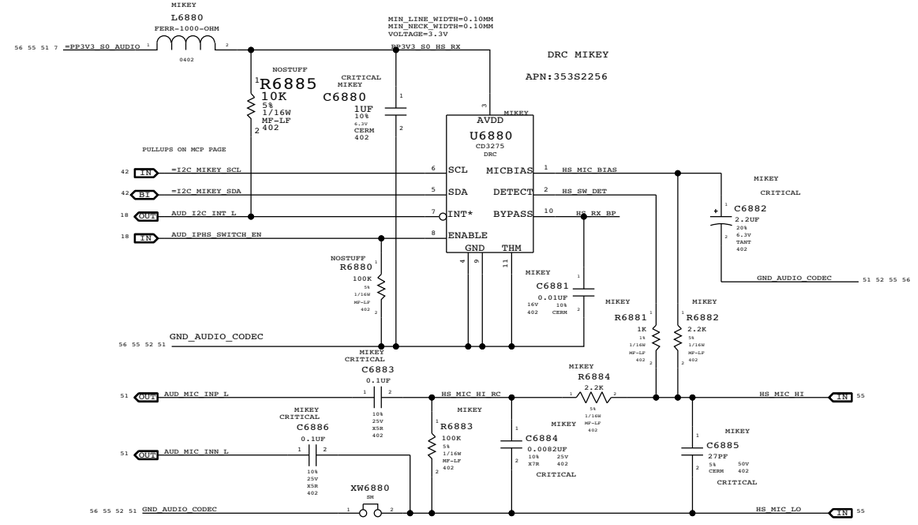
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

PORT A DETECT (HEADPHONES)

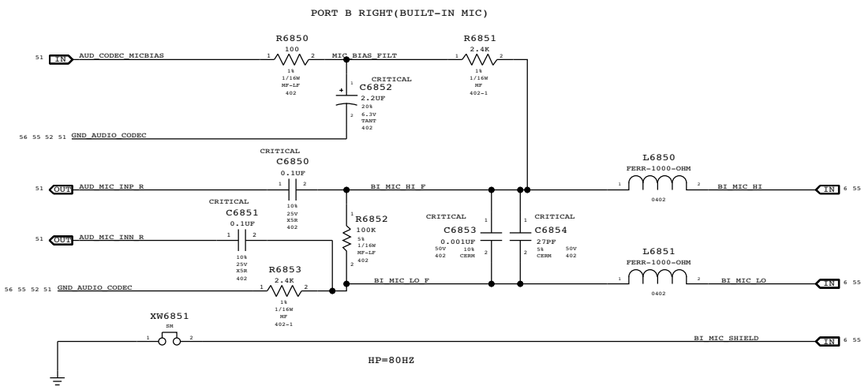
PORT B DETECT(SPDIF DELEGATE)



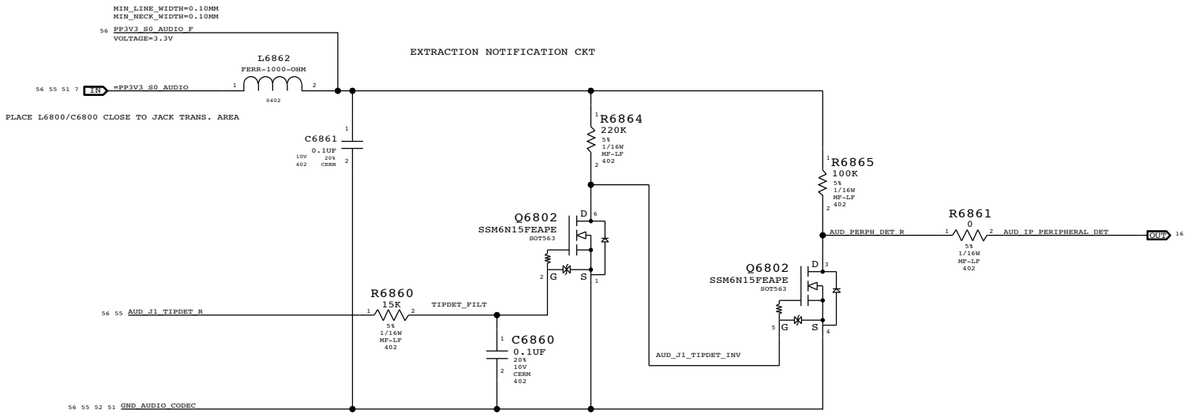
PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)



EXTRACTION NOTIFICATION CKT



SYNC MASTER=AUDIO	SYNC DATE=08/27/2009
PAGE TITLE	AUDIO: JACK TRANSLATORS
Apple Inc.	DRAWING NUMBER 051-8563 SIZE D
	REVISION A.13.0
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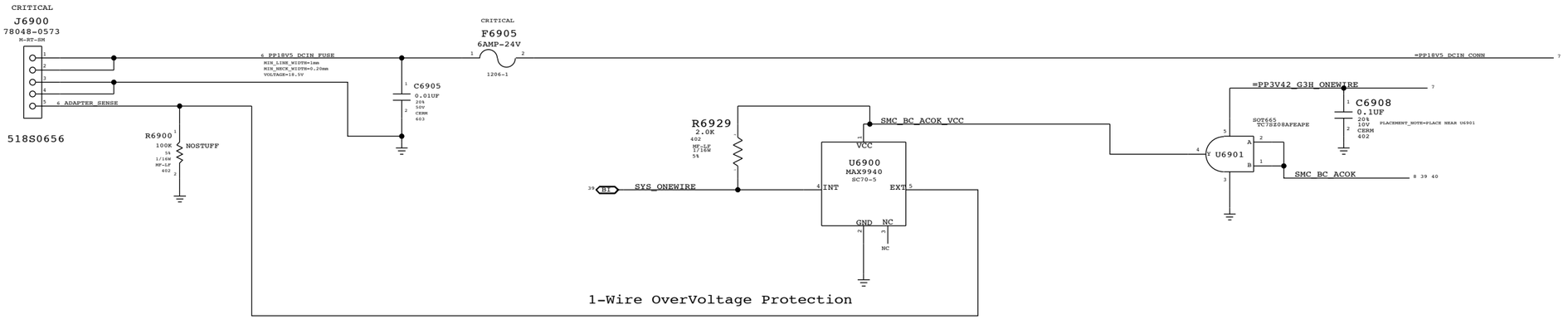
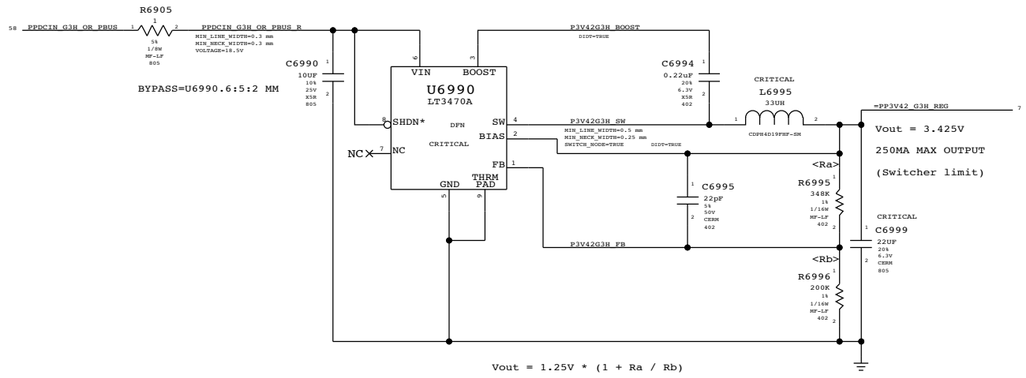
MagSafe DC Power Jack



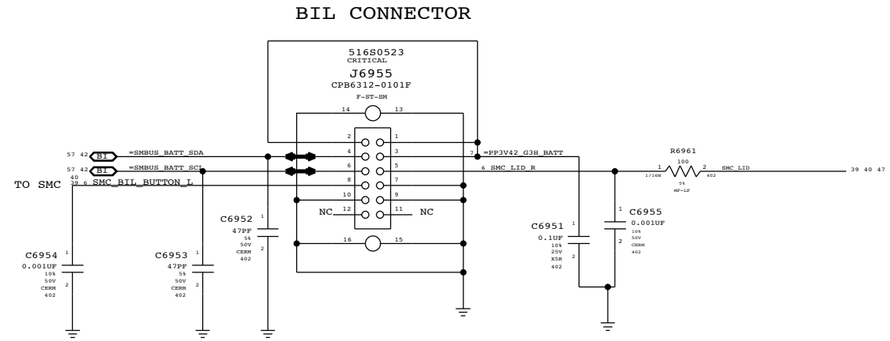
1-Wire OverVoltage Protection

3.425V "G3Hot" Supply

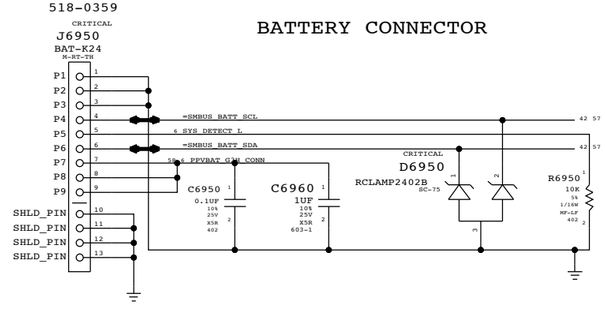
Supply needs to guarantee 3.31V delivered to SMC VRef generator



BIL CONNECTOR



BATTERY CONNECTOR



SYNC MASTER=K24 MLB	SYNC DATE=07/20/2009
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER 051-8563 SIZE D
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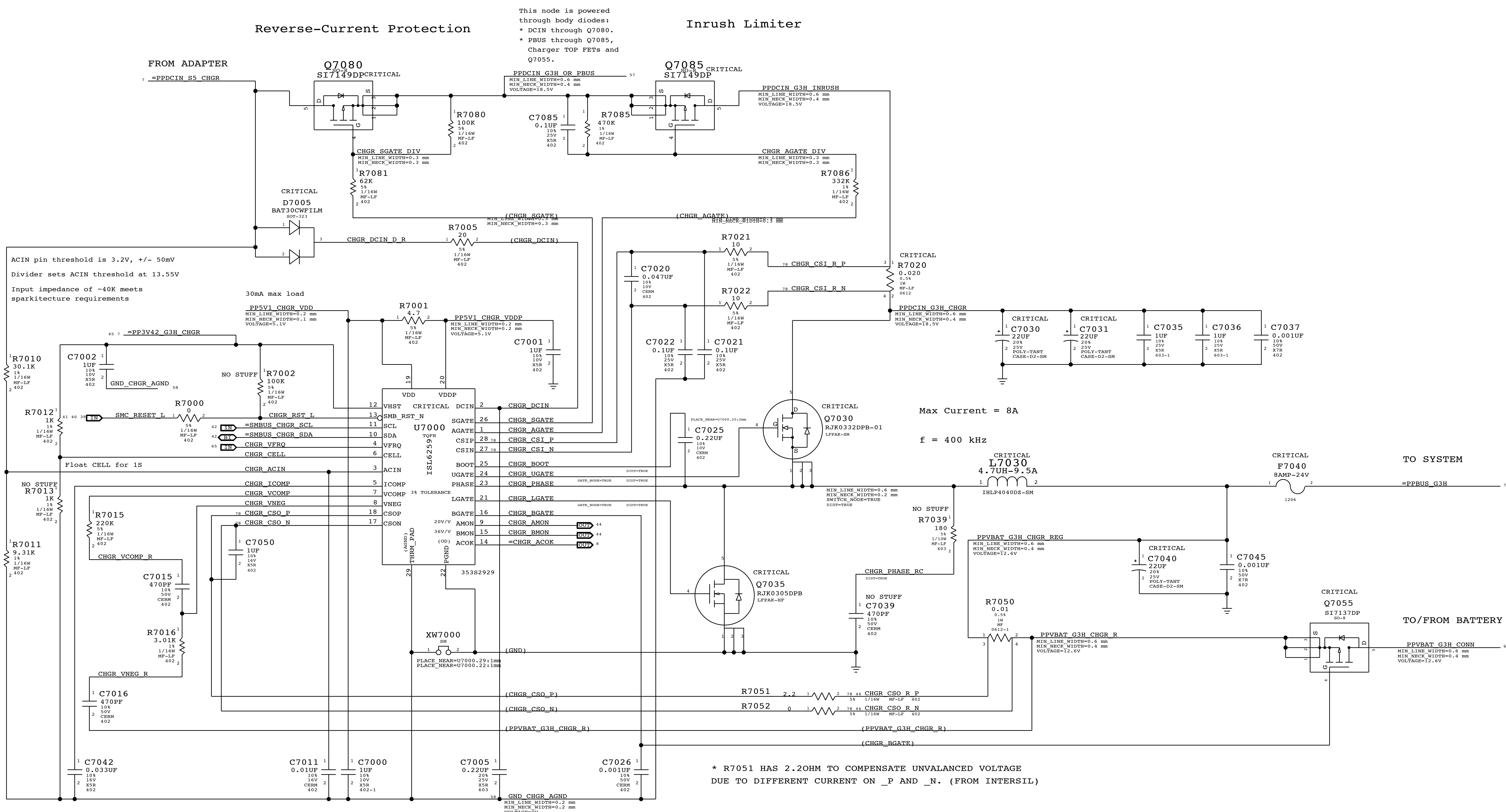

Reverse-Current Protection
Inrush Limiter
This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.
FROM ADAPTER
=PPDCIN_S5_CHGR
Q7080
SI7149DP
CRITICAL
PPDCIN_G3H_OR_PBUS
Q7085
SI7149DP
PPDCIN_G3H_INRUSH
R7080
100K
C7085
0.1UF
R7085
470K
CHGR_SGATE_DIV
CHGR_AGATE_DIV
R7081
62K
R7086
332K
D7005
BAT30CWFILM
R7005
20
CHGR_DCIN_D_R
ACIN pin threshold is 3.2V, +/- 50mV
Divider sets ACIN threshold at 13.55V
Input impedance of ~40K meets sparkitecture requirements
30mA max load
PP5V1_CHGR_VDD
R7001
4.7
PP5V1_CHGR_VDDP
C7001
1UF
R7021
10
R7022
10
C7020
0.047UF
R7020
0.020
CHGR_CSI_R_P
CHGR_CSI_R_N
PPDCIN_G3H_CHGR
C7030
22UF
C7031
22UF
C7035
1UF
C7036
1UF
C7037
0.001UF
R7010
30.1K
C7002
1UF
=PP3V42_G3H_CHGR
GND_CHGR_AGND
NO STUFF
R7002
100K
R7012
1K
R7000
0
SMC_RESET_L
CHGR_RST_L
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL
Float CELL for 1S
CHGR_ACIN
U7000
ISL6259
VHST
SMB_RST_N
SCL
SDA
VFRQ
CELL
ACIN
ICOMP
VCOMP
VNEG
CSOP
CSON
DCIN
SGATE
AGATE
CSIP
CSIN
BOOT
UGATE
PHASE
LGATE
BGATE
AMON
BMON
ACOK
THRM_PAD
PGND
353S2929
C7022
0.1UF
C7021
0.1UF
C7025
0.22UF
Q7030
RJK0332DPB-01
Max Current = 8A
f = 400 kHz
L7030
4.7UH-9.5A
F7040
8AMP-24V
TO SYSTEM
=PPBUS_G3H
R7013
1K
R7011
9.31K
R7015
220K
C7050
1UF
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_BGATE
CHGR_AMON
CHGR_BMON
=CHGR_ACOK
CHGR_VCOMP_R
C7015
470PF
R7016
3.01K
CHGR_VNEG_R
C7016
470PF
Q7035
RJK0305DPB
R7039
180
PPVBAT_G3H_CHGR_REG
C7040
22UF
C7045
0.001UF
CHGR_PHASE_RC
C7039
470PF
R7050
0.01
PPVBAT_G3H_CHGR_R
Q7055
SI7137DP
TO/FROM BATTERY
PPVBAT_G3H_CONN
XW7000
PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm
R7051
2.2
CHGR_CSO_R_P
R7052
0
CHGR_CSO_R_N
(CHGR_BGATE)
C7042
0.033UF
C7011
0.01UF
C7000
1UF
C7005
0.22UF
C7026
0.001UF
GND_CHGR_AGND
* R7051 HAS 2.2OHM TO COMPENSATE UNVALANCED VOLTAGE
DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

SYNC_MASTER=T27_MLB SYNC_DATE=07/29/2009

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

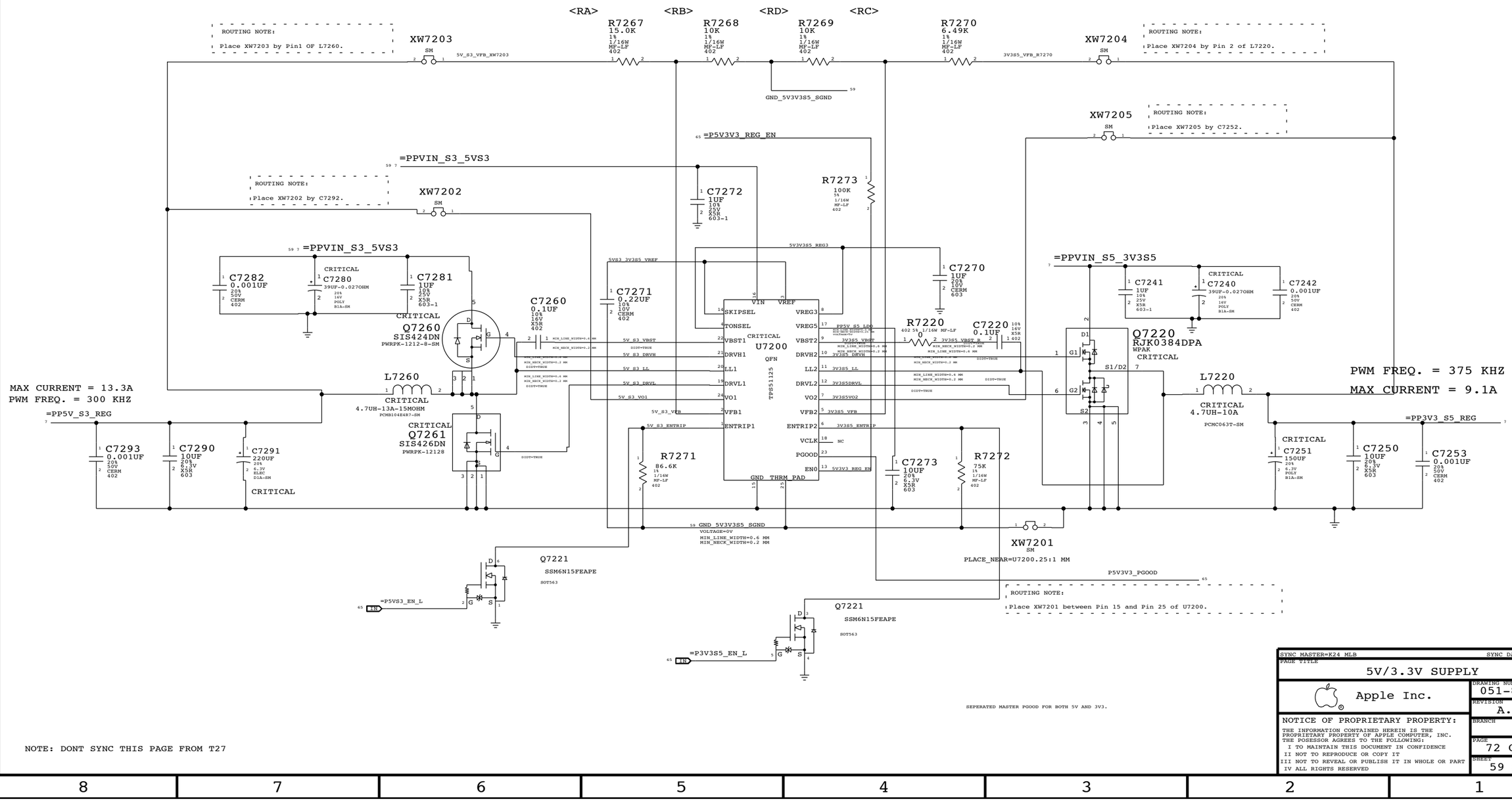
REVISION A.13.0

BRANCH

5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



NOTE: DONT SYNC THIS PAGE FROM T27

SYNC MASTER=K24 MLB
SYNC DATE=07/20/2005

PAGE TITLE
5V/3.3V SUPPLY

Apple Inc.

DRAWING NUMBER 051-8563
SIZE D
REVISION A.13.0
BRANCH
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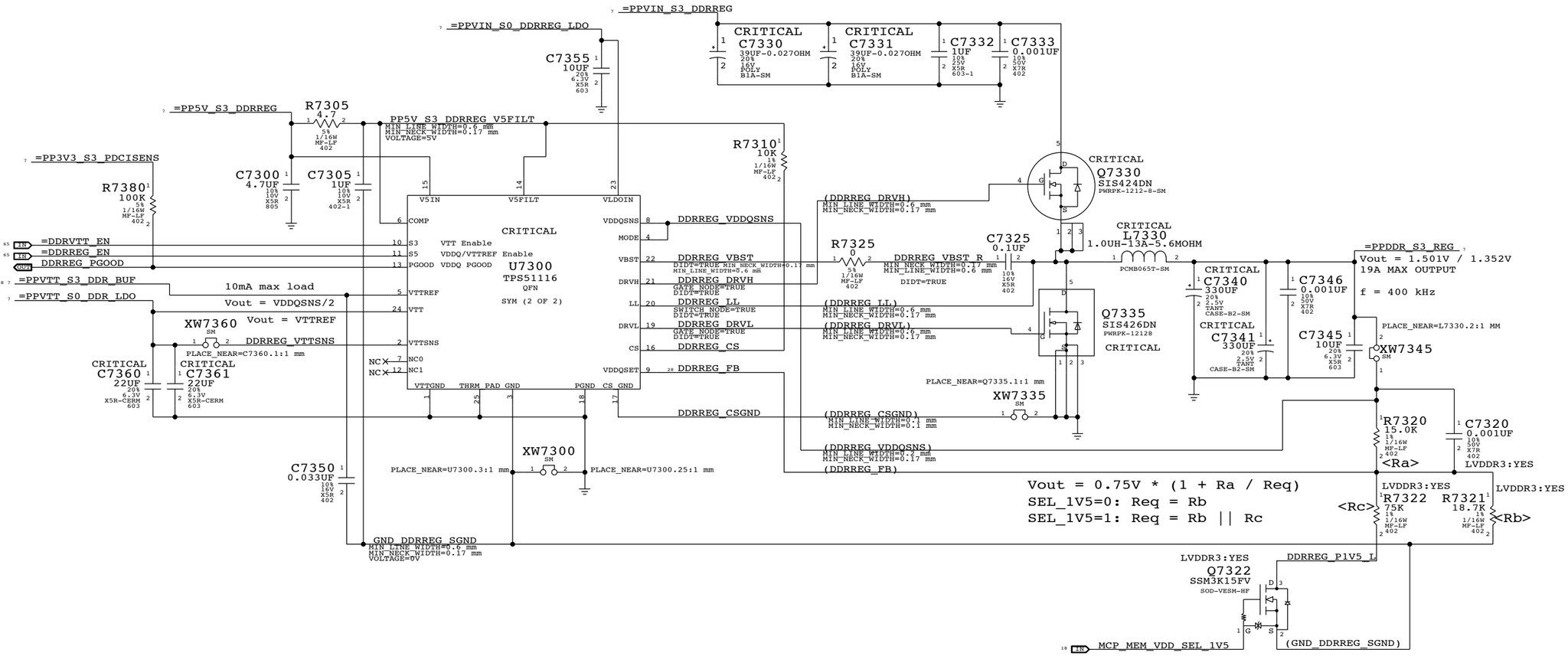

Use LVDDR3 for 1.5V/1.35V support or LVDDR3_NOT for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

NOTE: DONT SYNC THIS PAGE FROM T27. C7330 AND C7331 IS CHANGED TO OSCON CAPS

SYNC MASTER=T27 MLB SYNC DATE=08/06/2009

PAGE TITLE
1.5V/1.35V LVDDR3 Supply

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

REVISION A.13.0

BRANCH

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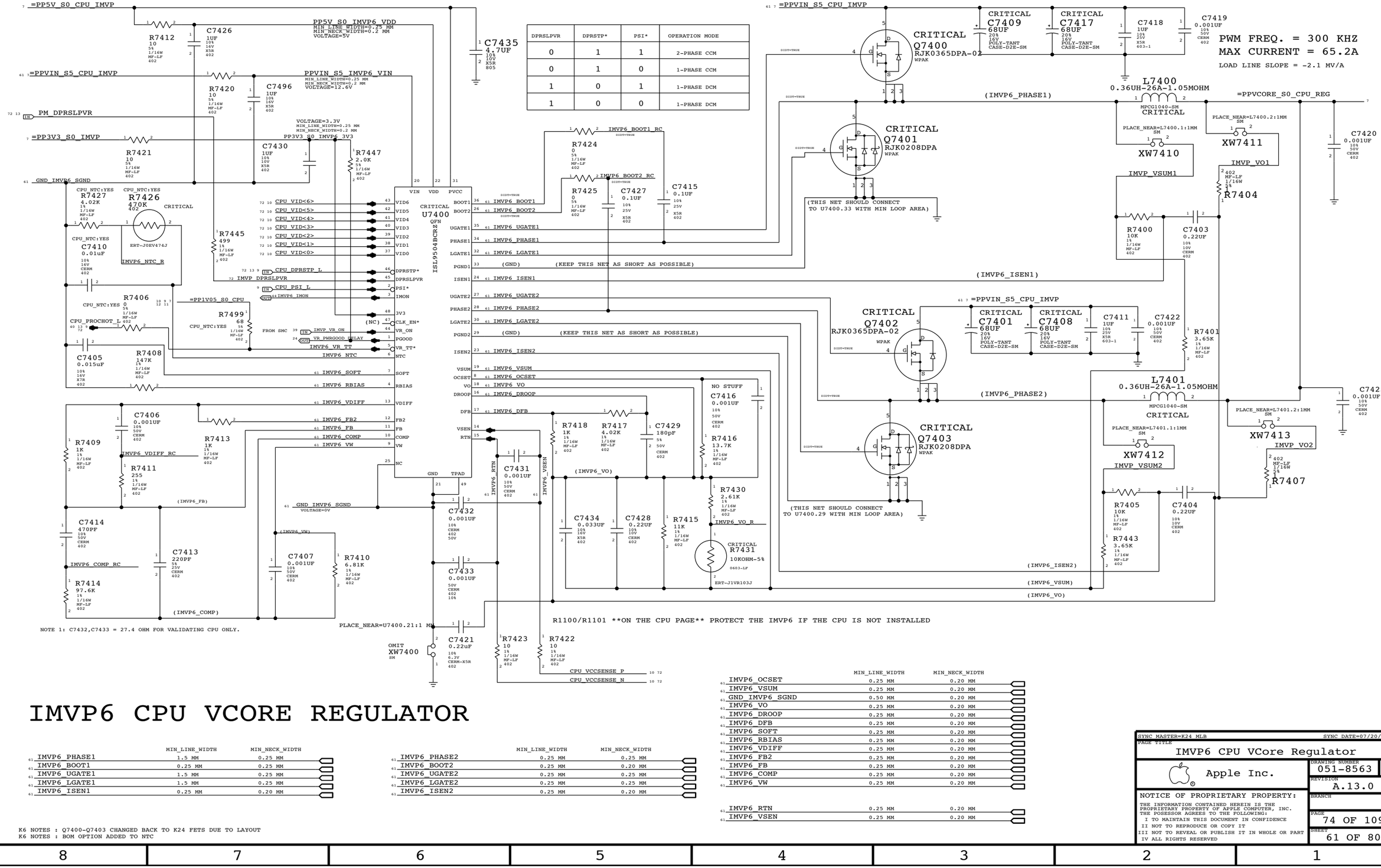

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.20 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_RTN	0.25 MM	0.20 MM
IMVP6_VSEN	0.25 MM	0.20 MM

K6 NOTES : Q7400-Q7403 CHANGED BACK TO K24 FETS DUE TO LAYOUT
K6 NOTES : BOM OPTION ADDED TO NTC

SYNC MASTER=K24 MLB
SYNC DATE=07/20/2005
PAGE TITLE
IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER 051-8563
SIZE D
REVISION A.13.0
BRANCH
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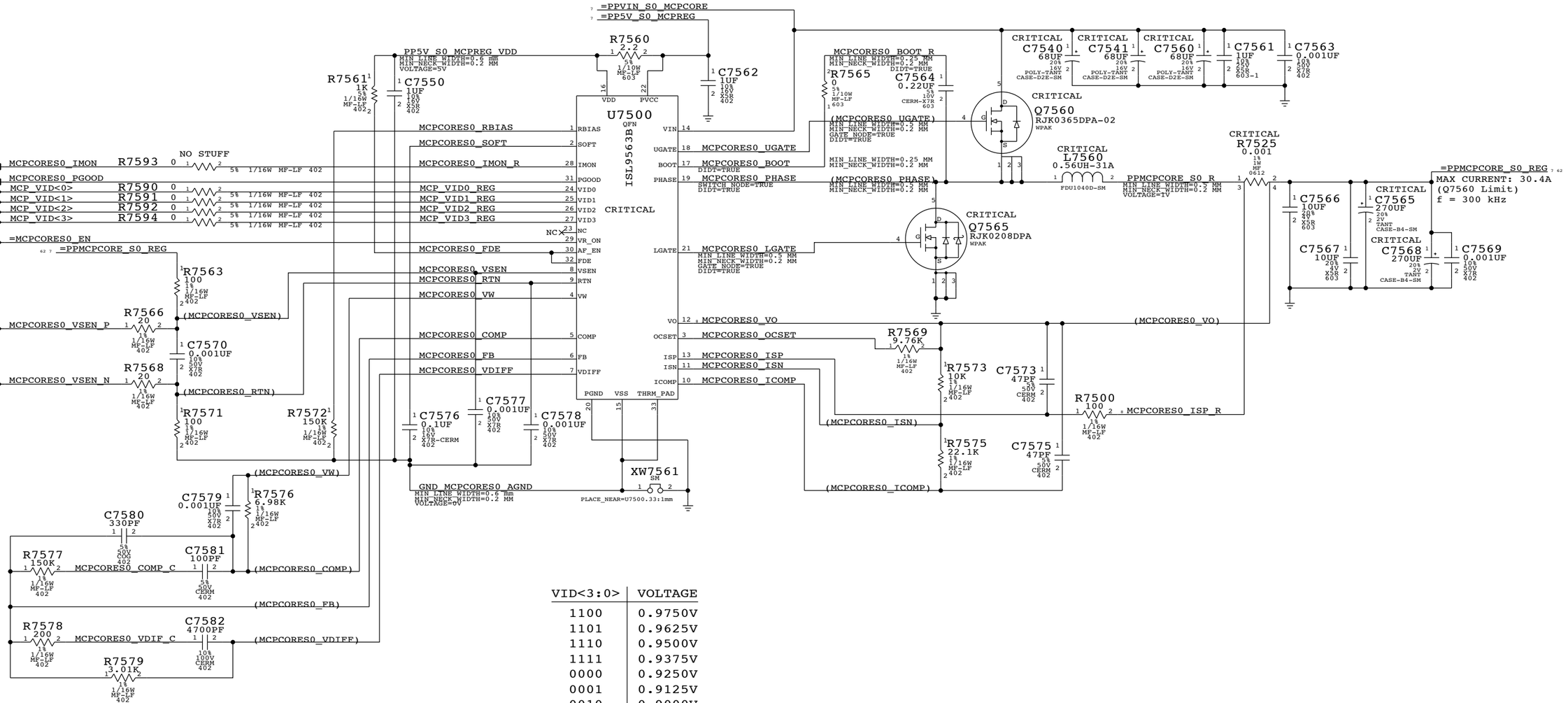

VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC MASTER=T27 MLB | SYNC DATE=08/18/2009

PAGE TITLE: MCP VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8563 | SIZE: D

REVISION: A.13.0

BRANCH:

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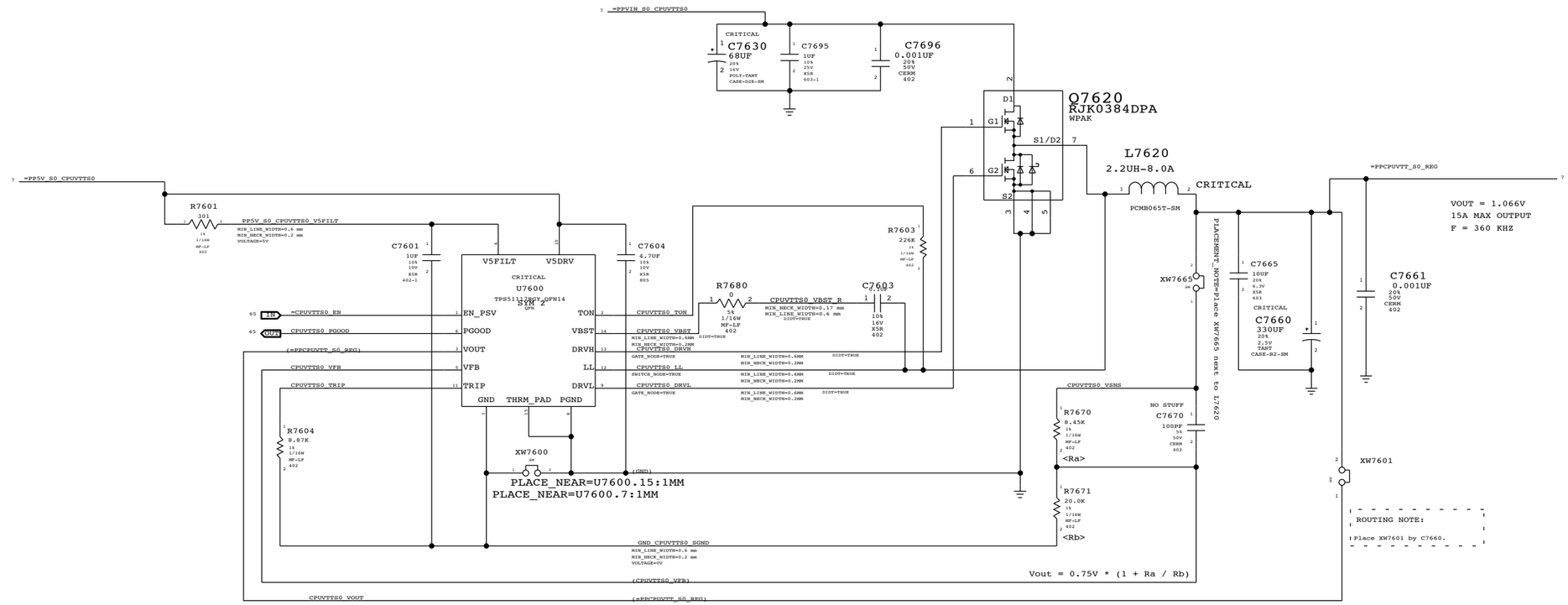
CPUVTT POWER SUPPLY



K6 NOTES : Q7620 CHANGED BACK TO K24 FETS DUE TO LAYOUT

SYNC MASTER=K24_MLB | SYNC DATE=07/20/2009

PAGE TITLE: CPU VTT(1.05V) SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8563 | SIZE: D

REVISION: A.13.0

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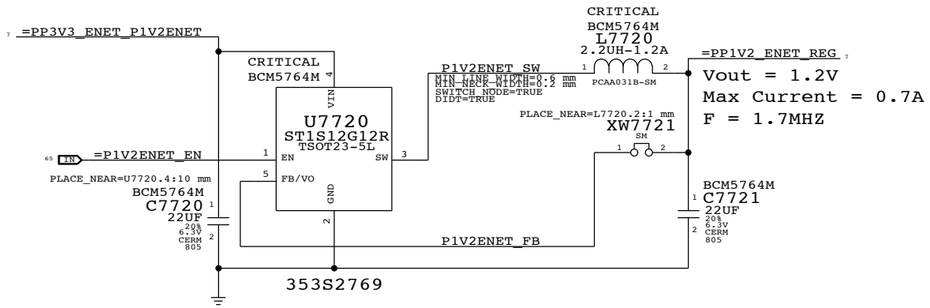
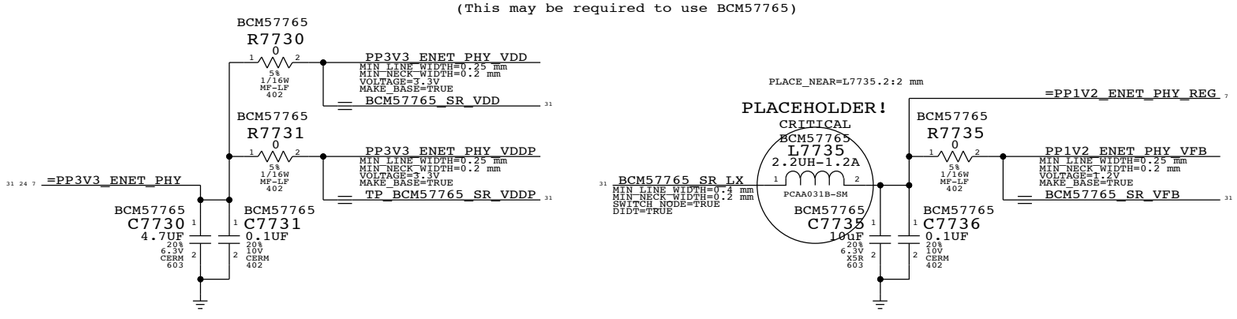
1.2V ENET Switcher

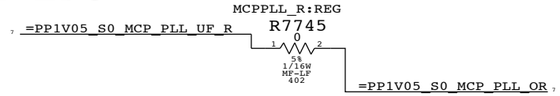


BCM57765 Internal Switcher Support

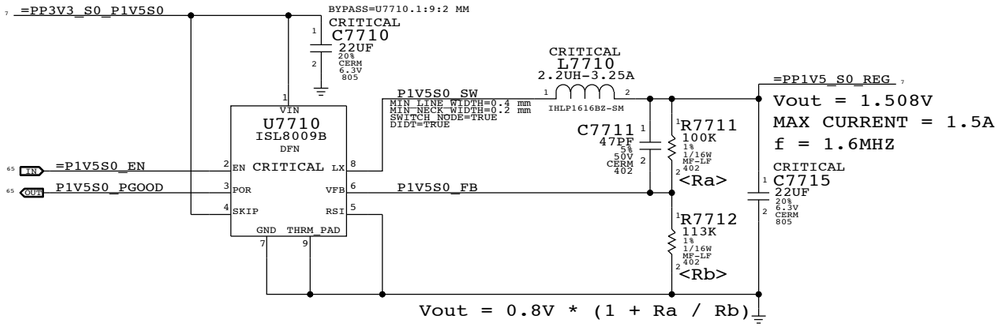
(This may be required to use BCM57765)



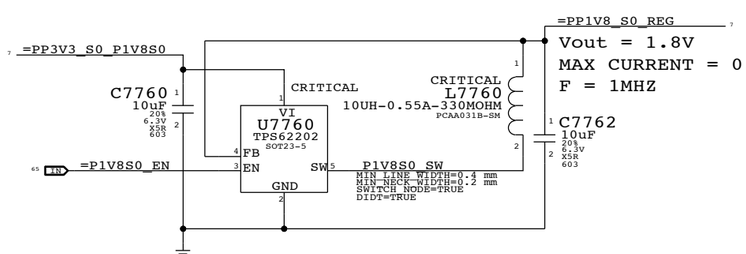
1.05V S0 MCP PLL LDO



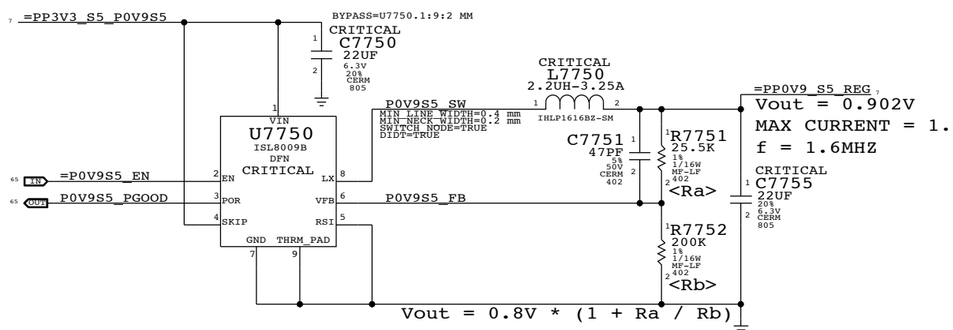
1.5V S0 Regulator



1.8V S0 Switcher



MCP 0.9V S5 (AUXC) Switcher



BOMOPTIONs:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

K6 NOTES : C7710 AND C7750 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=T27 MLB SYNC DATE=09/30/2009

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D
REVISION: A.13.0
BRANCH:
PAGE: 77 OF 109
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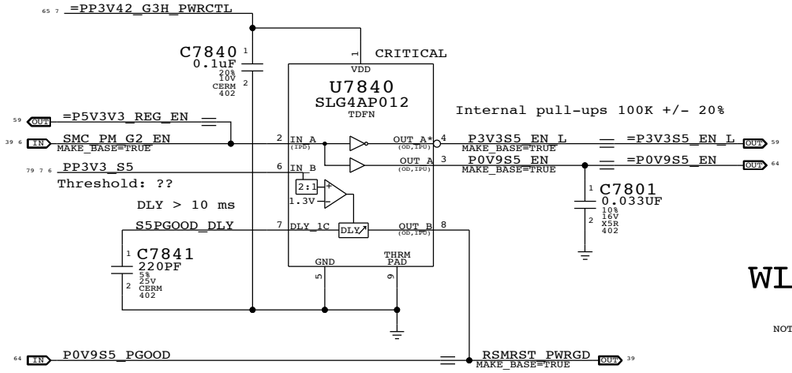
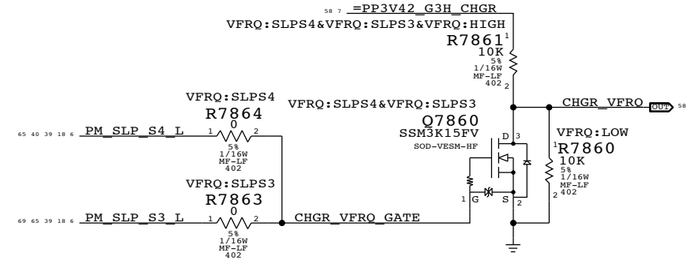
S5 Rail Enables & PGOOD



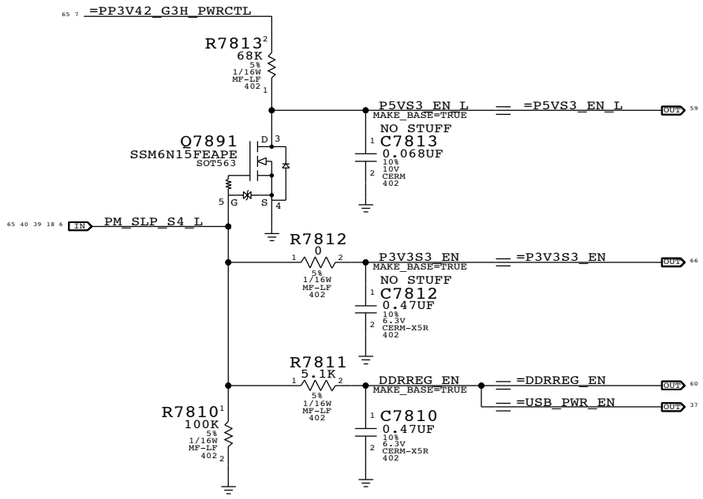
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

ISL6259 Frequency Select



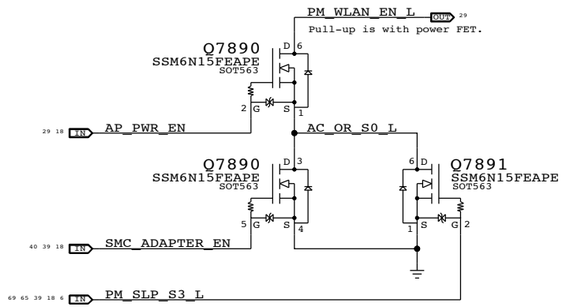
S3 Rail Enables



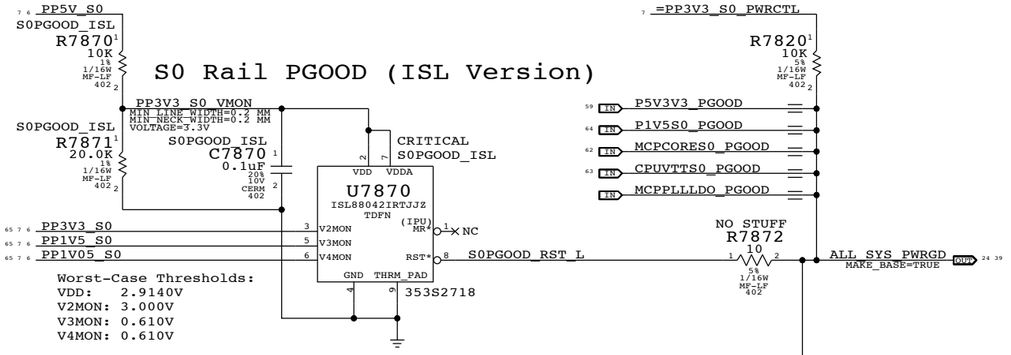
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

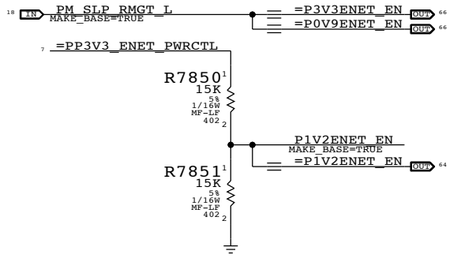
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



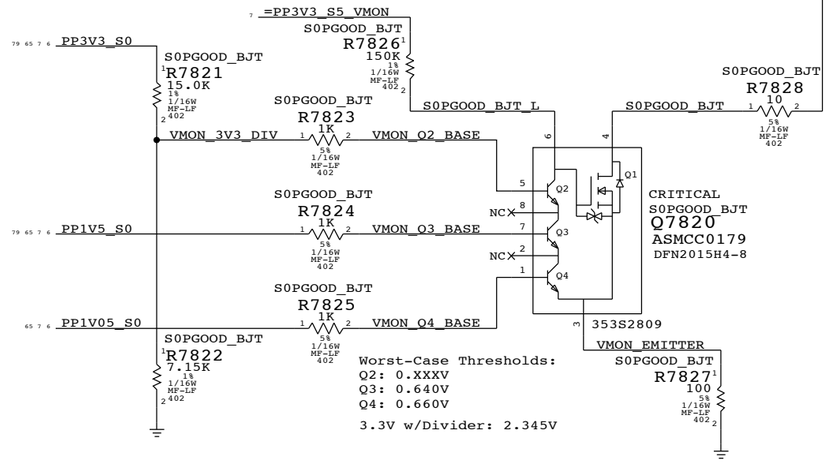
S0 Rail PGOOD Circuitry



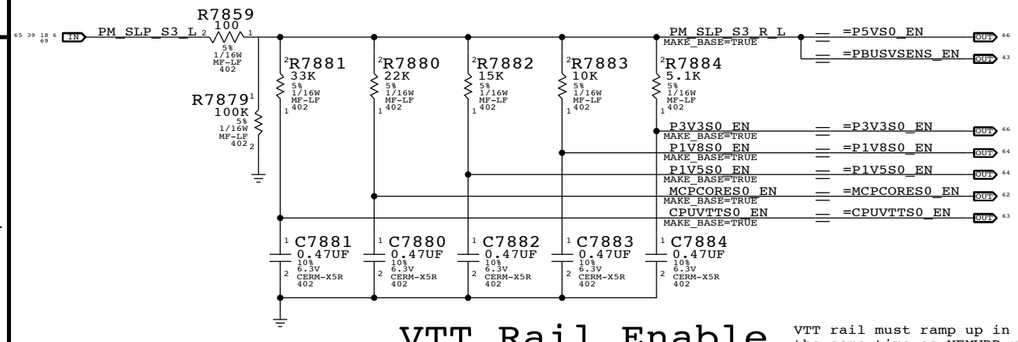
ENET Rail Enables



S0 Rail PGOOD (BJT Version)



S0 Rail Enables



VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

K6 HAS A PULL UP ON DDRREG PGOOD. REMOVED ALIAS TO TP SIGNAL

SYNC MASTER=T27_MLB SYNC DATE=11/24/2009

PAGE TITLE: Power Sequencing

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

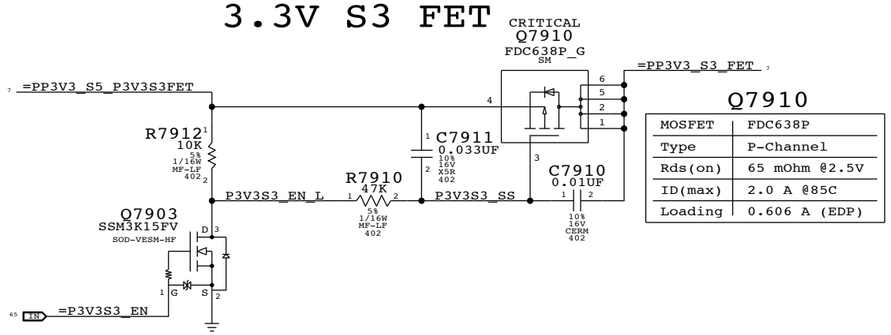
REVISION: A.13.0

BRANCH:

PAGE: 78 OF 109

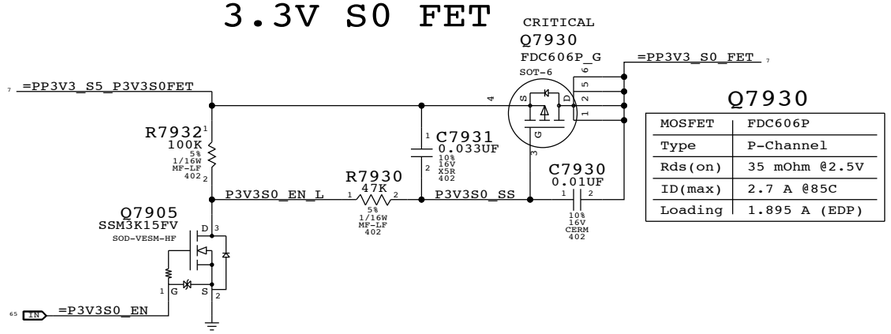
SHEET: 65 OF 80

3.3V S3 FET



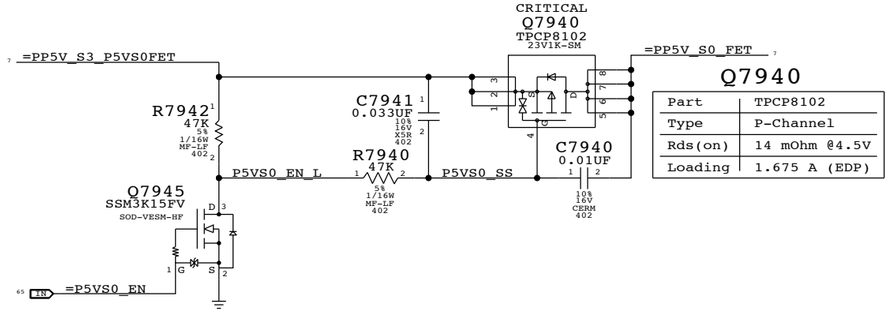
Q7910	
MOSFET	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	0.606 A (EDP)

3.3V S0 FET



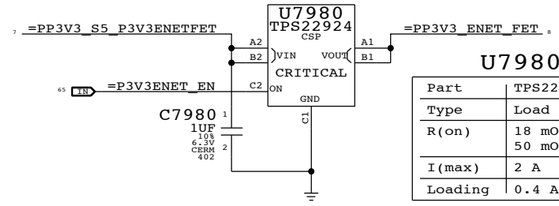
Q7930	
MOSFET	FDC606P
Type	P-Channel
Rds(on)	35 mOhm @2.5V
ID(max)	2.7 A @85C
Loading	1.895 A (EDP)

5V S0 FET



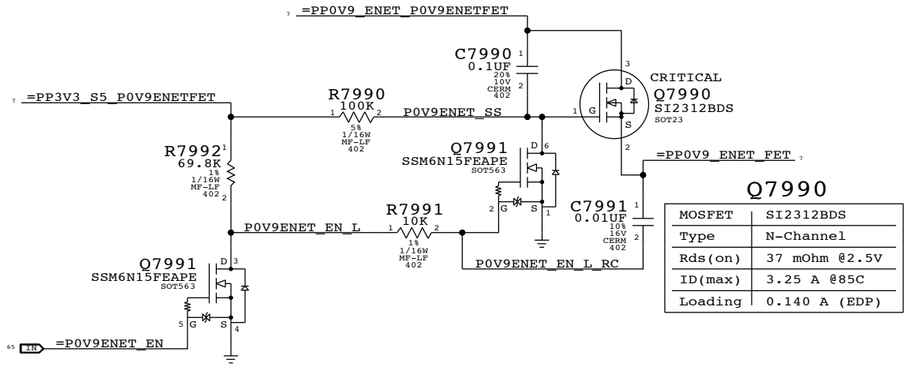
Q7940	
Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
Loading	1.675 A (EDP)

3.3V ENET Switch

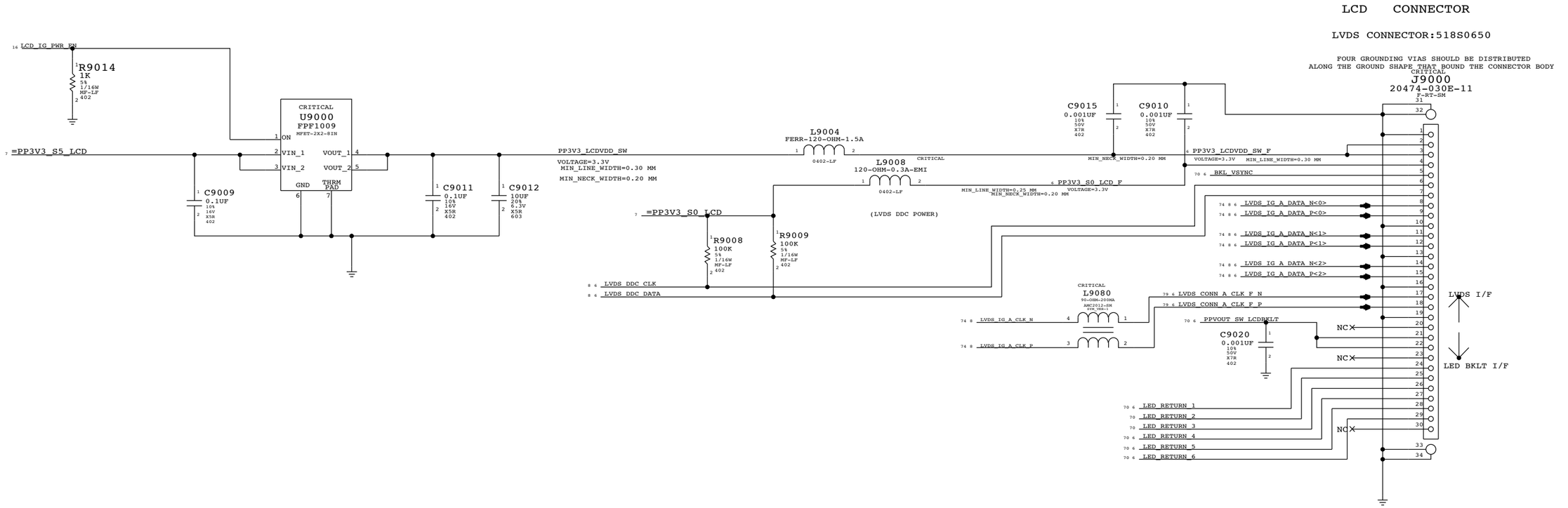


U7980	
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max
I(max)	2 A
Loading	0.4 A (EDP)

0.9V ENET FET



Q7990	
MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)



SYNC MASTER=K24 MLB	SYNC DATE=07/20/2009
PAGE TITLE: LVDS CONNECTOR	
Apple Inc.	DRAWING NUMBER: 051-8563 SIZE: D
	REVISION: A.13.0
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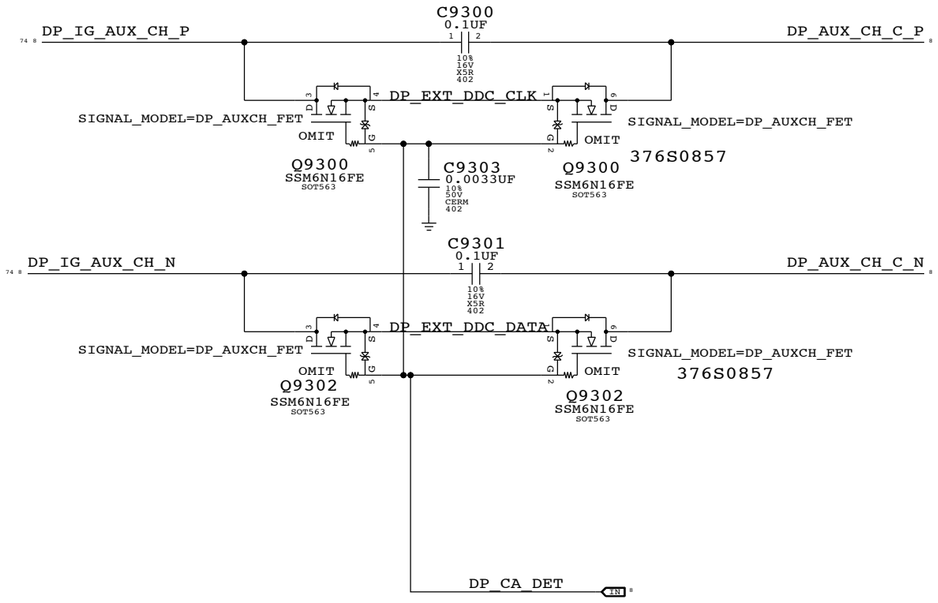
	SHEET: 67 OF 80



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0859	2	XSTR,FT,N-CH,DUAL,SOT-563	Q9300,Q9302	CRITICAL	

SYNC MASTER=K69_MLB SYNC DATE=08/12/2009

PAGE TITLE

DISPLAYPORT SUPPORT

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

REVISION A.13.0

BRANCH

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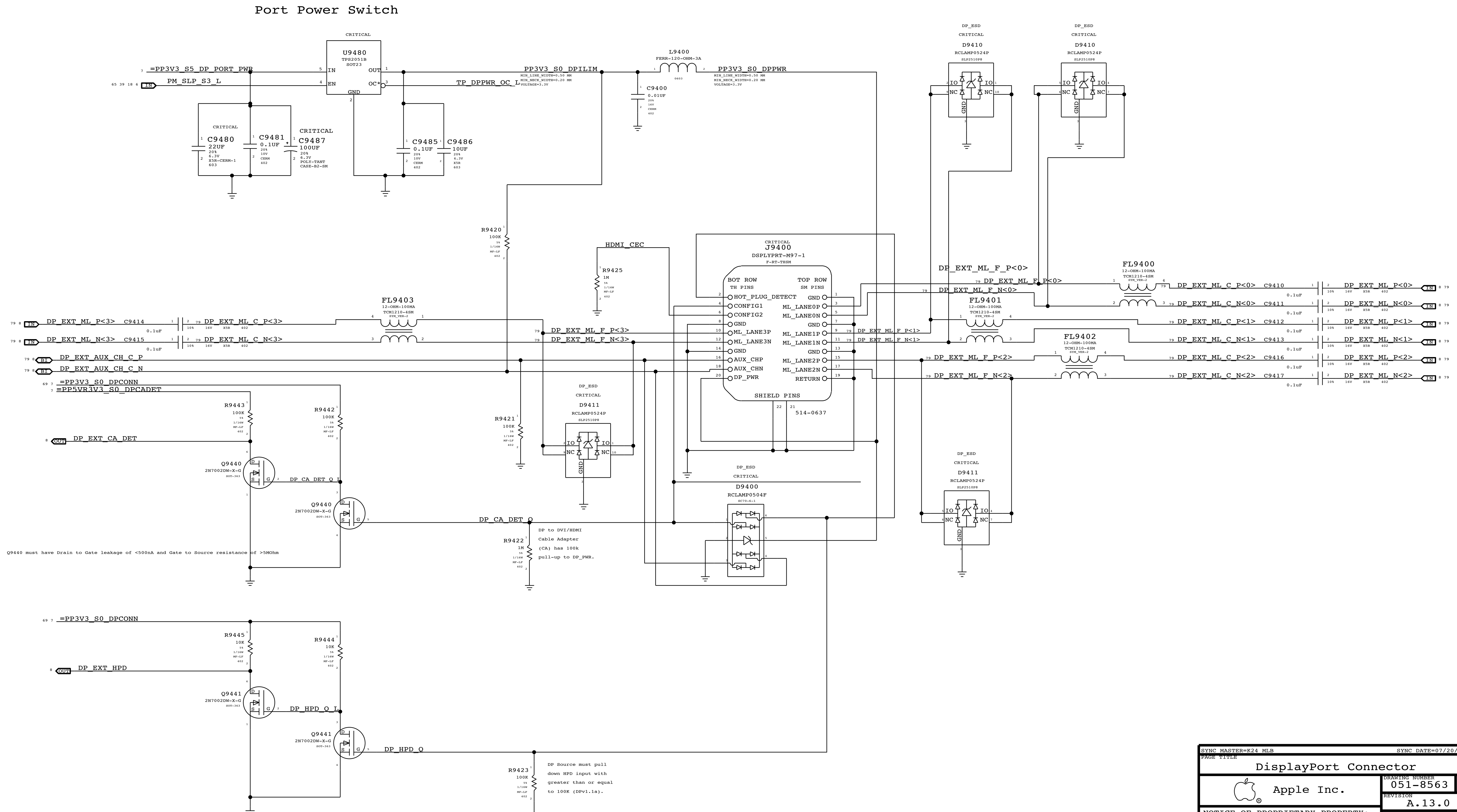

Port Power Switch
CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
IN
EN
OUT
OC*
GND
PP3V3_S0_DPILIM
TP_DPPWR_OC_L
L9400
FERR-120-OHM-3A
PP3V3_S0_DPPWR
C9400
0.01UF
C9480
22UF
C9481
0.1UF
C9487
100UF
C9485
0.1UF
C9486
10UF
R9420
100K
HDMI_CEC
R9425
1M
J9400
DSPLYPRT-M97-1
F-RT-THSM
BOT ROW
TH PINS
TOP ROW
SM PINS
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS
514-0637
DP_ESD
D9410
RCLAMP0524P
FL9400
FL9401
FL9402
FL9403
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_P<3>
DP_EXT_ML_N<3>
DP_EXT_ML_C_P<3>
DP_EXT_ML_C_N<3>
DP_EXT_ML_F_P<3>
DP_EXT_ML_F_N<3>
DP_EXT_AUX_CH_C_P
DP_EXT_AUX_CH_C_N
DP_EXT_ML_F_P<0>
DP_EXT_ML_F_N<0>
DP_EXT_ML_C_P<0>
DP_EXT_ML_C_N<0>
DP_EXT_ML_P<0>
DP_EXT_ML_N<0>
DP_EXT_ML_F_P<1>
DP_EXT_ML_F_N<1>
DP_EXT_ML_C_P<1>
DP_EXT_ML_C_N<1>
DP_EXT_ML_P<1>
DP_EXT_ML_N<1>
DP_EXT_ML_F_P<2>
DP_EXT_ML_F_N<2>
DP_EXT_ML_C_P<2>
DP_EXT_ML_C_N<2>
DP_EXT_ML_P<2>
DP_EXT_ML_N<2>
C9410
C9411
C9412
C9413
C9414
C9415
C9416
C9417
0.1uF
=PP3V3_S0_DPCONN
=PP5VR3V3_S0_DPCADET
R9443
100K
R9442
100K
DP_EXT_CA_DET
Q9440
2N7002DW-X-G
DP_CA_DET_Q_L
DP_CA_DET_Q
R9421
100K
D9411
RCLAMP0524P
D9400
RCLAMP0504F
R9422
1M
DP to DVI/HDMI
Cable Adapter
(CA) has 100k
pull-up to DP_PWR.
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm
R9445
10K
R9444
10K
DP_EXT_HPD
Q9441
2N7002DW-X-G
DP_HPD_Q_L
DP_HPD_Q
R9423
100K
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

SYNC_MASTER=K24_MLB SYNC_DATE=07/20/2009

PAGE TITLE

DisplayPort Connector

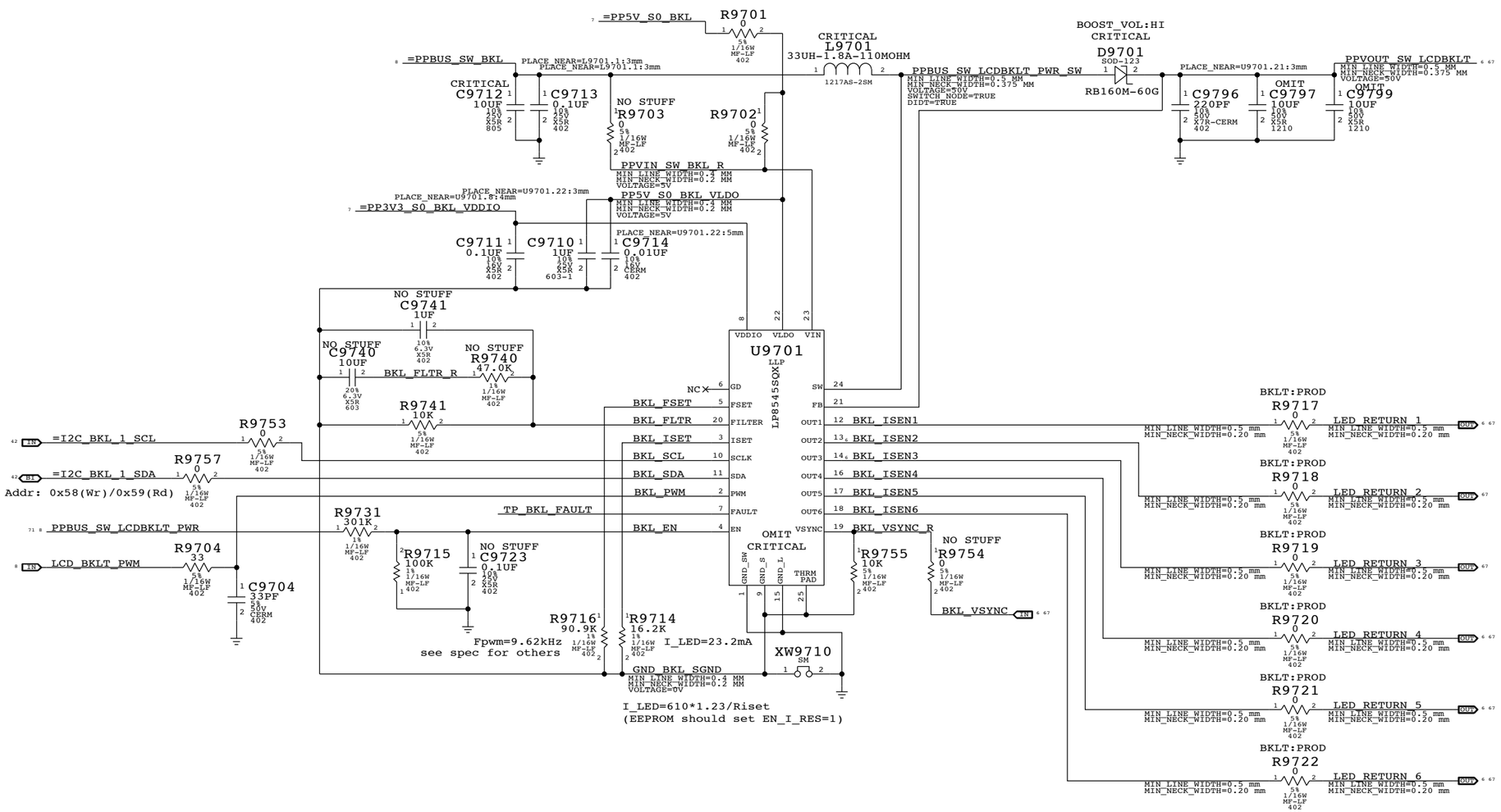
Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

REVISION A.13.0

BRANCH

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



FOR LP8543:
STUFF R9741
NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
371S0580	1	SCHOTTKY BARRIER DIODE RB160M-40	D9701		BOOST_VOL:LOW
138S0673	2	CAP, 50V, 1210, X5R, 10UF+/-10%	C9797,C9799	CRITICAL	

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K69_MLB SYNC_DATE=08/27/2009

PAGE TITLE
LCD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D
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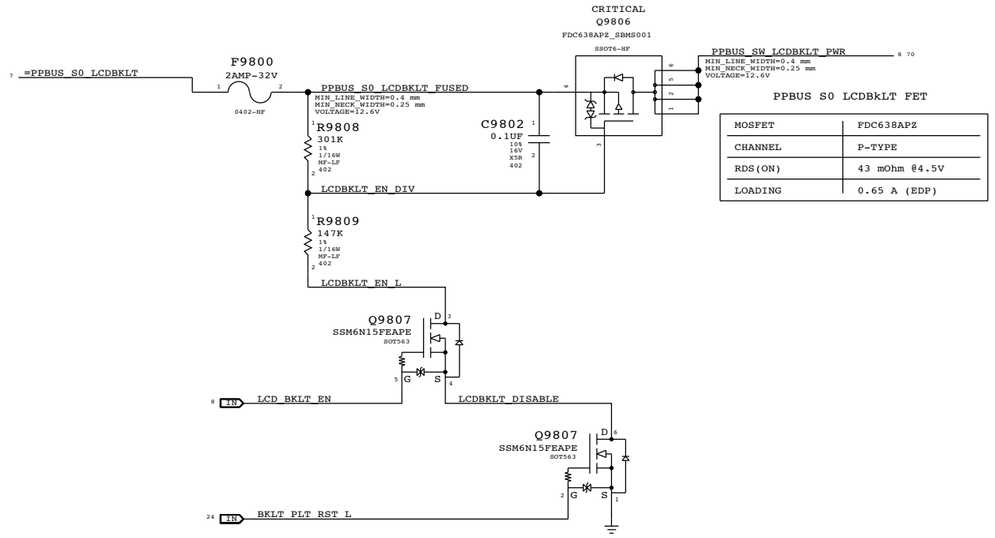

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

SYNC MASTER=T27 MLB SYNC DATE=07/28/2009

PAGE TITLE

LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-8563 SIZE D

REVISION A.13.0

BRANCH

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	6 9 13
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	6 9 13
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	6 9 13
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	6 9 13
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	6 9 13
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	6 9 13
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	6 9 13
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	6 9 13
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	6 9 13
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	6 9 13
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	6 9 13
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	6 9 13
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	6 9 13
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	6 9 13
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	6 9 13
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	6 9 13
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	6 9 13
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	6 9 13
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	6 9 13
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	6 9 13
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	6 9 13
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	6 9 13
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	6 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	6 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	6 9 13
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 12 13
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	9 13
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	8 9
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	9 13
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	9 13
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 13
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 13
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9 13 40 61
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9 12 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	9 13
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	9 13 40
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9 13
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	9 13
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 13 61
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	9 13
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9 13
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9 13
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	12 13
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	12 13
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	13
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	13
	CPU_IERR_L	CPU_50S		CPU_IERR_L	9
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	13 61
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	61
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	13
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	9 28
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	9
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	9
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	9 12
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	9 12
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	9 12
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	9 12
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	9 12
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	9 12
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	9 12
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	12
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	10 61
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10 61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

SYNC_MASTER=T27_MLB SYNC_DATE=08/03/2009

PAGE TITLE: CPU/FSB Constraints

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
MEM_CLK2MEM	*	=4:1_SPACING	?	NV DG says 3x inner, 4x outer
MEM_CTRL2CTRL	*	=2:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CTRL2MEM	*	=2.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2CMD	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2DATA	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DQS2MEM	*	=3:1_SPACING	?	NV DG says 4x inner, 5x outer
MEM_2OTHER	*	25 MIL	?	

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_P<5..0>	14 25
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_N<5..0>	14 25
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM_A_CKE<3..0>	14 20 25
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_CS_L<3..0>	14 25
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_ODT<3..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	14 25
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	14 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	14 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	14 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	14 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	14 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	14 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	14 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	14 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	14 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	14 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	14 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	14 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	14 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	14 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	14 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	14 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	14 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	14 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	14 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	14 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	14 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	14 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	14 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	14 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	14 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	14 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	14 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	14 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	14 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	14 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	14 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	14 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_P<5..0>	14 26
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_N<5..0>	14 26
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM_B_CKE<3..0>	14 20 26
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_CS_L<3..0>	14 26
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_ODT<3..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	14 26
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	14 27
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	14 27
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	14 27
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	14 27
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	14 27
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	14 27
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	14 27
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	14 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	14 27
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	14 27
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	14 27
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	14 27
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	14 27
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	14 27
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	14 27
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	14 27
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	14 27
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	14 27
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	14 27
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	14 27
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	14 27
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	14 27
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	14 27
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	14 27
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	14 27
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	14 27
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	14 27
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	14 27
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	14 27
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	14 27
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	14 27
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	14 27
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	14
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	14

SYNC MASTER=T27 MLB SYNC DATE=08/03/2009

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

	NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG_R2D_P<15..0>
	PCIE_90D	PCIE	PEG_R2D_N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>
	PCIE_90D	PCIE	PEG_D2R_N<15..0>
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>
	PCIE_90D	PCIE	PCIE_AP_R2D_P 6 29
	PCIE_90D	PCIE	PCIE_AP_R2D_N 6 29
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE_AP_R2D_C_P 15 29
	PCIE_90D	PCIE	PCIE_AP_R2D_C_N 15 29
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE_AP_D2R_P 6 15 29
	PCIE_90D	PCIE	PCIE_AP_D2R_N 6 15 29
	PCIE_90D	PCIE	PCIE_ENET_R2D_P 31
	PCIE_90D	PCIE	PCIE_ENET_R2D_N 31
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE_ENET_R2D_C_P 15 31
	PCIE_90D	PCIE	PCIE_ENET_R2D_C_N 15 31
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE_ENET_D2R_P 15 31
	PCIE_90D	PCIE	PCIE_ENET_D2R_N 15 31
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_P 31
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_N 31
	PCIE_90D	PCIE	PCIE_FW_R2D_P 33
	PCIE_90D	PCIE	PCIE_FW_R2D_N 33
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P 15 33
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N 15 33
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P 15 33
	PCIE_90D	PCIE	PCIE_FW_D2R_N 15 33
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P 33
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N 33
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P 8 15
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N 8 15
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_P 15 29
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_N 15 29
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P 15 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N 15 31
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P 15 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N 15 33
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMP 15
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR 8
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y 8
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB 8
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC 8
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC 8
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET 8
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF 8
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS_IG_TXC_P
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS_IG_TXC_N
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS_IG_TXD_P<5..0>
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS_IG_TXD_N<5..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML_P<3..0> 8
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML_N<3..0> 8
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH_P 8 68
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH_N 8 68
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET 16 23
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE 16 23
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P 8 67
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N 8 67
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0> 6 8 67
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0> 6 8 67
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET 16 23
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE 16 23
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 17 36
	SATA_90D	SATA	SATA_HDD_R2D_C_N 17 36
	SATA_90D	SATA	SATA_HDD_R2D_P 6 36
	SATA_90D	SATA	SATA_HDD_R2D_N 6 36
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 17 36
	SATA_90D	SATA	SATA_HDD_D2R_N 17 36
	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 36
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 36
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 17 36
	SATA_90D	SATA	SATA_ODD_R2D_C_N 17 36
	SATA_90D	SATA	SATA_ODD_R2D_P 6 36
	SATA_90D	SATA	SATA_ODD_R2D_N 6 36
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 17 36
	SATA_90D	SATA	SATA_ODD_D2R_N 17 36
	SATA_90D	SATA	SATA_ODD_D2R_C_P 36
	SATA_90D	SATA	SATA_ODD_D2R_C_N 36
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP 17

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 18 39 41
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 18 39 41
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 18 24
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 18 24
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 24 39
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 24 41
USB_EXTA	USB_90D	USB	USB_EXTA_P 17 37
	USB_90D	USB	USB_EXTA_N 17 37
	USB_90D	USB	USB_EXTA_MUXED_P 37 79
	USB_90D	USB	USB_EXTA_MUXED_N 37 79
USB_MINI	USB_90D	USB	USB_MINI_P 8 17
	USB_90D	USB	USB_MINI_N 8 17
USB_EXTD	USB_90D	USB	USB_EXTD_P 8 17
	USB_90D	USB	USB_EXTD_N 8 17
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 17 29
	USB_90D	USB	USB_CAMERA_N 17 29
USB_BT	USB_90D	USB	USB_BT_P 17 29
	USB_90D	USB	USB_BT_N 17 29
USB_TPAD	USB_90D	USB	USB_TPAD_P 17 47
	USB_90D	USB	USB_TPAD_N 17 47
USB_IR	USB_90D	USB	USB_IR_P 17 38
	USB_90D	USB	USB_IR_N 17 38
USB_EXTB	USB_90D	USB	USB_EXTB_P 17 37
	USB_90D	USB	USB_EXTB_N 17 37
USB_T57	USB_90D	USB	USB_T57_P 6 38
	USB_90D	USB	USB_T57_N 6 38
USB_EXTC	USB_90D	USB	USB_EXTC_P 8 17
	USB_90D	USB	USB_EXTC_N 8 17
USB_SDCARD	USB_90D	USB	USB_SDCARD_P 17 30
	USB_90D	USB	USB_SDCARD_N 17 30
USB_WM	USB_90D	USB	USB_WM_P 8 17
	USB_90D	USB	USB_WM_N 8 17
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 17
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 12 18 42
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 12 18 42
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS_MCP_1_CLK 18 42
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS_MCP_1_DATA 18 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 18 51
	HDA_55S	HDA	HDA_BIT_CLK_R 18
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 18 51
	HDA_55S	HDA	HDA_SYNC_R 18
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 18
	HDA_55S	HDA	HDA_RST_L 18 51
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 18 51
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 18 51
	HDA_55S	HDA	HDA_SDOUT_R 18
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 18
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 18 24
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 24 39
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 18 41
	SPI_55S	SPI	SPI_CLK 6 41
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 18 41
	SPI_55S	SPI	SPI_MOSI 6 41
SPI_MISO	SPI_55S	SPI	SPI_MISO 6 18 41
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 18 41
	SPI_55S	SPI	SPI_CS0_L 6 41
	SPI_55S	SPI	SPI_MLB_CLK 41 50
	SPI_55S	SPI	SPI_MLB_MOSI 41 50
	SPI_55S	SPI	SPI_MLB_MISO 41 50
	SPI_55S	SPI	SPI_MLB_CS_L 41 50
	SPI_55S	SPI	SPI_ALT_CLK 41
	SPI_55S	SPI	SPI_ALT_MOSI 41
	SPI_55S	SPI	SPI_ALT_MISO 41
	SPI_55S	SPI	SPI_ALT_CS_L 41

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	17
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	17
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	8 17
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	8 17
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	8 17
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	8 17
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	8 17
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	
	ENET_MII_55S	ENET_MII	ENET_RESET_L	24 31

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31 32
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31 32

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SD_DATA	SD_55S	SD_INTERFACE	SD_D<4..0>	30
	SD_55S	SD_INTERFACE	SDCONN_DATA<4..0>	30 31
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>	31
SD_DATA_R	SD_55S	SD_INTERFACE	SD_D<7..5>	30
	SD_55S	SD_INTERFACE	SDCONN_DATA<7..5>	30 31
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>	31
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	30
	SD_55S	SD_INTERFACE	SD_CLK_R	30
	SD_55S	SD_INTERFACE	SDCONN_CLK	30 31
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	30
	SD_55S	SD_INTERFACE	SDCONN_CMD	30 31
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD	31

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING
FW_P0_TPA	FW_100D	FW_TP
FW_P0_TPA	FW_100D	FW_TP
FW_P0_TPB	FW_100D	FW_TP
FW_P0_TPB	FW_100D	FW_TP
FW_P1_TPA	FW_100D	FW_TP
FW_P1_TPA	FW_100D	FW_TP
FW_P1_TPB	FW_100D	FW_TP
FW_P1_TPB	FW_100D	FW_TP

Port 2 Not Used

FW_P0_TPA_P 33 35
FW_P0_TPA_N 33 35
FW_P0_TPB_P 33 35
FW_P0_TPB_N 33 35
FW_P1_TPA_P 33 35
FW_P1_TPA_N 33 35
FW_P1_TPB_P 33 35
FW_P1_TPB_N 33 35

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FireWire Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	6 42
SMBUS_SMC_A_S3_SDA	SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	6 42
SMBUS_SMC_B_S0_SCL	SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	42
SMBUS_SMC_B_S0_SDA	SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	42
SMBUS_SMC_0_S0_SCL	SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	42
SMBUS_SMC_0_S0_SDA	SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	42
SMBUS_SMC_BSA_SCL	SMB_5S	SMB	SMBUS_SMC_BSA_SCL	6 42
SMBUS_SMC_BSA_SDA	SMB_5S	SMB	SMBUS_SMC_BSA_SDA	6 42
SMBUS_SMC_MGMT_SCL	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	42
SMBUS_SMC_MGMT_SDA	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	58
	1TO1_DIFFPAIR		CHGR_CSI_N	58
	1TO1_DIFFPAIR		CHGR_CSI_R_P	58
	1TO1_DIFFPAIR		CHGR_CSI_R_N	58
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	58
	1TO1_DIFFPAIR		CHGR_CSO_N	58
	1TO1_DIFFPAIR		CHGR_CSO_R_P	44 58
	1TO1_DIFFPAIR		CHGR_CSO_R_N	44 58

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(PCIE_AP)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P 6 29
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N 6 29
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_P 37 75
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_N 37 75
(USB_EXTA)	USB_90D	USB	USB_LT1_P 37
(USB_EXTA)	USB_90D	USB	USB_LT1_N 37
(USB_TPAD)	USB_90D	USB	USB_TPAD_R_P 47
(USB_TPAD)	USB_90D	USB	USB_TPAD_R_N 47
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P 6 29
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N 6 29
	USB_90D	USB	USB_BT_CONN_P 6 29
	USB_90D	USB	USB_BT_CONN_N 6 29
	USB_90D	USB	USB_LT2_P 37
	USB_90D	USB	USB_LT2_N 37
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0> 32
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0> 32
	SATA_90D	SATA	SATA_ODD_R2D_UF_P 36
	SATA_90D	SATA	SATA_ODD_R2D_UF_N 36
	SATA_90D	SATA	SATA_ODD_D2R_UF_P 6 36
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 6 36
	SATA_90D	SATA	SATA_HDD_D2R_UF_P 36
	SATA_90D	SATA	SATA_HDD_D2R_UF_N 36
	SATA_90D	SATA	SATA_HDD_R2D_UF_P 36
	SATA_90D	SATA	SATA_HDD_R2D_UF_N 36
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P 36
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N 36
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P 36
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N 36
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P 36
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N 36
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P 36
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N 36
	SATA_90D	SATA	SATA_HDD_D2R_NORDRV_P 36
	SATA_90D	SATA	SATA_HDD_D2R_NORDRV_N 36
	SATA_90D	SATA	SATA_HDD_R2D_NORDRV_P 36
	SATA_90D	SATA	SATA_HDD_R2D_NORDRV_N 36

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P 6 67
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N 6 67
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML_P<3..0> 8 69
	DP_90D	DISPLAYPORT	DP_EXT_ML_N<3..0> 8 69
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_P<3..0> 69
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_N<3..0> 69
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_P<3..0> 69
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_N<3..0> 69
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_P 8 69
	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_N 8 69
	DP_90D	DISPLAYPORT	DP_AUX_CH_SW_P
	DP_90D	DISPLAYPORT	DP_AUX_CH_SW_N

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 45
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N 45
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P 9 45
	THERM_1TO1_55S	THERM	CPU_THERMD_N 9 45
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MCPTHMSNS_D2_P
	THERM_1TO1_55S	THERM	MCPTHMSNS_D2_N
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P 18 45
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N 18 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_P
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_P
	SENSE_1TO1_55S	SENSE	ISNS_ODD_N
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPUVTT_P 44
	SENSE_1TO1_55S	SENSE	ISNS_CPUVTT_N 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_P 21 62
	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_N 21 62
PWR		MEM_POWER	PP1V5R1V35_S3 6 7
		SB_POWER	PP3V3_S5 6 7 65
		SB_POWER	PP3V3_S0 6 7 65
		SB_POWER	PP1V5_S0 6 7 65
		GND	GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	DIFFPAIR	AUDIO	AUD_SPKRAMP_LIN_P
	DIFFPAIR	AUDIO	AUD_SPKRAMP_LIN_N
	DIFFPAIR	AUDIO	AUD_SPKRAMP_SUBIN_P
	DIFFPAIR	AUDIO	AUD_SPKRAMP_SUBIN_N
	DIFFPAIR	AUDIO	AUD_SPKRAMP_RIN_P
	DIFFPAIR	AUDIO	AUD_SPKRAMP_RIN_N
	DIFFPAIR	AUDIO	SSM2315L_P
	DIFFPAIR	AUDIO	SSM2315L_N
	DIFFPAIR	AUDIO	SSM2315S_P
	DIFFPAIR	AUDIO	SSM2315S_N
	DIFFPAIR	AUDIO	SSM2315R_P
	DIFFPAIR	AUDIO	SSM2315R_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N
	DIFFPAIR	AUDIO	BI_MIC_P
	DIFFPAIR	AUDIO	BI_MIC_N
	DIFFPAIR	AUDIO	HS_MIC_P
	DIFFPAIR	AUDIO	HS_MIC_N

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K6/K69 Specific Constraints

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K6/K69 Board-Specific Physical & Spacing Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.080 MM	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.109 MM	=STANDARD	0.224 MM	0.090 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5X_DIELECTRIC	TOP,BOTTOM	0.105 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
1.5X_DIELECTRIC	*	0.095 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_LPC	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA	STANDARD

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