Advance Information

MPC7455BPXPNS/D
Rev. 1, 7/2003

MPC7455 Part Number Specification for the XC7455BRXnnnPx Series

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Motorola Part Numbers Affected:

XC7455BRX1000PF
XC7455BRX1250PF
XC7455BRX1333PF
XC7455BRX1400PF

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7455 RISC Microprocessor Hardware Specifications* (Order No. MPC7455EC/D). The products described here are PowerPC™ microprocessors.

Specifications provided in this document supersede those in the *MPC7455 RISC Microprocessor Hardware Specifications*, Rev. 2 or later, for the part numbers listed in A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in A.

Table A. Part Numbers Addressed by this Data Sheet

Motorola Part Numbers	Operating Conditions			Significant Differences from Hardware Specification
	Max. Core Frequency (MHz)	V_{DD}	T_J (°C)	
XC7455BRX1000PF	1000	1.57 V +30/–50 mV	0 to 65	Modified core voltage, temperature and system bus AC specifications, support for 167-MHz system bus in MPX mode.
XC7455BRX1250PF	1250			
XC7455BRX1333PF	1333			
XC7455BRX1400PF	1400	1.61 V +30/–50 mV		

Note: The X prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.1 Features

This section summarizes changes to the features of the MPC7455 described in the *MPC7455 RISC Microprocessor Hardware Specifications*.

- Power management
  - See Table 4 for nominal processor core voltage

1.4 General Parameters

- Core power supply: See Table 4 for nominal processor core voltage

1.5.1DC Electrical Characteristics

Table 4 provides the recommended operating conditions for the MPC7455 part numbers described herein.

Table 4. Recommended Operating Conditions

Characteristic	Speed Grade	Symbol	Recommended Value	Unit
Core supply voltage	1000, 1250, 1333 MHz	V_{DD}	1.57 V +30/–50 mV	V
	1400 MHz		1.61 V +30/–50 mV	
PLL supply voltage	1000, 1250, 1333 MHz	AV_{DD}	1.57 V +30/–50 mV	V
	1400 MHz		1.61 V +30/–50 mV	
Die-junction temperature	All	T_j	0 to 65	°C

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 7 provides the power consumption for the MPC7455 part numbers described herein.

Table 7. Power Consumption for MPC7455

	Processor Core Frequency		Unit	Notes
	1000, 1250, 1333 MHz	1400 MHz		
Full-Power Mode				
Typical	30.0	34.0	W	1, 3
Maximum	40.0	45.0	W	1, 2
Doze Mode				
Typical	—	—	W	1, 2, 4
Nap Mode				
Typical	8.0	8.0	W	1, 2
Sleep Mode				
Typical	8.0	8.0	W	1, 2
Deep Sleep Mode (PLL Disabled)				
Typical	8.0	8.0	W	1, 3

Notes:

1. These values apply for all valid processor bus and L3 bus ratios. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} and GV_{DD} power is system dependent, but is typically <5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Maximum power is measured at nominal V_{DD} while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, with or without AltiVec, maximally busy.
3. Typical power is an average value measured at nominal V_{DD} and 65°C in a system while running a typical code sequence.
4. Doze mode is not a user-definable state; it is an intermediate state between Full-power and either Nap or Sleep mode. As a result, power consumption for this mode is not tested.

1.5.2.1 Clock AC Specifications

Table 9. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Processor Core Frequency								Unit
		1000 MHz		1250 MHz		1333 MHz		1400 MHz		
		Min	Max	Min	Max	Min	Max	Min	Max	
Processor frequency	f_{core}	500	1000	500	1250	500	1333	500	1400	MHz
VCO frequency	f_{VCO}	1000	2000	1000	2500	1000	2666	1000	2800	MHz
SYSCLK frequency	f_{SYSCLK}									MHz
MPX bus mode		33	167	33	167	33	167	33	167	
60x bus mode		33	133	33	133	33	133	33	133	
SYSCLK cycle time	t_{SYSCLK}									ns
MPX bus mode		6.0	30	6.0	30	6.0	30	6.0	30	
60x bus mode		7.5	30	7.5	30	7.5	30	7.5	30	

1.5.2.2 Processor Bus AC Specifications

Table 10. Processor Bus AC Timing Specifications

At recommended operating conditions. See Table 4.

Parameter	Symbol	MPX bus mode		60x bus mode		Unit
		Min	Max	Min	Max	
Input setup times: A[0:35], AP[0:4], GBL, TBST, TSIZ[0:2], WT, CI, D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], HRESET, INT, MCP, QACK, SMI, SRESET, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1]	t_{AVKH} t_{IVKH}	1.5 1.5	— —	2.0 2.0	— —	ns
Input hold times: A[0:35], AP[0:4], GBL, TBST, TSIZ[0:2], WT, CI, D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], HRESET, INT, MCP, QACK, SMI, SRESET, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1]	t_{AXKH} t_{IXKH}	0 0	— —	0 0	— —	ns
Output valid times: A[0:35], AP[0:4], GBL, TBST, TSIZ[0:2], WT, CI TS D[0:63], DP[0:7] ARTRY/SHD0/SHD1 BR, CKSTP_OUT, DRDY, HIT, PMON_OUT, QREQ]	t_{KHAV} t_{KHTSV} t_{KHDV} t_{KHARV} t_{KHOV}	— — — — —	2.0 2.0 2.0 2.0 2.0	— — — — —	2.5 2.5 2.5 2.5 2.5	ns
Output hold times: A[0:35], AP[0:4], GBL, TBST, TSIZ[0:2], WT, CI TS D[0:63], DP[0:7] ARTRY/SHD0/SHD1 BR, CKSTP_OUT, DRDY, HIT, PMON_OUT, QREQ	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHARX} t_{KHOX}	0.5 0.5 0.5 0.5 0.5	— — — — —	0.5 0.5 0.5 0.5 0.5	— — — — —	ns

1.11 Ordering Information

1.11.1 Part Numbers Addressed by this Specification

Table 20 provides the ordering information for the MPC7455 parts described in this document.

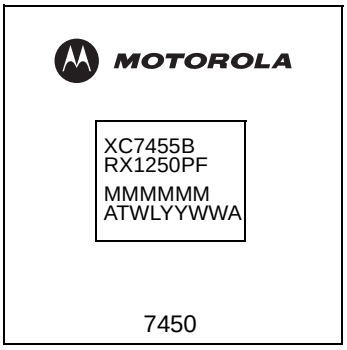
Table 20. Part Marking Nomenclature

XC	7455	B	RX	*nnn*	*x*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package**	**Processor Frequency [1]**	**Application Modifier**	**Revision Level**
XC [2]	7455	B	RX = CBGA	1000 1250 1333	P: 1.57 V +30/–50 mV 0 to 65°C	F: 3.3; PVR = 8001 0303
				1400	P: 1.61 V +30/–50 mV 0 to 65°C	

Notes:
1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.
2. The X prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.11.3 Part Marking

Parts are marked as the example shown in Figure 27.



BGA

Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 27. Motorola Part Marking for BGA Device

Document Revision History

Table B provides a revision history for this part number specification.

Table B. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
1	Corrected processor core voltage specifications for 1400 MHz device (changed from 1.57 V to 1.61 V); this was a documentation error only and does not reflect a change in the test regime or supported core voltage for this device.

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